优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Features

- I_{USB} = 35A typical
- BV_{CES} > 80V
- BV_{CEO} > 15V
- Specifically Designed for Low Voltage Avalanche Mode Operation

Mechanical Data

- Package: SOT23
- Package Material: Molded Plastic. “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin-Plated Leads. Solderable per MIL-STD-202, Method 208
- Weight: 0.008 grams (Approximate)

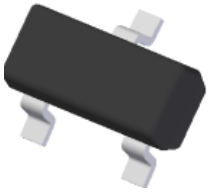
Description

The NK-FMMT411Q is a silicon planar bipolar transistor designed for operating in avalanche mode. Tight process control and low inductance packaging combine to produce high-current pulses with fast edges.

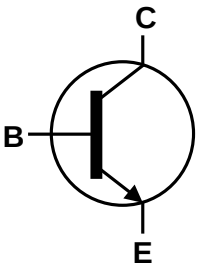
Applications

- Laser diode drivers for ranging and measurement (LIDAR)
- Fast edge switch generators
- High-speed pulse generators

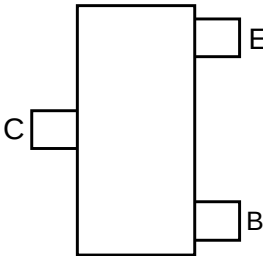
SOT23 (Type DN)



Top View



Device Symbol



Top View
Pin-Out

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage	V_{CES}	80	V
Collector-Emitter Voltage	V_{CEO}	15	V
Emitter-Base Voltage	V_{EBO}	7	V
Continuous Collector Current	I_C	900	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

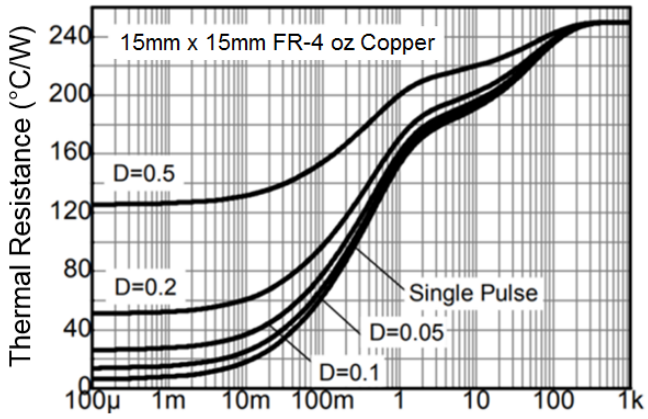
Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	800	mW
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	150	°C/W
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	30	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

ESD Ratings (Note 7)

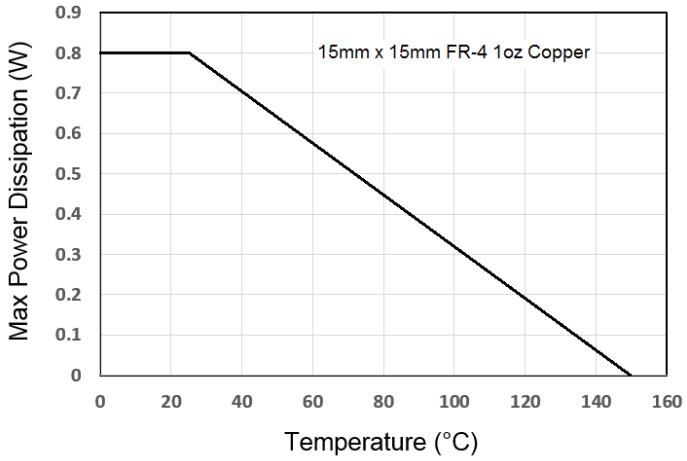
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	400	V	C

Notes:
5. For a device mounted with the collector lead on 15mm × 15mm 1oz copper that is on a single-sided 1.6mm FR-4 PCB; device is measured under still air conditions whilst operating in a steady state.
6. Thermal resistance from junction to top of case.
7. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

Thermal Characteristics and Derating information



Transient Thermal Impedance



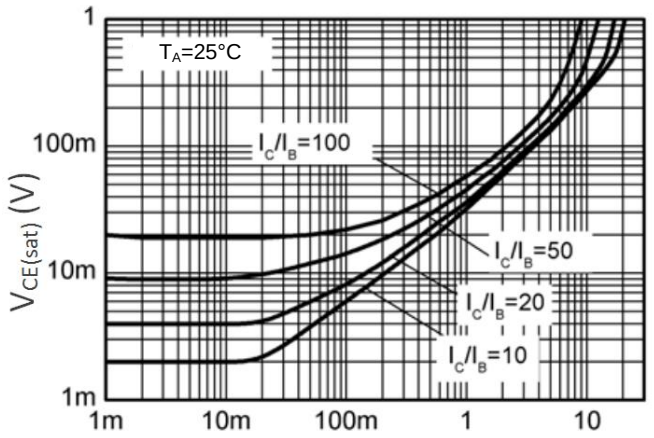
Derating Curve

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

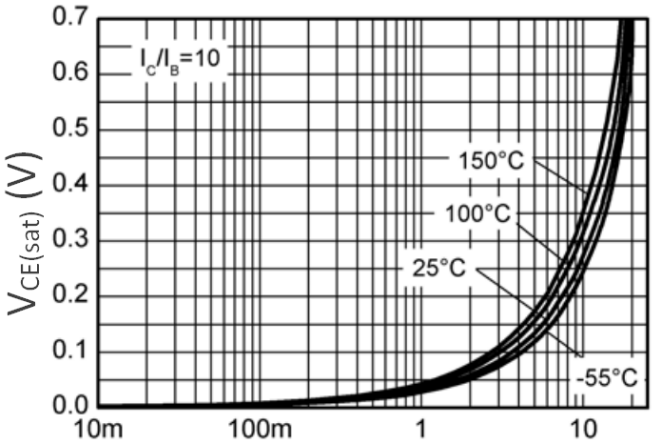
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV_{CBO}	80	—	—	V	I_C = 100μA
Collector-Emitter Breakdown Voltage	BV_{CES}	80 75	—	—	V	I_C = 100μA T_J = -50°C to +150°C
Collector-Emitter Breakdown Voltage	BV_{CEO}	15	—	—	V	I_C = 100μA
Emitter-Base Breakdown Voltage	BV_{EBO}	7	—	—	V	I_E = 100μA
Collector Cutoff Current	I_{CBO}	—	—	100 10	nA μA	V_{CB} = 75V V_{CB} = 75V, T_J = +100°C
Emitter Cutoff Current	I_{EBO}	—	—	20	nA	V_{EB} = 6V
Static Forward Current Transfer Ratio (Note 8)	h_{FE}	100	—	—	—	I_C = 10mA, V_{CE} = 10V
Collector-Emitter Saturation Voltage (Note 8)	$V_{CE(sat)}$	—	—	100	mV	I_C = 10mA, I_B = 1mA
Base-Emitter Saturation Voltage (Note 8)	$V_{BE(sat)}$	—	—	800	mV	I_C = 10mA, I_B = 1mA
Current in Second Breakdown (Pulsed) (Note 9)	I_{USB}	—	35	—	A	V_{CE} = 70V, C_{CE} = 470pF
Collector-Emitter Inductance	L_{ce}	—	2	—	nH	Standard SOT23 leads
Output Capacitance	C_{cbo}	—	15	—	pF	V_{CB} = 20V, f = 100MHz
Transition Frequency	f_T	40	—	—	MHz	V_{CE} = 20V, I_C = 10mA, f = 20MHz
Switching Times	t_d	—	118	—	ns	I_C = 100mA, V_{CC} = 10V I_{B1} = -I_{B2} = 10mA
	t_r	—	79	—	ns	
	t_s	—	388	—	ns	
	t_f	—	48	—	ns	

Notes: 8. Measured under pulsed conditions. Pulse width ≤ 300μs. Duty cycle ≤ 2%.
9. Dependent on circuit layout parasitics and base drive di/dt. Not production tested.

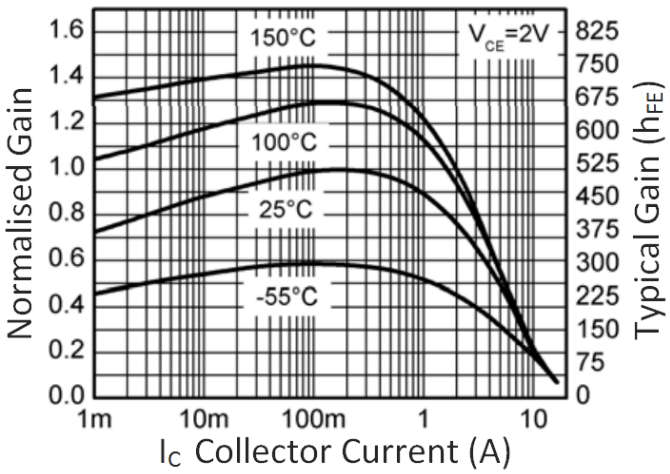
Typical Characteristics (@T_A = +25°C, unless otherwise specified.)



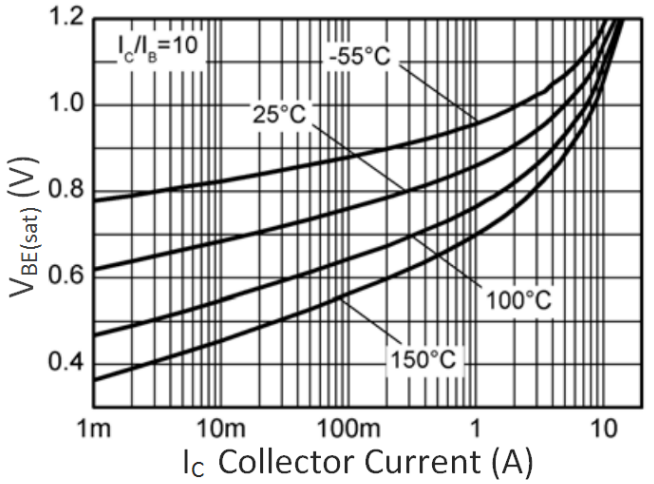
$V_{CE(sat)}$ vs I_C



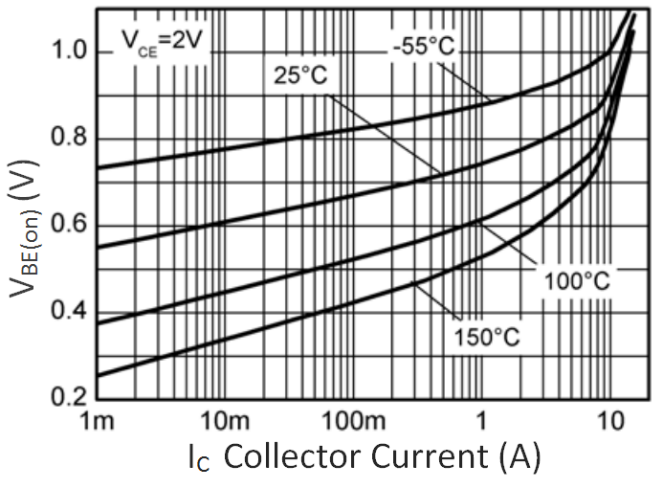
$V_{CE(sat)}$ vs I_C



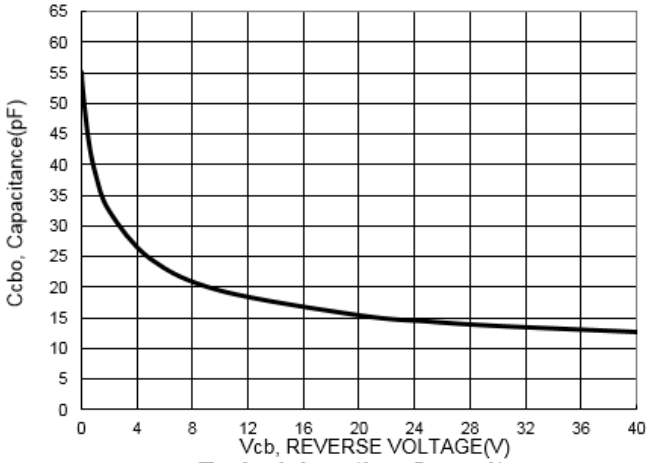
h_{FE} vs I_C



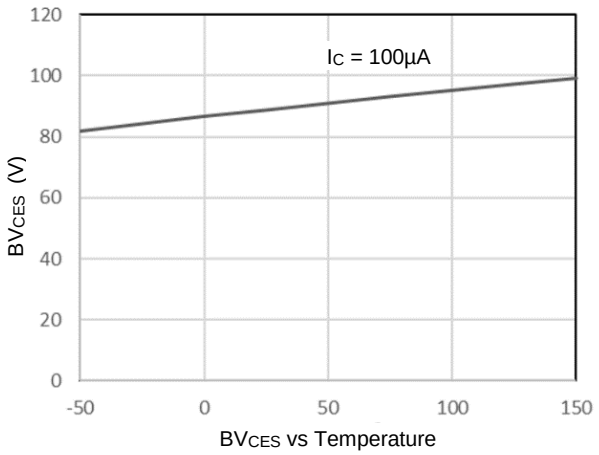
$V_{BE(sat)}$ vs I_C



$V_{BE(on)}$ vs I_C



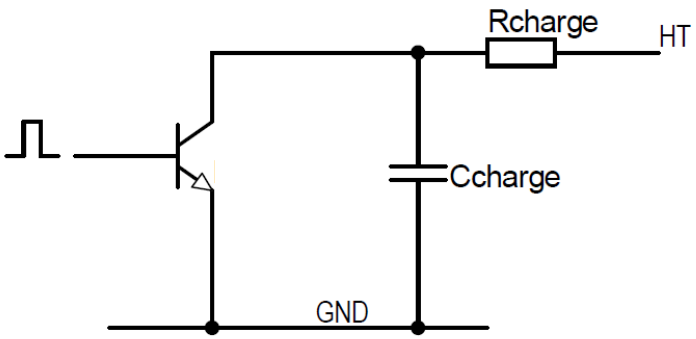
Typical Junction Capacitance



BVCES vs Temperature

Application Considerations

In a typical circuit a large pulse is applied to the base and the resultant energy is enough to cause the onset of avalanche multiplication. Once breakdown has been established it will continue until the energy in the breakdown region is insufficient to maintain the condition, or the crystal lattice is permanently damaged. It is important therefore to limit the total energy expended during breakdown. The typical method of achieving avalanche uses the circuit shown below, wherein the energy per cycle is set by the charge voltage and capacitance value.

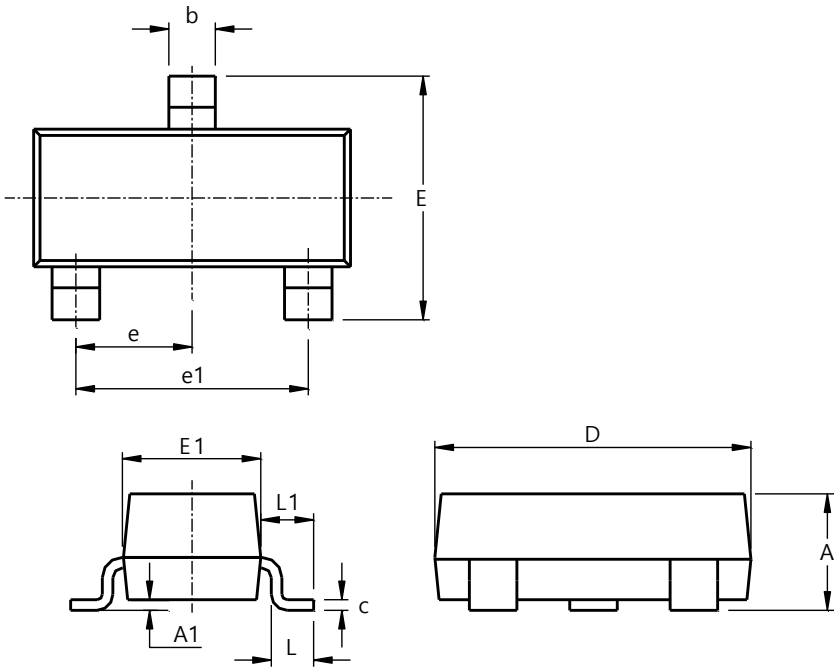


The effect of parasitic inductance in the circuit must be considered. Excessive inductance will reduce the current pulse height and slew current pulse edges. Loop area enclosed by the power circuit and track lengths should be minimized.

Thermal limitations must also be observed to ensure the transistor junction temperature is not exceeded. Avalanche power dissipation can be calculated from the energy per pulse and the pulse frequency, but PCB thermal resistance depends on many factors such as design, layout, and proximity of other components; so thermal performance should be verified by measurement.

Package Outline Dimensions

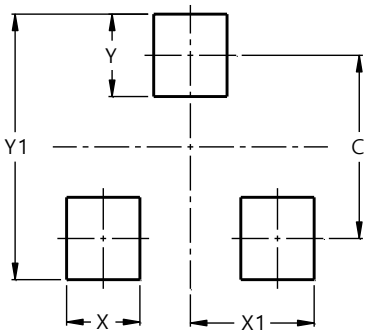
SOT23 (Type DN)



SOT23 Type DN			
Dim	**Min**	**Max**	**Typ**
A	0.89	1.12	1.00
A1	0.01	0.10	0.05
b	0.30	0.51	0.45
c	0.08	0.20	0.10
D	2.80	3.04	3.00
E	2.10	2.64	2.42
E1	1.20	1.40	1.37
e	0.95 REF		
e1	1.90 REF		
L	0.25	0.60	0.30
L1	0.45	0.62	0.54
All Dimensions in mm			

Suggested Pad Layout

SOT23 (Type DN)



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9