优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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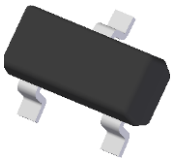
Features

- BV_{CEO} > -500V
- I_C = -150mA high Continuous Collector Current
- I_{CM} Up to -500mA Peak Pulse Current
- Excellent h_{FE} Characteristics up to I_C = -100mA

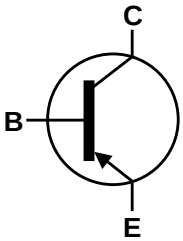
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight 0.008 grams (Approximate)

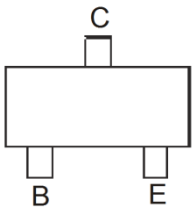
SOT23



Top View



Device Symbol



Top View
Pin-Out

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-500	V
Collector-Emitter Voltage	V_{CEO}	-500	V
Emitter-Base Voltage	V_{EBO}	-7	V
Continuous Collector Current	I_C	-150	mA
Peak Pulse Current	I_{CM}	-500	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

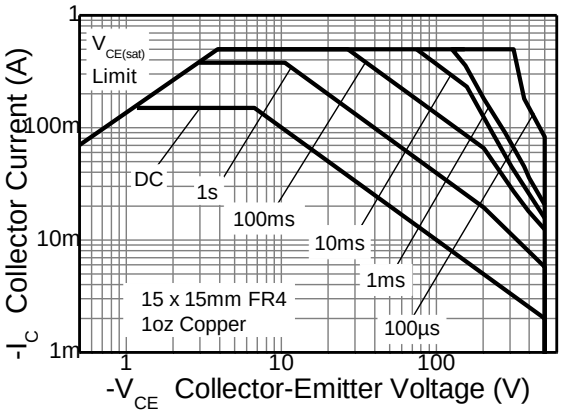
Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	500	mW
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	250	°C/W
Thermal Resistance, Junction to Lead	(Note 6)	$R_{\theta JL}$	194	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

ESD Ratings (Note 7)

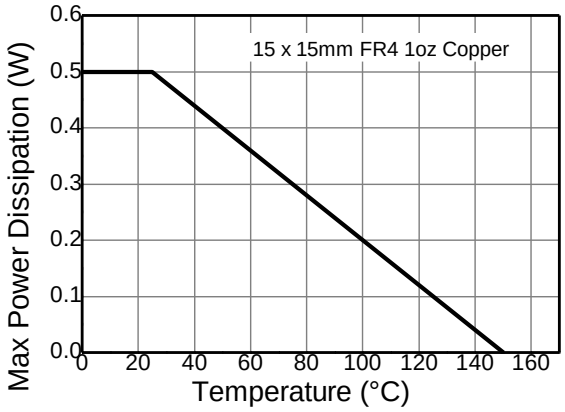
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge – Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge – Machine Model	ESD MM	400	V	C

Notes:
5. For a device mounted with the collector lead on 15mm x 15mm 1oz copper that is on a single-sided FR4 PCB; device is measured under still air conditions whilst operating in a steady-state.
6. Thermal resistance from junction to solder-point (at the end of the collector lead).
7. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

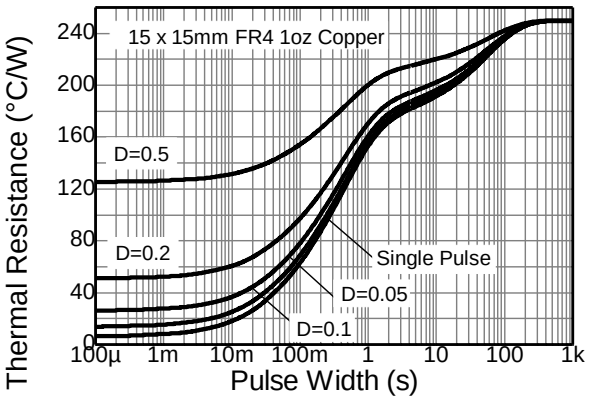
Thermal Characteristics and Derating Information



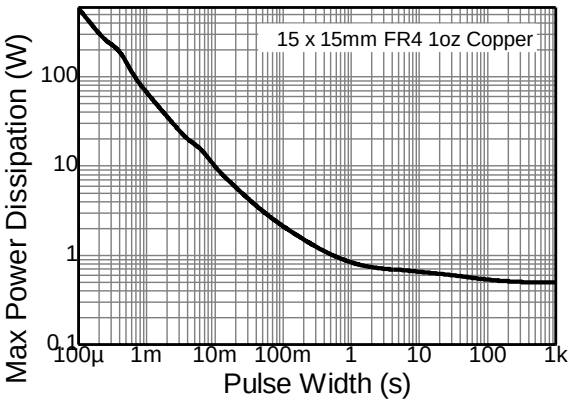
Safe Operating Area



Derating Curve



Transient Thermal Impedance



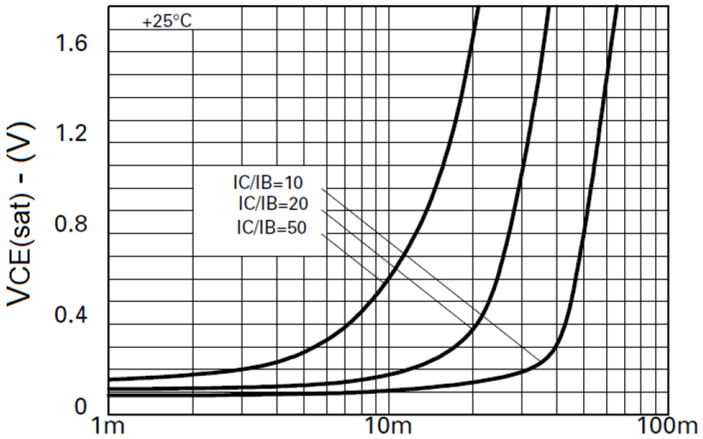
Pulse Power Dissipation

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

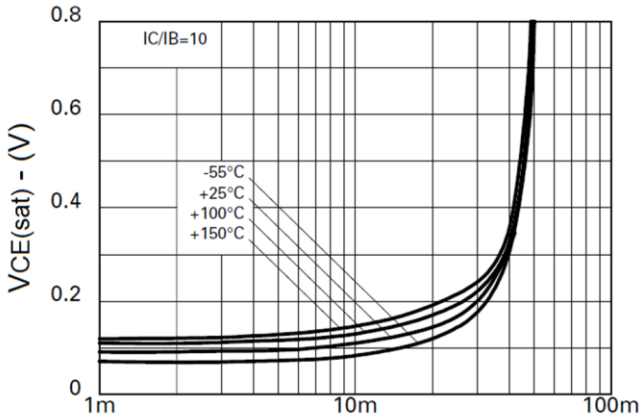
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV_{CBO}	-500	—	—	V	I_C = -100μA
Collector-Emitter Breakdown Voltage (Note 8)	BV_{CEO}	-500	—	—	V	I_C = -1mA
Emitter-Base Breakdown Voltage	BV_{EBO}	-7	—	—	V	I_E = -100μA
Collector Cutoff Current	I_{CBO}	—	—	-100	nA	V_{CB} = -500V
Emitter Cutoff Current	I_{EBO}	—	—	-100	nA	V_{EB} = -5V
Static Forward Current Transfer Ratio (Note 8)	h_{FE}	100 80 —	— — 15	300 300 —	—	I_C = -1mA, V_{CE} = -10V I_C = -50mA, V_{CE} = -10V I_C = -100mA, V_{CE} = -10V
Collector-Emitter Saturation Voltage (Note 8)	$V_{CE(SAT)}$	—	—	-200 -500	mV	I_C = - 20mA, I_B = -2mA I_C = - 50mA, I_B = -10mA
Base-Emitter Saturation Voltage (Note 8)	$V_{BE(SAT)}$	—	—	-0.9	V	I_C = -50mA, I_B = -10mA
Base-Emitter Turn-On Voltage (Note 8)	$V_{BE(ON)}$	—	—	-0.9	V	I_C = -50mA, V_{CE} = -10V
Output Capacitance	C_{OBO}	—	—	8	pF	V_{CB} = -20V, f = 1MHz
Transition Frequency	f_T	60	—	—	MHz	V_{CE} = -20V, I_C = -10mA, f = 50MHz
Turn-On Time	t_{ON}	—	110	—	ns	V_{CE} = -100V, I_C = -50mA, I_{B1} = -5mA, I_{B2} = 10mA
Turn-Off Time	t_{OFF}	—	1.5	—	μs	

Note: 8. Measured under pulsed conditions. Pulse width ≤ 300μs. Duty cycle ≤ 2%

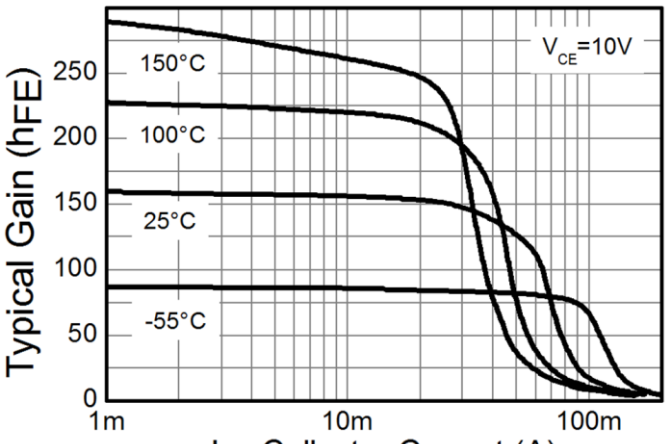
Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



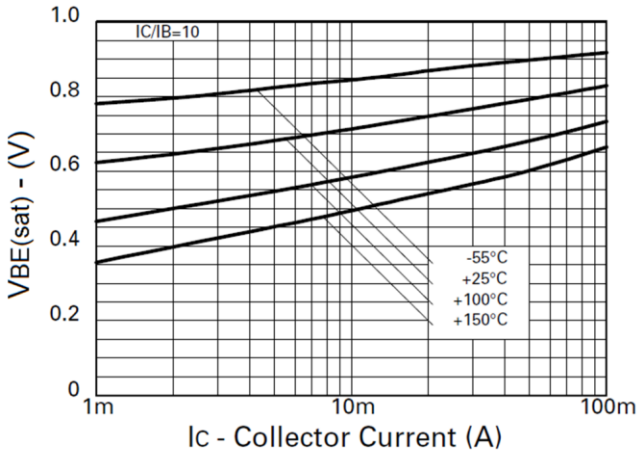
VCE(sat) v IC



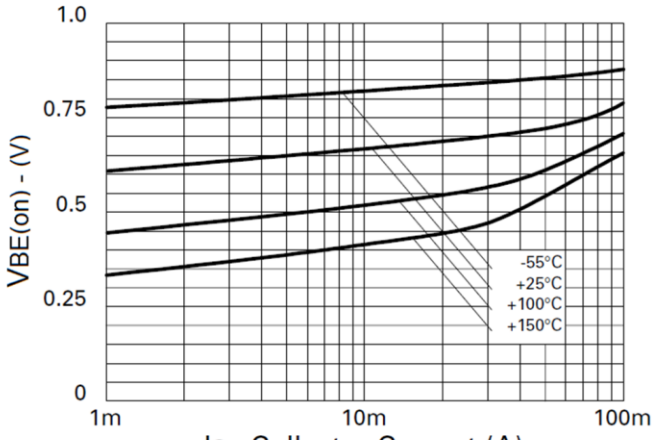
VCE(sat) v IC



hFE v IC



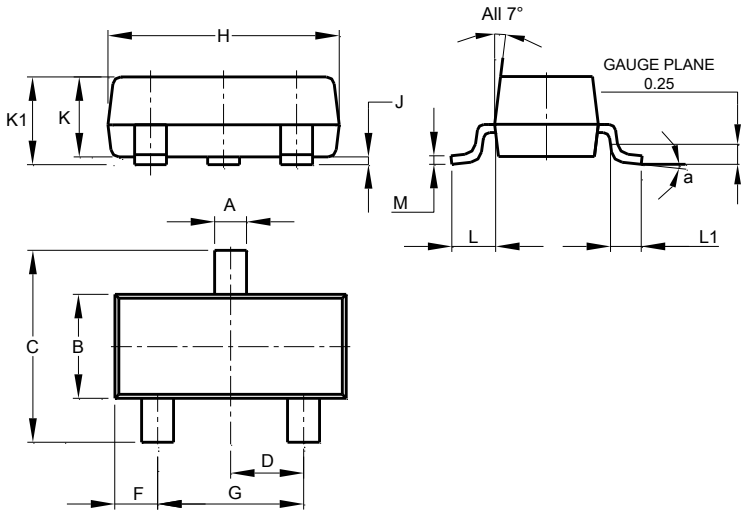
VBE(sat) v IC



VBE(on) v IC

Package Outline Dimensions

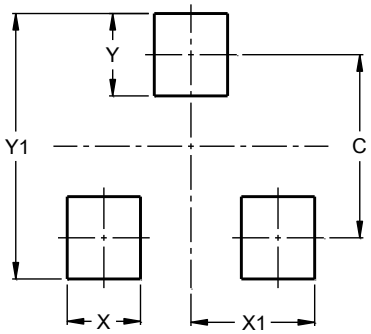
SOT23



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	–
All Dimensions in mm			

Suggested Pad Layout

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.