优尚

YOUSHANG SEMICONDUCTOR

# 设计研发新型功率器件

## 各类小信号开关

## 中低压及高压大电流等场效应管

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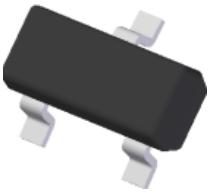
## Features

- $BV_{CEO}$ > 350V
- $I_C$ = 500mA High Collector Current
- 350mW Power Dissipation
- $h_{FE}$ of 15 @ $I_C$=100mA
- Complementary Part Number: NK-FMMT6520

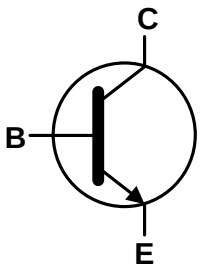
## Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (Approximate)

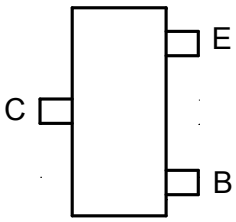
SOT23



Top View




Device Symbol




Top View
Pin-Out

## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Base Voltage | $V_{CBO}$ | 350 | V |
| Collector-Emitter Voltage | $V_{CEO}$ | 350 | V |
| Emitter-Base Voltage | $V_{EBO}$ | 7 | V |
| Base Current | $I_B$ | 25 | mA |
| Collector Current | $I_C$ | 500 | mA |

## Thermal Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

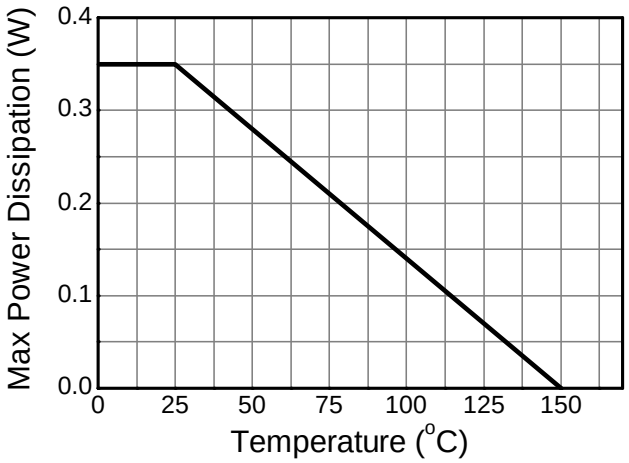
| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Dissipation | (Note 5) | $P_D$ | 310 | mW |
| | (Note 6) | | 350 | |
| Thermal Resistance, Junction to Ambient | (Note 5) | $R_{\theta JA}$ | 403 | °C/W |
| | (Note 6) | | 357 | |
| Thermal Resistance, Junction to Leads | (Note 7) | $R_{\theta JL}$ | 350 | °C/W |
| Operating and Storage Temperature Range | | $T_J$,$T_{STG}$ | -55 to +150 | °C |

## ESD Ratings (Note 8)

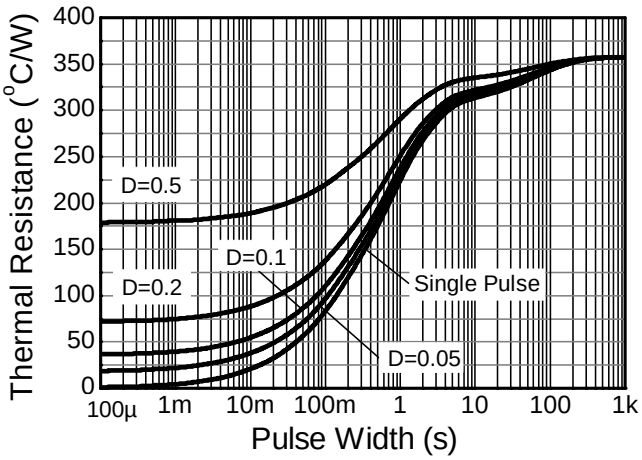
| Characteristic | Symbol | Value | Unit | JEDEC Class |
|---|---|---|---|---|
| Electrostatic Discharge - Human Body Model | ESD HBM | 4,000 | V | 3A |
| Electrostatic Discharge - Machine Model | ESD MM | 400 | V | C |

Notes:
5. For the device mounted on minimum recommended pad layout 1oz copper that is on a single-sided 1.6mm FR-4 PCB; device is measured under still air conditions whilst operating in steady state condition.
6. Same as note (5), except the device is mounted on 15mm x 15mm 1oz copper.
7. Thermal resistance from junction to solder-point (at the end of the leads).
8. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

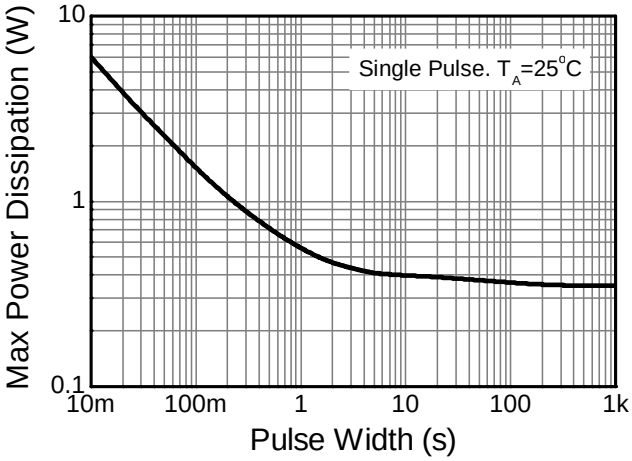
## Thermal Characteristics and Derating information




**Derating Curve**




**Transient Thermal Impedance**



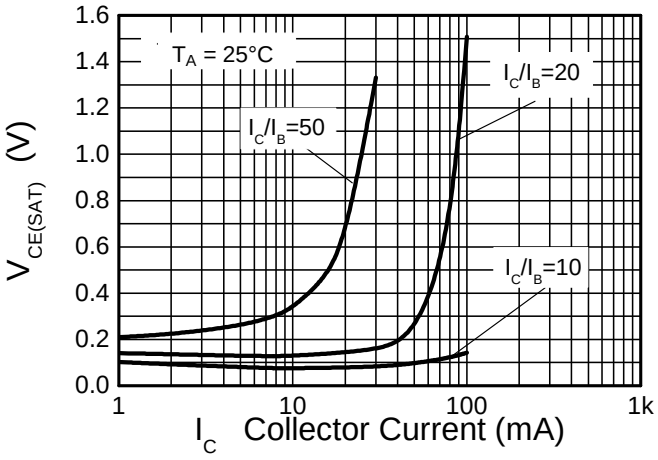

**Pulse Power Dissipation**

## Electrical Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

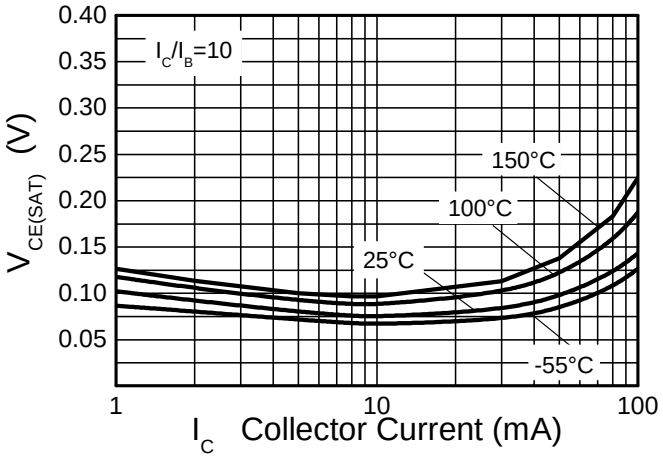
| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | 350 | — | — | V | $I_C$ = 100μA |
| Collector-Emitter Breakdown Voltage (Note 9) | $BV_{CEO}$ | 350 | — | — | V | $I_C$ = 1mA |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | 7 | — | — | V | $I_E$ = 100μA |
| Collector Cutoff Current | $I_{CBO}$ | — | — | 50 | nA | $V_{CB}$ = 250V |
| Emitter Cutoff Current | $I_{EBO}$ | — | — | 50 | nA | $V_{EB}$ = 6V |
| Static Forward Current Transfer Ratio (Note 9) | $h_{FE}$ | 20<br>30<br>30<br>20<br>15 | — | —<br>—<br>200<br>200<br>— | — | $I_C$ = 1mA, $V_{CE}$ = 10V<br>$I_C$ = 10mA, $V_{CE}$ = 10V<br>$I_C$ = 30mA, $V_{CE}$ = 10V<br>$I_C$ = 50mA, $V_{CE}$ = 10V<br>$I_C$ = 100mA, $V_{CE}$ = 10V |
| Collector-Emitter Saturation Voltage (Note 9) | $V_{CE(SAT)}$ | — | — | 0.3<br>0.35<br>0.5<br>1.0 | V | $I_C$ = 10mA, $I_B$ = 1mA<br>$I_C$ = 20mA, $I_B$ = 2mA<br>$I_C$ = 30mA, $I_B$ = 3mA<br>$I_C$ = 50mA, $I_B$ = 5mA |
| Base-Emitter Saturation Voltage (Note 9) | $V_{BE(SAT)}$ | — | — | 0.80<br>0.85<br>0.90 | V | $I_C$ = 10mA, $I_B$ = 1mA<br>$I_C$ = 20mA, $I_B$ = 2mA<br>$I_C$ = 30mA, $I_B$ = 3mA |
| Base-Emitter Turn-On Voltage (Note 9) | $V_{BE(ON)}$ | — | — | 2.0 | V | $I_C$ = 100mA, $V_{CE}$ = 10V |
| Output Capacitance | $C_{OBO}$ | — | — | 6 | pF | $V_{CB}$ = 20V. f = 1MHz |
| Transition Frequency | $f_T$ | 50 | — | — | MHz | $V_{CE}$ = 20V, $I_C$ = 10mA, f = 20MHz |

Note: 9. Measured under pulsed conditions. Pulse width ≤ 300μs. Duty cycle ≤ 2%.

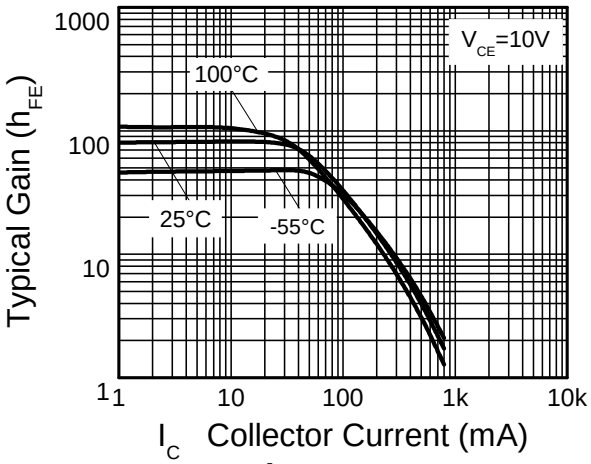
## Typical Electrical Characteristics (@$T_A$ = +25°C, unless otherwise specified.)



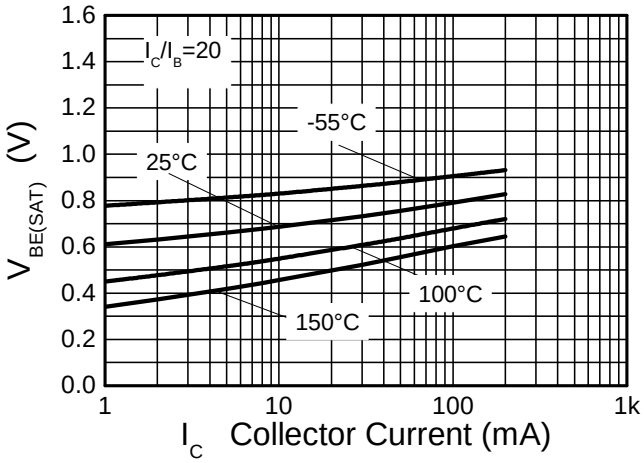

$V_{CE(SAT)}$ v $I_C$



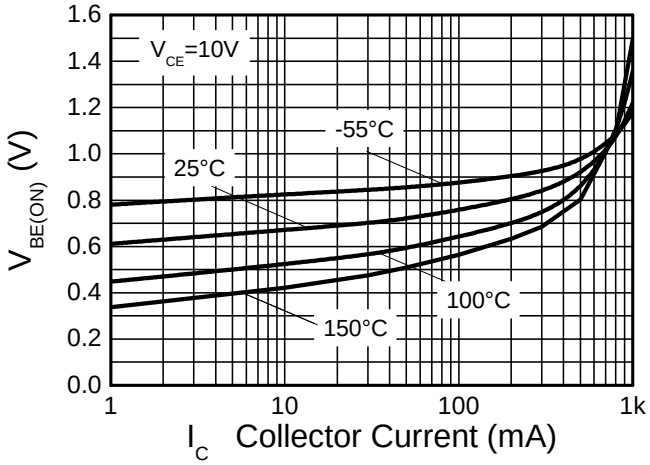

$V_{CE(SAT)}$ v $I_C$




$h_{FE}$ v $I_C$



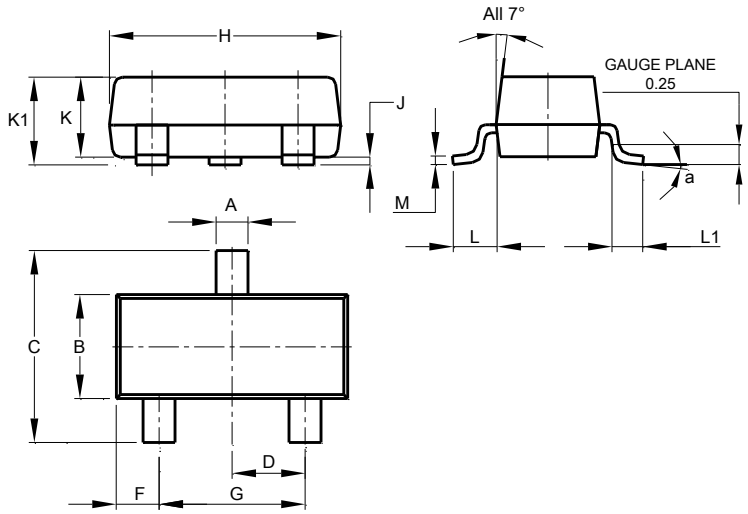

$V_{BE(SAT)}$ v $I_C$




$V_{BE(ON)}$ v $I_C$

## Package Outline Dimensions

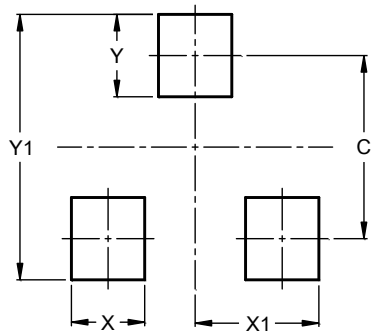
**SOT23**




| SOT23 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 0.37 | 0.51 | 0.40 |
| **B** | 1.20 | 1.40 | 1.30 |
| **C** | 2.30 | 2.50 | 2.40 |
| **D** | 0.89 | 1.03 | 0.915 |
| **F** | 0.45 | 0.60 | 0.535 |
| **G** | 1.78 | 2.05 | 1.83 |
| **H** | 2.80 | 3.00 | 2.90 |
| **J** | 0.013 | 0.10 | 0.05 |
| **K** | 0.890 | 1.00 | 0.975 |
| **K1** | 0.903 | 1.10 | 1.025 |
| **L** | 0.45 | 0.61 | 0.55 |
| **L1** | 0.25 | 0.55 | 0.40 |
| **M** | 0.085 | 0.150 | 0.110 |
| **a** | 0° | 8° | -- |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

**SOT23**




| Dimensions | Value (in mm) |
|---|---|
| **C** | 2.0 |
| **X** | 0.8 |
| **X1** | 1.35 |
| **Y** | 0.9 |
| **Y1** | 2.9 |

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.