优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

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Features

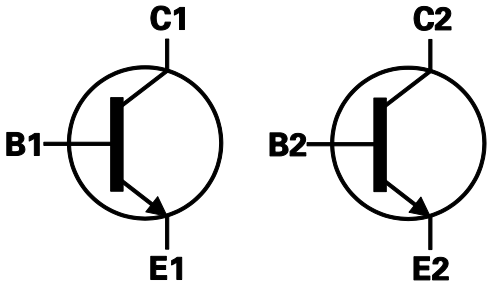
- Epitaxial Planar Die Construction
- Complementary PNP Type – NK-MMDT5401
- Ideal for Medium Power Amplification and Switching
- Ultra-Small Surface-Mount Package

Mechanical Data

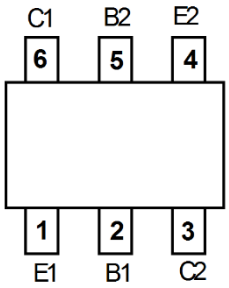
- Package: SOT363
- Package Material: Molded Plastic, “Green” Molding Compound, UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Finish. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.006 grams (Approximate)

SOT363

Top View



Device Symbol



Top View
Pin-Out

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	180	V
Collector-Emitter Voltage	V_{CEO}	160	V
Emitter-Base Voltage	V_{EBO}	6	V
Continuous Collector Current	I_C	200	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	200	mW
	(Notes 6 & 7)		320	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	625	°C/W
	(Notes 6 & 7)		390	
Thermal Resistance, Junction to Case	(Note 8)	$R_{\theta JC}$	140	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes:
5. For a device mounted on minimum recommended pad layout 1oz weight copper that is on a single-sided FR4 PCB; device is measured under still air conditions whilst operating in a steady state.
6. Same as Note 5, except the device is mounted 25mm × 25mm 2oz copper.
7. Maximum combined dissipation.
8. Thermal resistance from junction to the top of package.

Thermal Characteristics and Derating Information

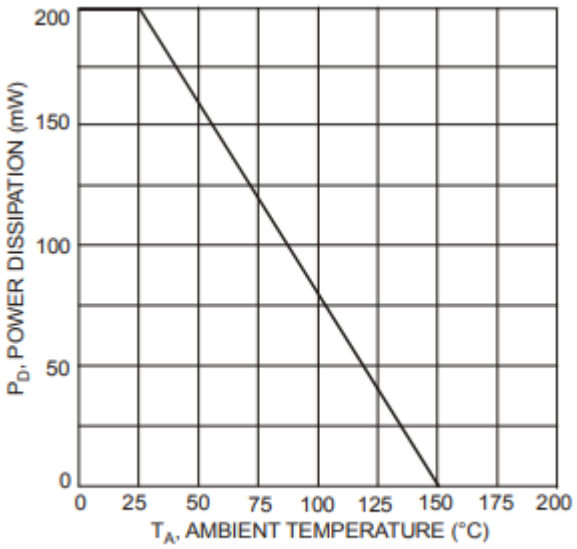


Figure 1. Max Power Dissipation vs. Ambient Temperature

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage	BV_{CBO}	180	—	—	V	I_C = 100μA, I_E = 0
Collector-Emitter Breakdown Voltage (Note 9)	BV_{CEO}	160	—	—	V	I_C = 1mA, I_B = 0
Emitter-Base Breakdown Voltage	BV_{EBO}	6	—	—	V	I_E = 10μA, I_C = 0
Collector-Base Cutoff Current	I_{CBO}	—	—	50	nA	V_{CB} = 120V, I_E = 0
		—	—	50	μA	V_{CB} = 120V, I_E = 0, T_A = +100°C
Base-Emitter Cutoff Current	I_{EBO}	—	—	50	nA	V_{EB} = 4V, I_C = 0
ON CHARACTERISTICS (Note 9)						
DC Current Gain	h_{FE}	80	—	—	—	I_C = 1mA, V_{CE} = 5.0V
		80		250		I_C = 10mA, V_{CE} = 5.0V
		30		—		I_C = 50mA, V_{CE} = 5.0V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	0.15	V	I_C = 10mA, I_B = 1.0mA
				0.20		I_C = 50mA, I_B = 5.0mA
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	—	—	1.0	V	I_C = 10mA, I_B = 1.0mA
						I_C = 50mA, I_B = 5.0mA
SMALL SIGNAL CHARACTERISTICS						
Output Capacitance	C_{obo}	—	—	6.0	pF	V_{CB} = 10V, f = 1.0MHz, I_E = 0
Small Signal Current Gain	h_{fe}	50	—	250	—	I_C = 1mA, V_{CE} = 10V, f = 1.0MHz
Current Gain-Bandwidth Product	f_T	100	—	300	MHz	I_C = 10mA, V_{CE} = 10V, f = 100MHz
Noise Figure	NF	—	—	8.0	dB	V_{CE} = 5.0V, I_C = 200μA, R_S = 1kΩ, f = 1.0kHz

Note: 9. Measured under pulsed conditions. Pulse width ≤ 300μs. Duty cycle ≤ 2%.

Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

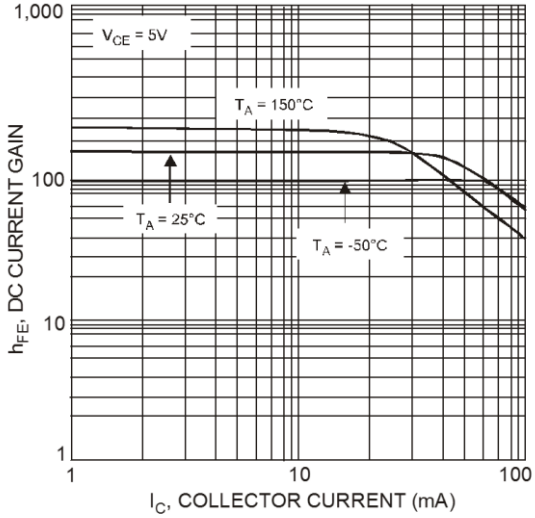


Figure 2. DC Current Gain vs. Collector Current

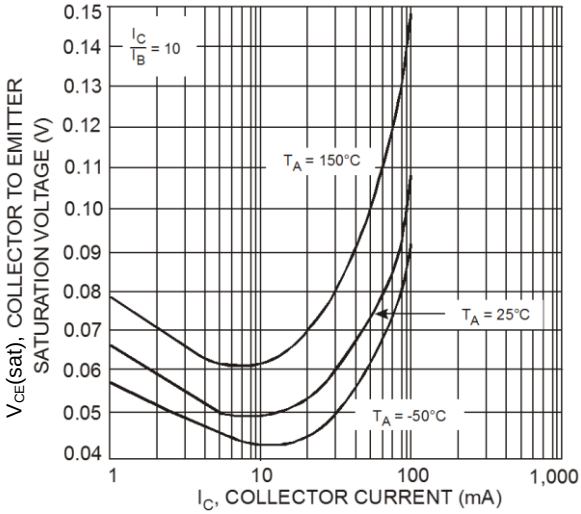


Figure 3. Collector Emitter Saturation Voltage vs. Collector Current

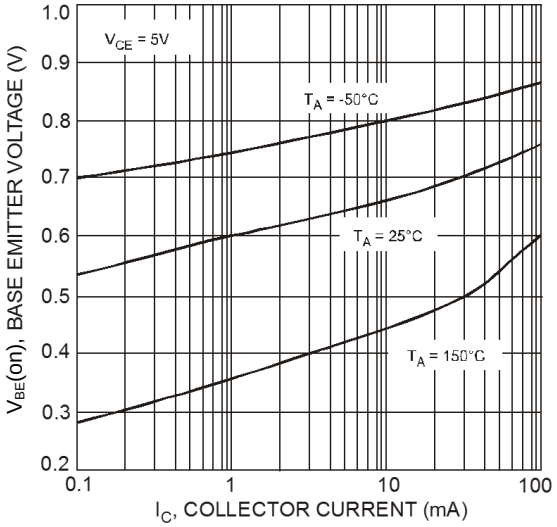


Figure 4. Base Emitter Voltage vs. Collector Current

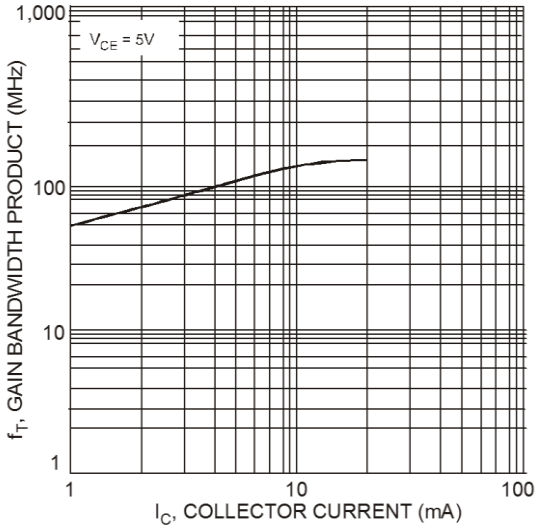
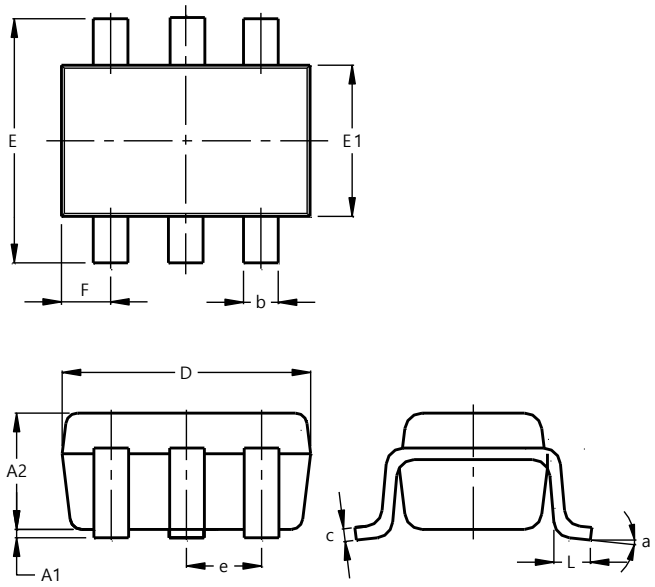


Figure 5. Gain Bandwidth Product vs. Collector Current

Package Outline Dimensions

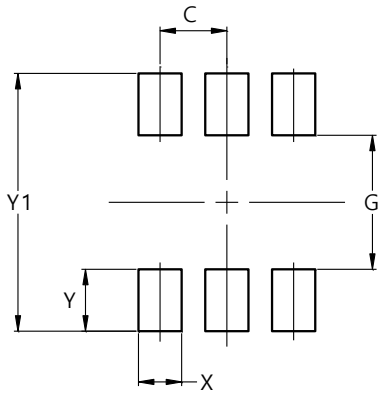
SOT363



SOT363			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT363



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.