优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Features

- BV_{CEO} > 120V
- BV_{CBO} > 140V
- I_C = 1.5A High Continuous current
- hFE > 2k for High Gain @ 1A

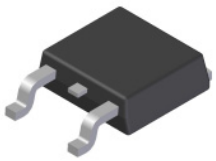
Mechanical Data

- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.34 grams (approximate)

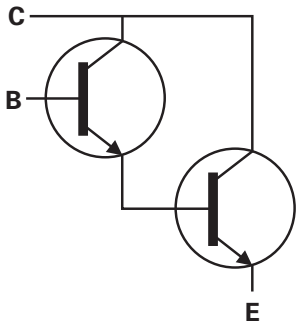
Applications

- DC Fans
- Regulator Transistors
- Relays
- Solenoid Driving

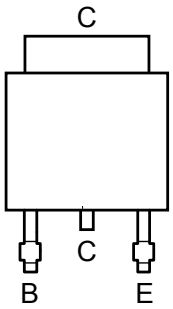
TO252 (DPAK)



Top View



Equivalent Circuit



Top View
Pin-Out

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	140	V
Collector-Emitter Voltage	V_{CEO}	120	V
Emitter-Base Voltage	V_{EBO}	14	V
Continuous Collector Current	I_C	1.5	A
Peak Pulse Current	I_{CM}	4	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

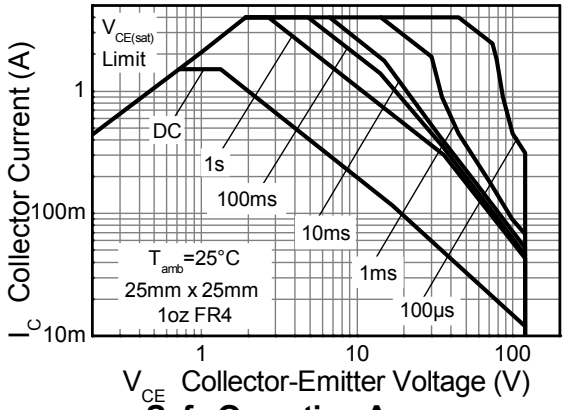
Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	3.9	W
	(Note 6)		2	
	(Note 7)		1.5	
Thermal Resistance, Junction to Ambient Air	(Note 5)	$R_{\theta JA}$	32	°C/W
	(Note 6)		62.5	
	(Note 7)		80	
Thermal Resistance, Junction to Leads	(Note 8)	$R_{\theta JL}$	9	
Thermal Resistance, Junction to Case	(Note 9)	$R_{\theta JC}$	11	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

ESD Ratings (Note 10)

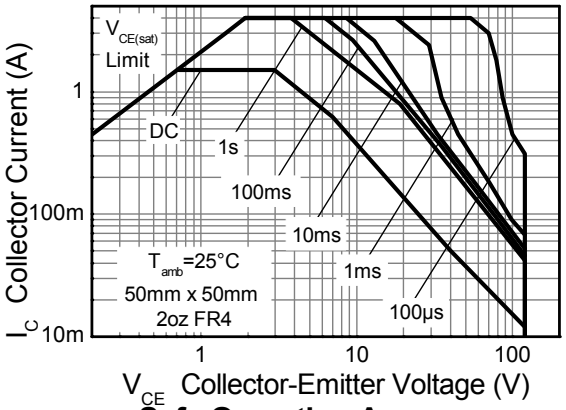
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	400	V	C

Notes:
5. For a device mounted with the exposed collector pad on 50mm x 50mm 2oz copper that is on a single-sided 1.6mm FR4 PCB; device is measured under still air conditions whilst operating in a steady-state.
6. Same as note (5), except mounted on 25mm x 25mm 1oz copper.
7. Same as note (5), except mounted on minimum recommended pad (MRP) layout.
8. Thermal resistance from junction to solder-point (on the exposed collector pad).
9. Thermal resistance from junction to the top of the case.
10. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

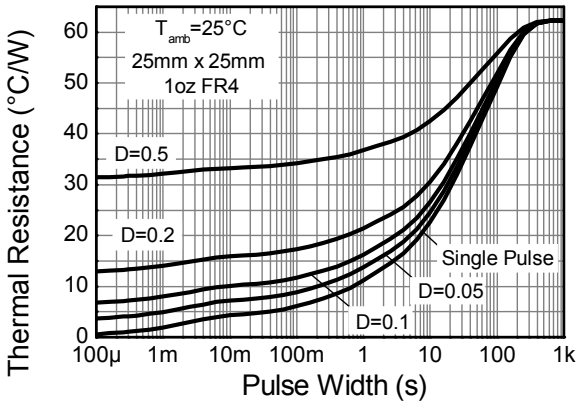
Thermal Characteristics and Derating Information



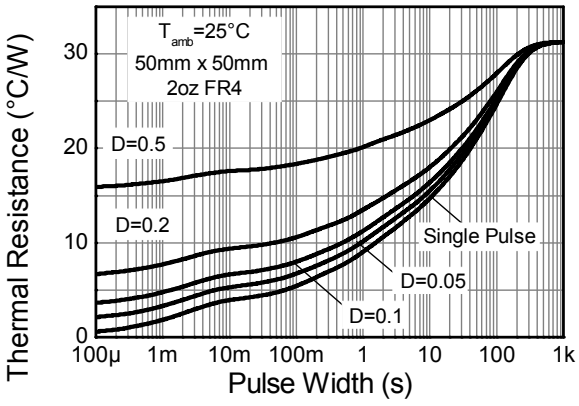
Safe Operating Area



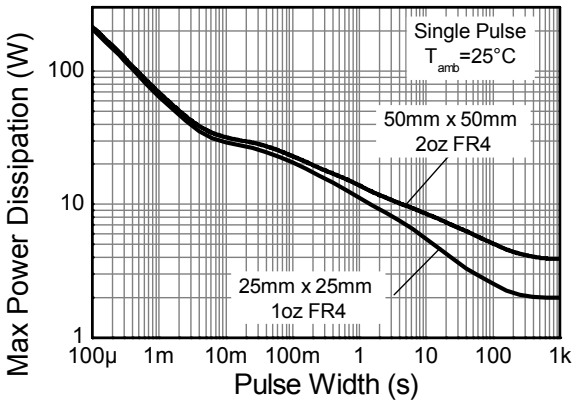
Safe Operating Area



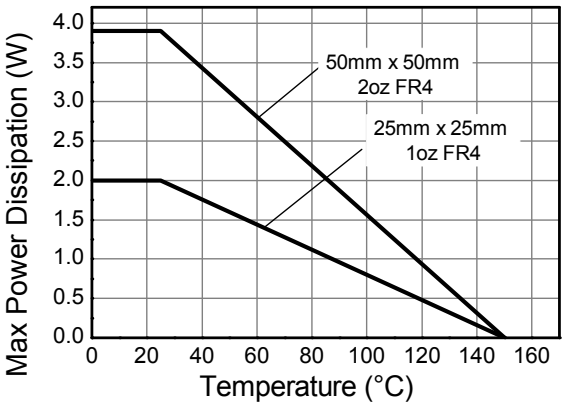
Transient Thermal Impedance



Transient Thermal Impedance



Pulse Power Dissipation



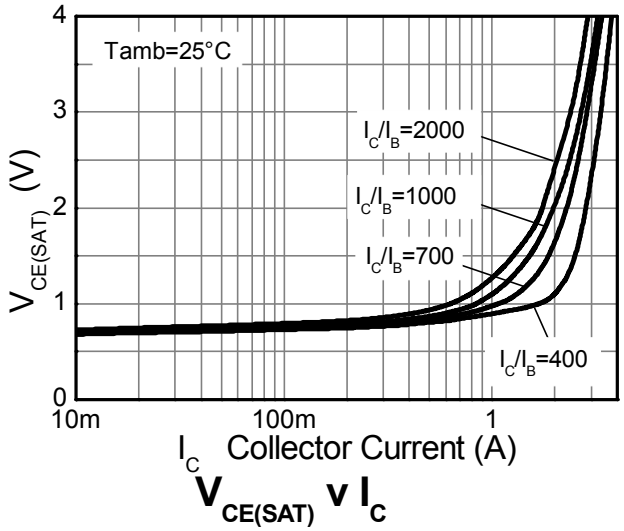
Derating Curve

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

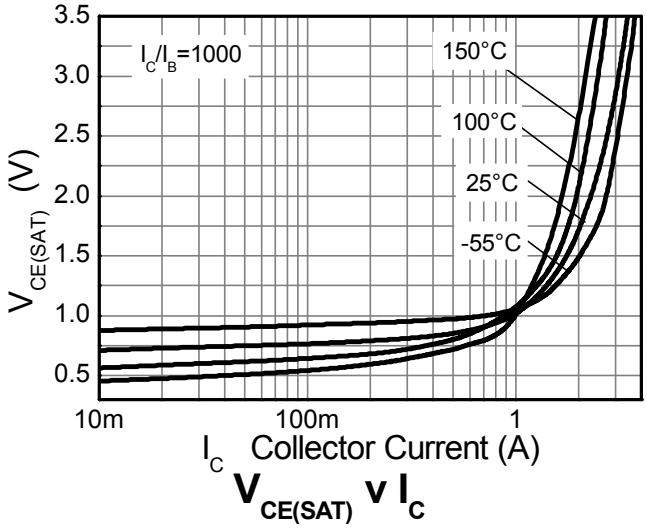
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV_{CBO}	140	—	—	V	I_C = 100μA
Collector-Emitter Breakdown Voltage (Note 11)	BV_{CEO}	120	—	—	V	I_C = 10mA
Emitter-Base Breakdown Voltage	BV_{EBO}	14	—	—	V	I_E = 100μA
Collector-Base Cutoff Current	I_{CBO}	—	—	100 10	nA μA	V_{CB} = 120V V_{CB} = 120V, T_A = +120°C
Collector-Emitter Cutoff Current	I_{CES}	—	—	100	nA	V_{CE} = 120V
Emitter Cutoff Current	I_{EBO}	—	—	100	nA	V_{EB} = 8V
DC Current Gain (Note 11)	h_{FE}	2,000 5,000 2,000 500	— — — —	— — 100,000 —	—	I_C = 50mA, V_{CE} = 5V I_C = 500mA, V_{CE} = 5V I_C = 1A, V_{CE} = 5V I_C = 2A, V_{CE} = 5V
Collector-Emitter Saturation Voltage (Note 11)	$V_{CE(sat)}$	— —	— —	1 1.5	V	I_C = 250mA, I_B = 0.25mA I_C = 1A, I_B = 1mA
Base-Emitter Saturation Voltage (Note 11)	$V_{BE(sat)}$	—	—	1.8	V	I_C = 1A, I_B = 1mA
Base-Emitter Turn-On Voltage (Note 11)	$V_{BE(on)}$	—	—	1.7	V	I_C = 1A, V_{CE} = 5V
Input Capacitance (Note 11)	C_{ibo}	—	90	—	pF	V_{EB} = 0.5V, f = 1MHz
Output Capacitance (Note 11)	C_{obo}	—	15	—	pF	V_{CB} = 10V, f = 1MHz
Current Gain-Bandwidth Product (Note 11)	f_T	150	—	—	MHz	V_{CE} = 10V, I_C = 100mA, f=20MHz
Turn-On Time	t_{on}	—	0.5	—	μs	V_{CC} = 10V, I_C = 500mA
Turn-Off Time	t_{off}	—	1.6	—	μs	I_{B1} = -I_{B2} = 0.5mA

Note: 11. Measured under pulsed conditions. Pulse width ≤ 300 μs. Duty cycle ≤ 2%.

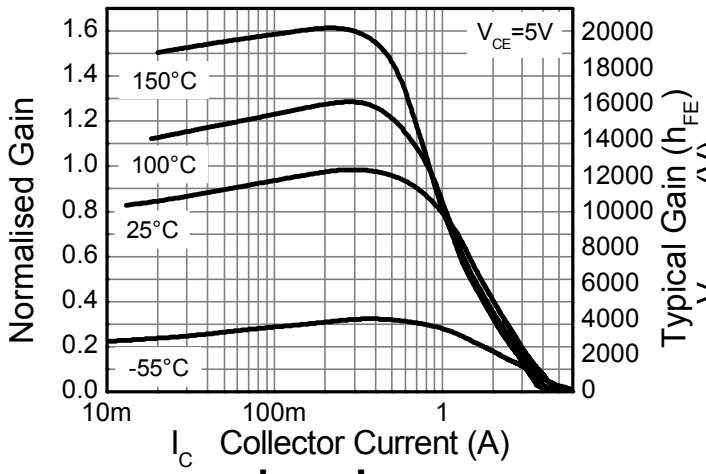
Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



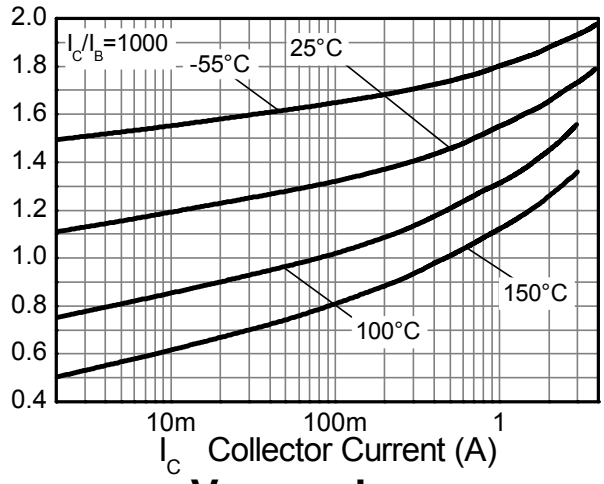
$V_{CE(SAT)}$ v I_C



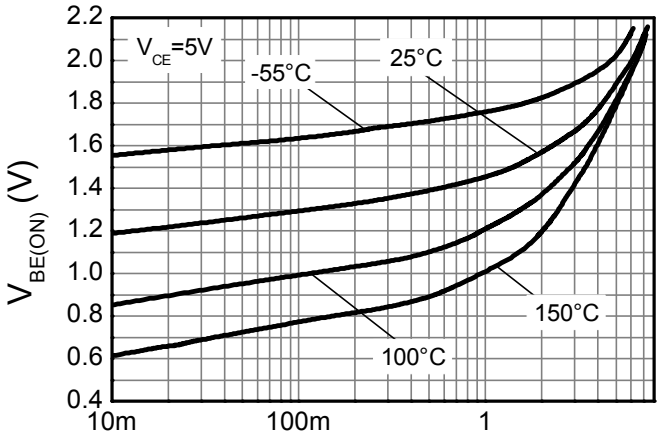
$V_{CE(SAT)}$ v I_C



h_{FE} v I_C

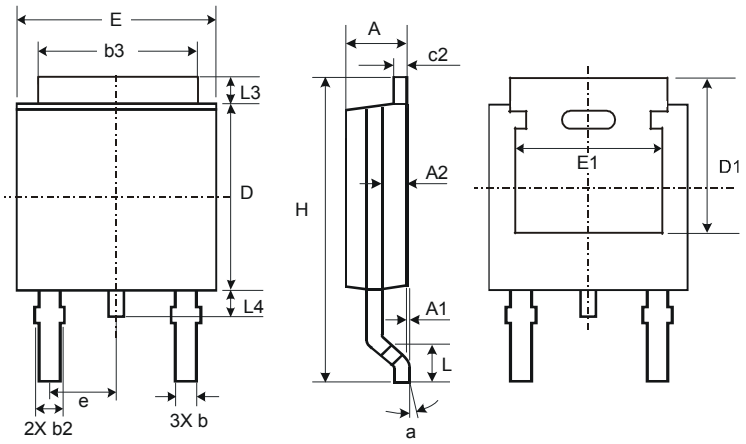


$V_{BE(SAT)}$ v I_C



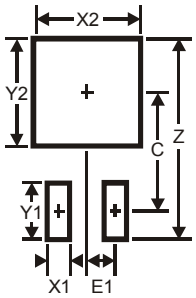
$V_{BE(ON)}$ v I_C

Package Outline Dimensions



TO252			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	–	–
e	–	–	2.286
E	6.45	6.70	6.58
E1	4.32	–	–
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	–
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

Note: 12. For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.