优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Description

The NK-AP2132A is a positive voltage regulator IC fabricated by CMOS process. The IC consists of a voltage reference, an error amplifier, a power transistor, a resistor network for setting output voltage, a current-limit circuit for current protection, and a chip-enable circuit.
The NK-AP2132A has features of large current, low-dropout voltage , high output-voltage accuracy and low input voltage. The NK-AP2132A provides a power-good (PG) signal to indicate if the voltage level of V_{OUT} reaches 92% of its rating value. And it operates with a V_{IN} as low as 1.4V and V_{CTRL} voltage 5V with output voltage programmable as low as 0.6V.

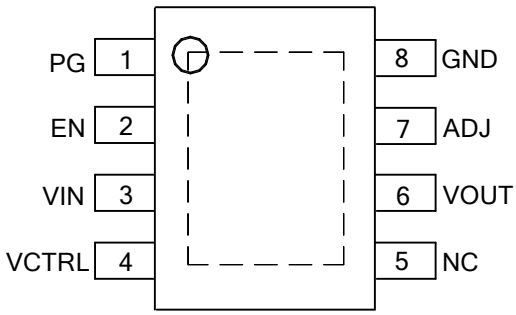
The NK-AP2132A is available in 1.8V fixed output voltage version and adjustable output voltage version. The fixed version integrates the adjust resistors. It is also available in an adjustable version, which can set the output voltage with external resistor. If the pin of adjustable output voltage is to ground, it will switch to fixed output voltage.
The NK-AP2132A is available in the PSOP-8 package.

Features

- Adjustable Output: 0.6V to 3.0V
- Low-Dropout Voltage: 300mV at I_{OUT} = 2A, V_{OUT} = 1.2V
- Overcurrent and Overtemperature Protection
- Enable Pin
- PSOP-8 Package with Thermal Pad
- Maximum Output Current: 3A (Peak)
- High Output-Voltage Accuracy: 2%
- V_{OUT} Power-Good Signal
- Excellent Line/Load Regulation

Pin Assignments

(Top View)

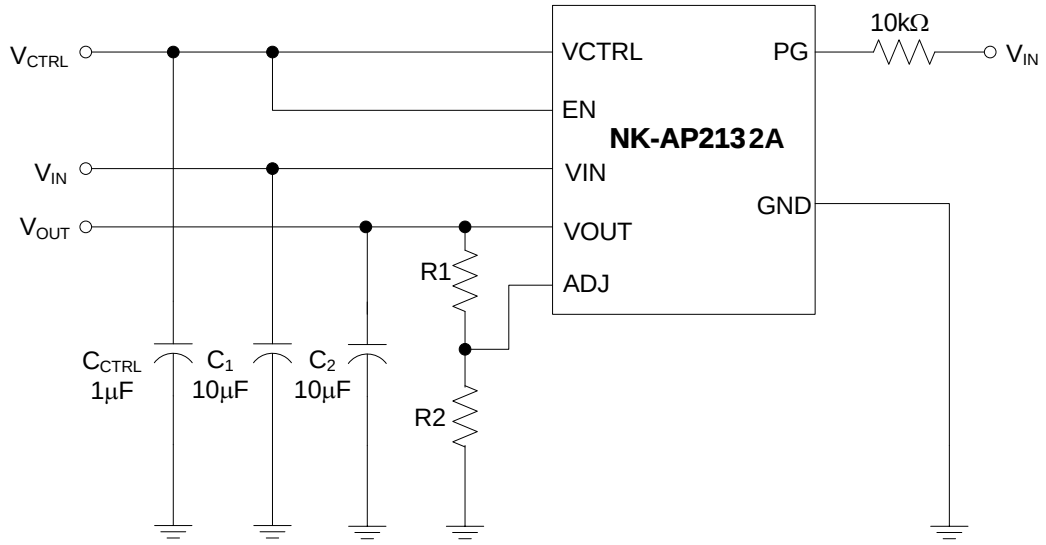


PSOP-8

Applications

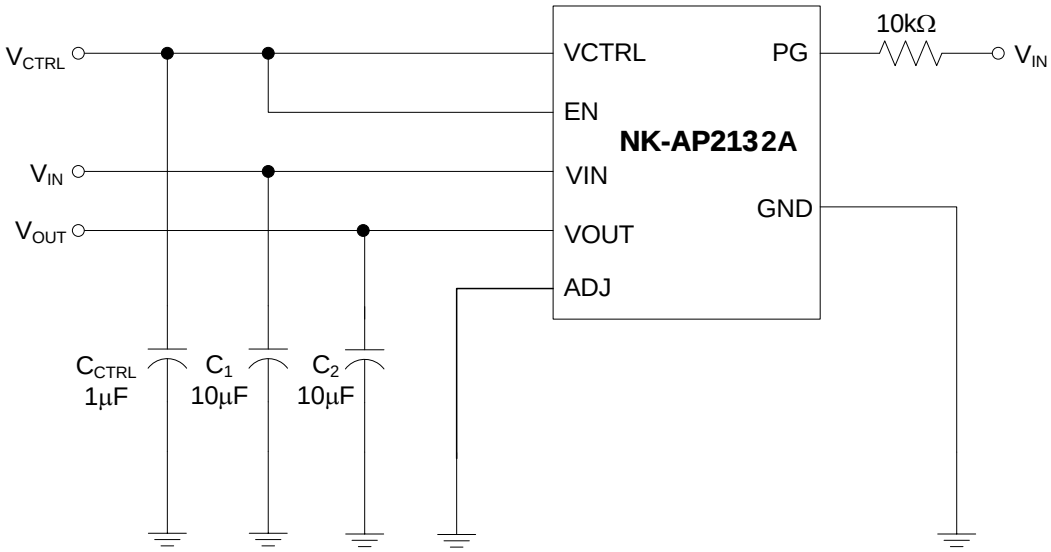
- Notebooks

Typical Applications Circuit



$$V_{OUT}=\frac{0.6(R1+R2)}{R2}\ (V)$$

Adjustable Version

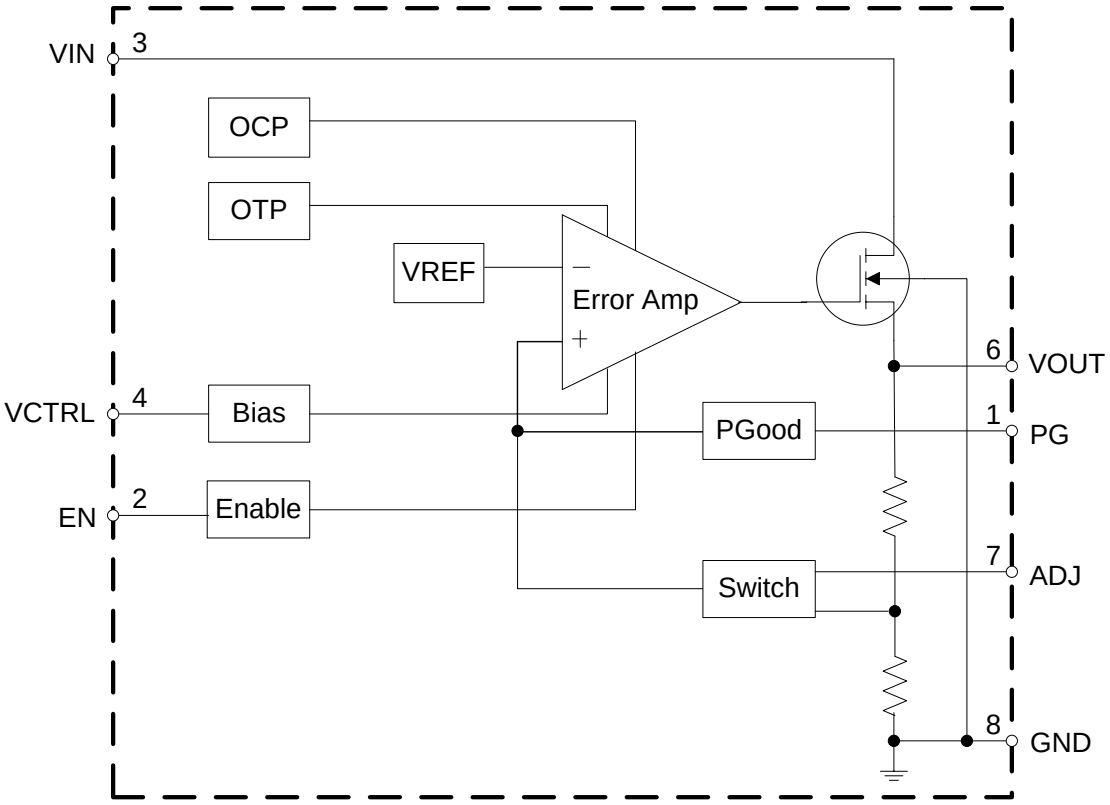


Fixed Version

Pin Descriptions

Pin Number	Pin Name	Function
1	PG	Assert high once V_{OUT} reaches 92% of its rating voltage
2	EN	Enable input
3	VIN	Input voltage
4	VCTRL	Input voltage for controlling circuit
5	NC	Not connected
6	VOUT	Regulated output voltage
7	ADJ	Adjust output: when connected to ground, the output voltage is set by internal resistors; when external feedback resistors are connected, the output voltage will be V_{OUT} = 0.6V×(R1+R2)/R2.
8	GND	Ground

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN} V_{CTRL}	Input Voltage Input Voltage for Controlling Circuit	6.0	V
V_{EN}	Enable Input Voltage	-0.3 to 6.0	V
θ_{JA}	Thermal Resistance (No Heatsink)	130	°C/W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
—	ESD (Machine Model)	200	V
—	ESD (Human Body Model)	2000	V

Note 4: Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.4	5.5	V
V_{CTRL}	Input Voltage for Controlling Circuit	4.5	5.5	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

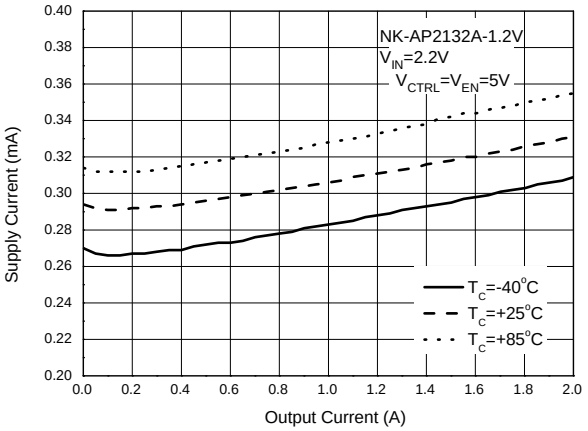
Electrical Characteristics

(@V_{IN} = V_{OUT}+0.5V, V_{CTRL} = V_{EN} = 5V, T_A = +25°C, C_{IN} = C_{OUT} = 10µF, C_{CTRL} = 1µF, I_{OUT} = 10mA, Bold typeface applies over -40°C ≤ T_A ≤ +85°C, unless otherwise specified.)

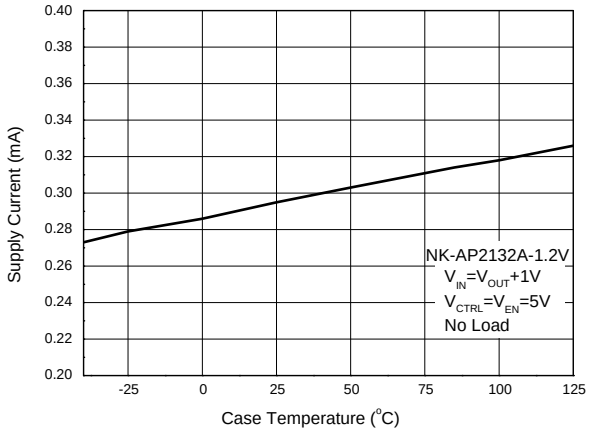
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = V_{OUT}+0.5V, I_{OUT} = 10mA	V_{OUT} × 98%	—	V_{OUT} × 102%	V
V_{IN}	Input Voltage	—	1.4	—	5.5	V
I_{LIMIT}	Current Limit	V_{IN}–V_{OUT} = 1V	3	—	—	A
V_{RLOAD}	Load Regulation	V_{IN} = V_{OUT}+0.5V, 10mA ≤ I_{OUT} ≤ 2A	—	10	—	mV
V_{RLINE}	Line Regulation	V_{OUT}+0.5V ≤ V_{IN} ≤ 5V, I_{OUT} = 10mA	—	2	—	mV
V_{DROP}	Dropout Voltage	I_{OUT} = 500mA	—	80	120	mV
		I_{OUT} = 1A	—	150	200	mV
		I_{OUT} = 2A	—	300	450	mV
I_{SUPPLY}	Supply Current	V_{IN} = V_{OUT}+0.5V, I_{OUT} = 0	—	300	—	µA
I_{CTRLH}	V_{CTRL} Current	V_{IN} = V_{OUT}+0.5V, V_{CTRL} = V_{EN} = 5V	—	250	500	µA
I_{CTRLL}		V_{IN} = V_{OUT}+0.5V, V_{CTRL} = 5V, V_{EN} = 0	—	0.1	1.0	µA
PSRR	Power-Supply Rejection Ratio	Ripple 0.5Vp-p, V_{IN} = V_{OUT}+1V, f = 100Hz	—	60	—	dB
		Ripple 0.5Vp-p, V_{IN} = V_{OUT}+1V, f = 1kHz	—	60	—	dB
$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T}$	Output Voltage Temperature Coefficient	I_{OUT} = 10mA, -40°C ≤ T_A ≤ +85°C	—	±100	—	ppm/°C
V_{REF}	Reference Voltage	Adjust Short to V_{OUT}	0.588	0.6	0.612	V
—	Enable “High” Voltage	Enable Input Voltage “High”	1.5	—	—	V
—	Enable “Low” Voltage	Enable Input Voltage “Low”	—	—	0.4	V
OTSD	Thermal Shutdown	—	—	+165	—	°C
—	Thermal Shutdown Hysteresis	—	—	+20	—	°C
V_{THPG}	V_{OUT} Power-Good Voltage	—	—	92	—	%
—	V_{PG} Hysteresis	—	—	7	—	%
—	Adjust Pin Threshold	—	—	200	—	mV
θ_{JC}	Thermal Resistance (Junction to Case)	PSOP-8	—	40	—	°C/W

Performance Characteristics

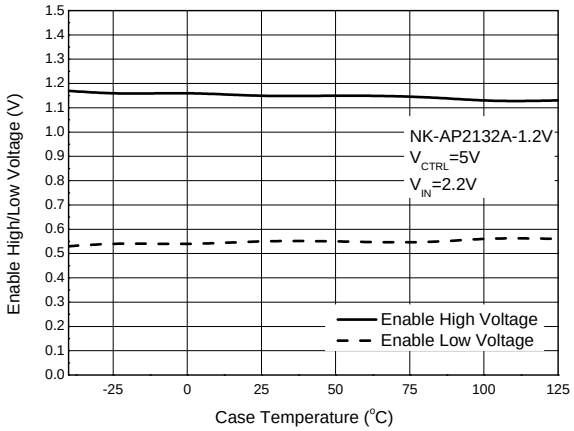
Supply Current vs. Output Current



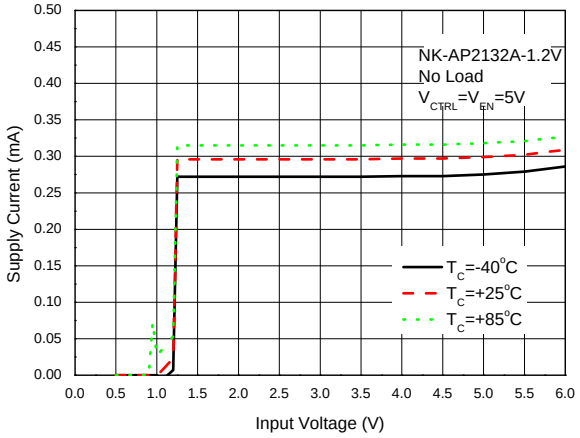
Supply Current vs. Case Temperature



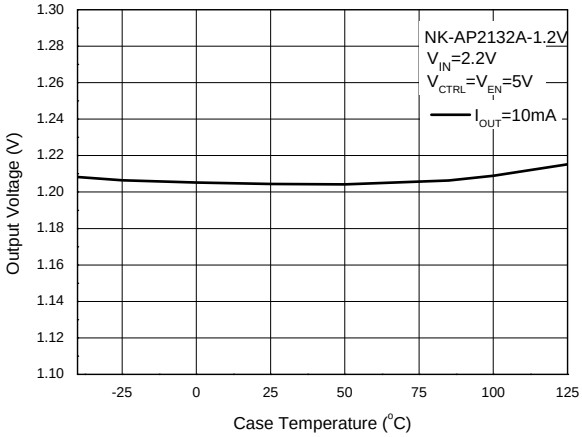
Enable High/Low Voltage vs. Case Temperature



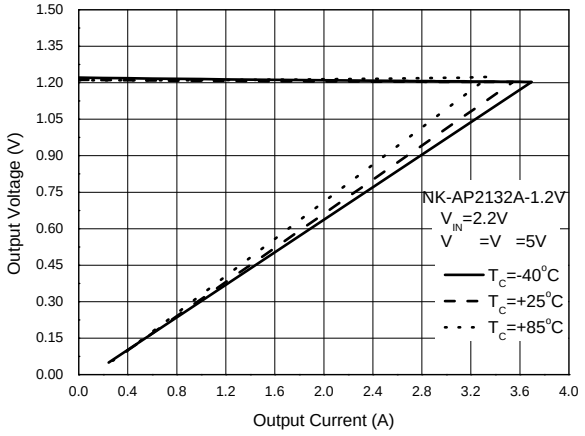
Supply Current vs. Input Voltage



Output Voltage vs. Case Temperature

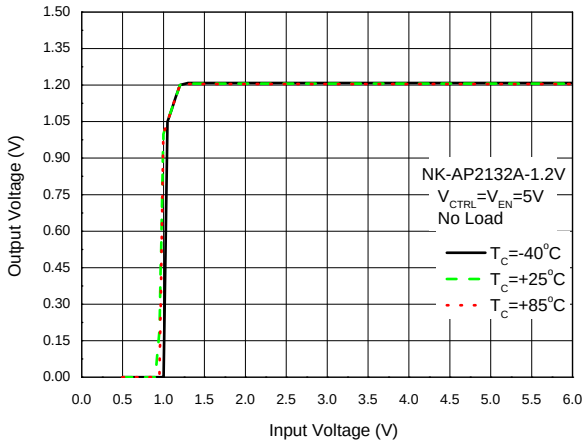


Output Voltage vs. Output Current

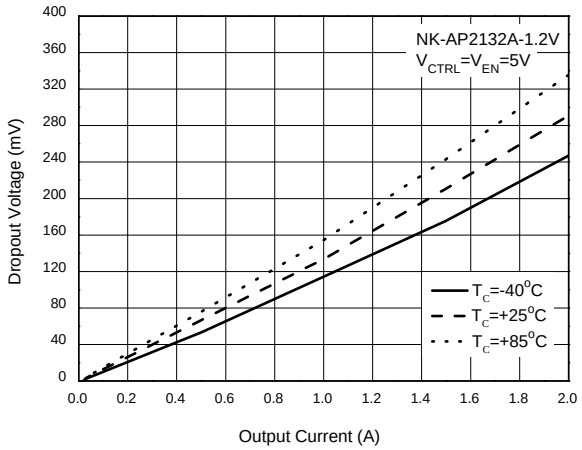


Performance Characteristics (continued)

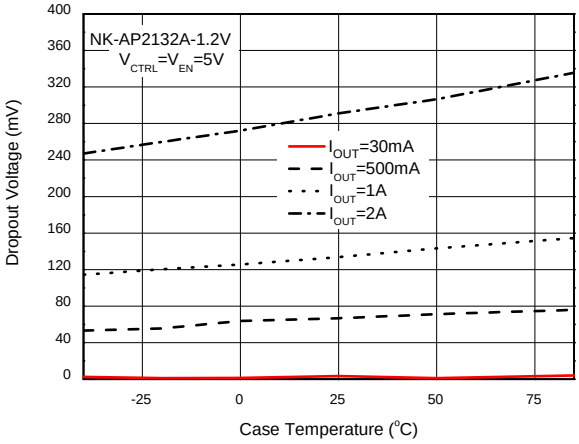
Output Voltage vs. Input Voltage



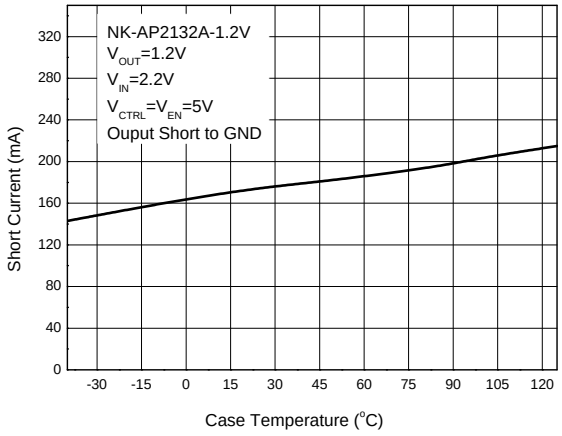
Dropout Voltage vs. Output Current



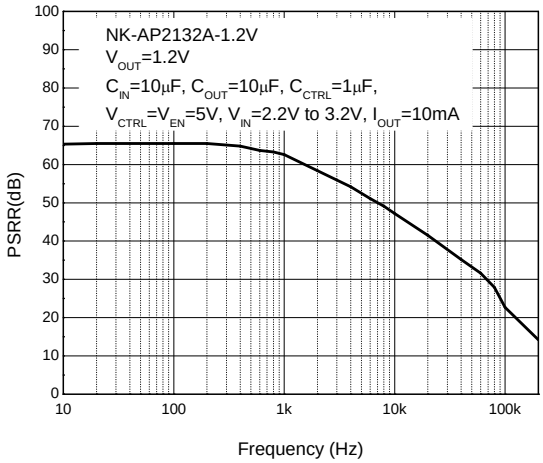
Dropout Voltage vs. Case Temperature



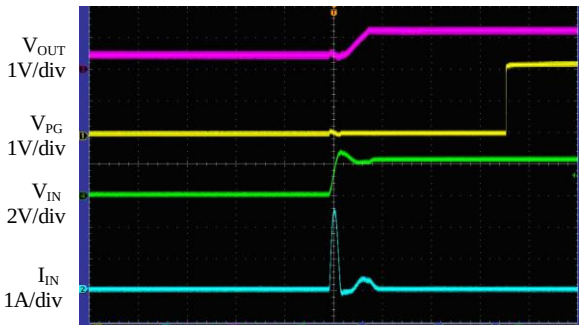
Short Current vs. Case Temperature



PSRR vs. Frequency



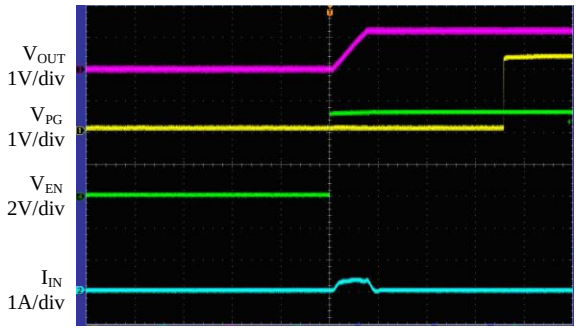
V_{IN} Startup Waveform (V_{CTRL}=V_{EN}=5V, V_{IN}=0 to 2.2V, No Load)



Time 80μs/div

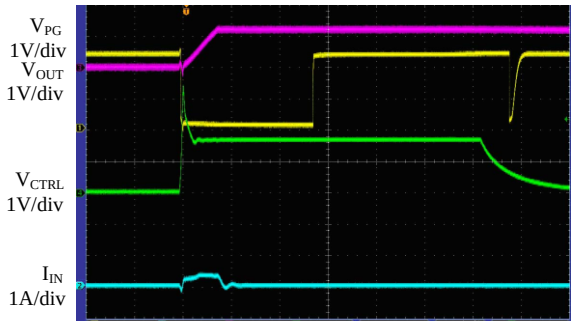
Performance Characteristics (continued)

V_{EN} Startup Waveform
(V_{CTRL}=5V, V_{EN}=0 to 5V, V_{IN}=2.2V, No Load)



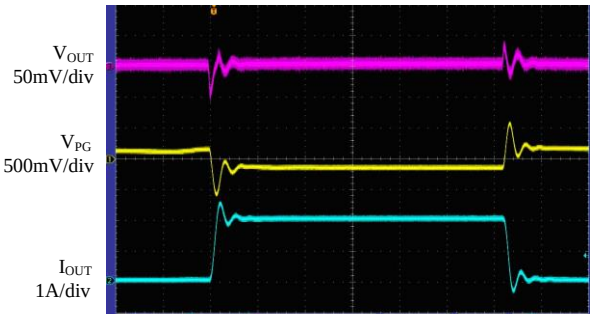
Time 80μs/div

V_{CTRL} Startup and Shutdown Waveform
(V_{CTRL}=0 to 5V, V_{EN}=5V, V_{IN}=2.2V, No Load)



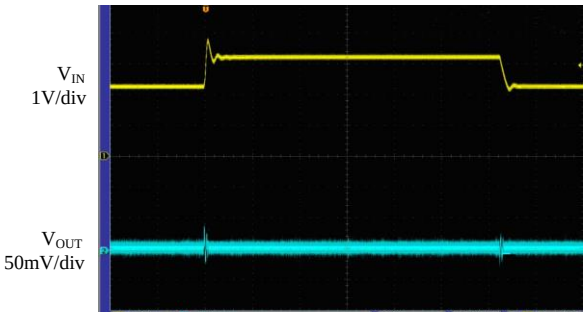
Time 80μs/div

Load Transient
(V_{CTRL}=V_{EN}=5V, V_{IN}=2.2V, I_{OUT}=0 to 2A)



Time 80μs/div

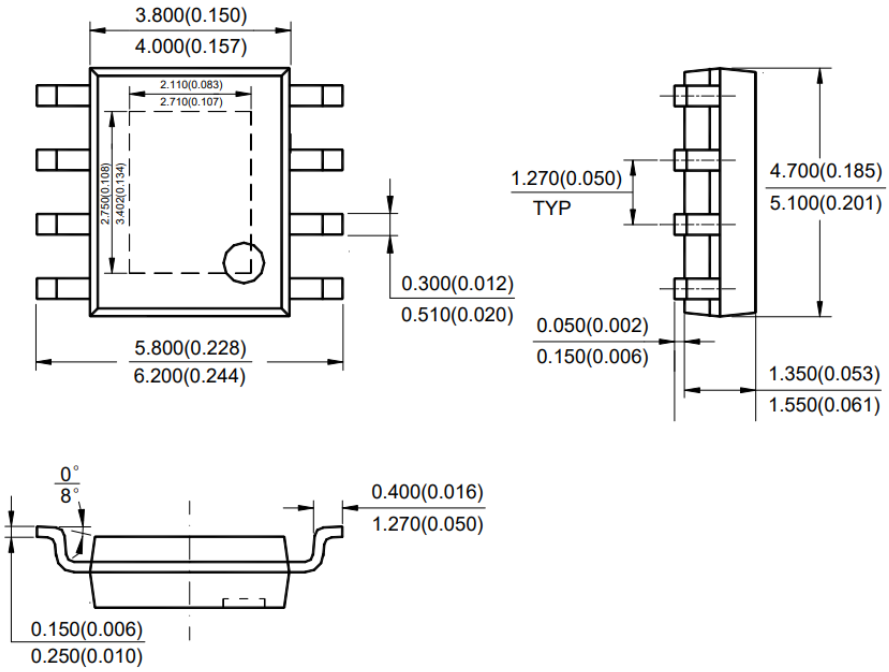
Line Transient
(V_{CTRL}=V_{EN}=5V, C_{IN}=C_{CTRL}=1μF, C_{OUT}=10μF, V_{IN}=2.2V to 3.2V, I_{OUT}=10mA)



Time 80μs/div

Package Outline Dimensions (All dimensions in mm(inch).)

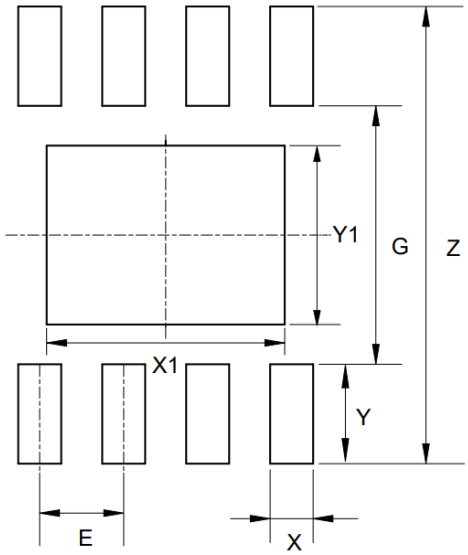
PSOP-8



Note: Eject hole, oriented hole and mold mark is optional.

Suggested Pad Layout

PSOP-8



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	3.600/0.142	2.700/0.106	1.270/0.050