



YOUSHANG SEMICONDUCTOR

**设计研发新型功率器件**

**各类小信号开关**

**中低压及高压大电流等场效应管**

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## Description

The NK-AP7361E is a 1A, adjustable and fixed output voltage, ultra-low dropout linear regulator with enable function. The device includes

pass element, error amplifier, band-gap reference, current limit, and thermal shutdown circuitry. The device is turned on when the EN pin is set to logic high level.

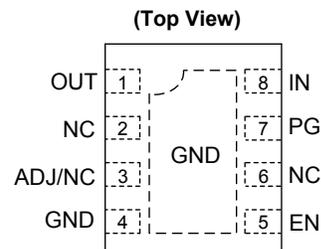
The device's low dropout voltage and low quiescent current make it suitable for low to medium power applications, such as laptop computers, audio and video applications, and battery powered devices. The typical quiescent current is approximately 60 $\mu$ A. Built-in current-limit, thermal-shutdown and power good functions prevent IC from damage in fault conditions.

The NK-AP7361E is available in the U-DFN3030-8 (Type E) package.

## Features

- Wide Input Voltage Range: 2.2V to 6.0V
- Output Voltage Accuracy:  $\pm 1\%$
- Very Low Dropout Voltage (3.3V): 360mV at 1A Typical
- Low Quiescent Current ( $I_Q$ ): 60 $\mu$ A Typical
- Adjustable Output Voltage Range: 0.8V to 5.0V
- Fixed Output Options: 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V and 3.3V
- High PSRR: 75dB @ 1kHz
- Current Limit: 1.5A
- Fold-Back Short Circuit Protection: 400mA
- Power-Good (PG) Output for Supply Monitoring and for Sequencing of Other Supplies
- Thermal Shutdown Protection
- Stable with MLCC, E-Cap, Tan-Cap or Solid Capacitor  $\geq 2.2\mu$ F
- Ambient Temperature Range: -40°C to +85°C

## Pin Assignments

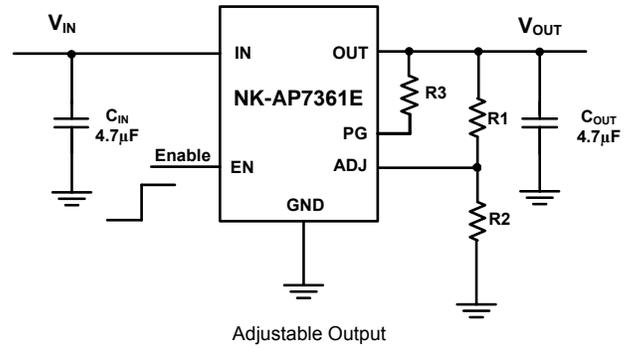
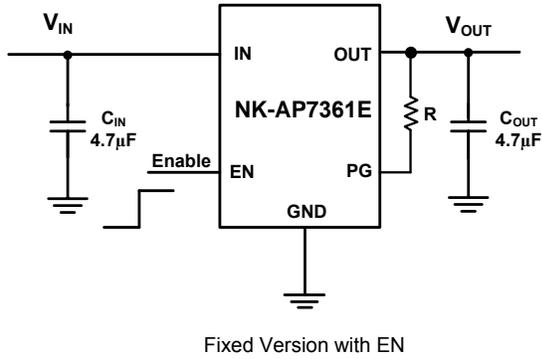


**U-DFN3030-8 (Type E)**

## Applications

- LCD-TVs and Monitors
- Set-Top-Boxes
- Home Electrical Appliances

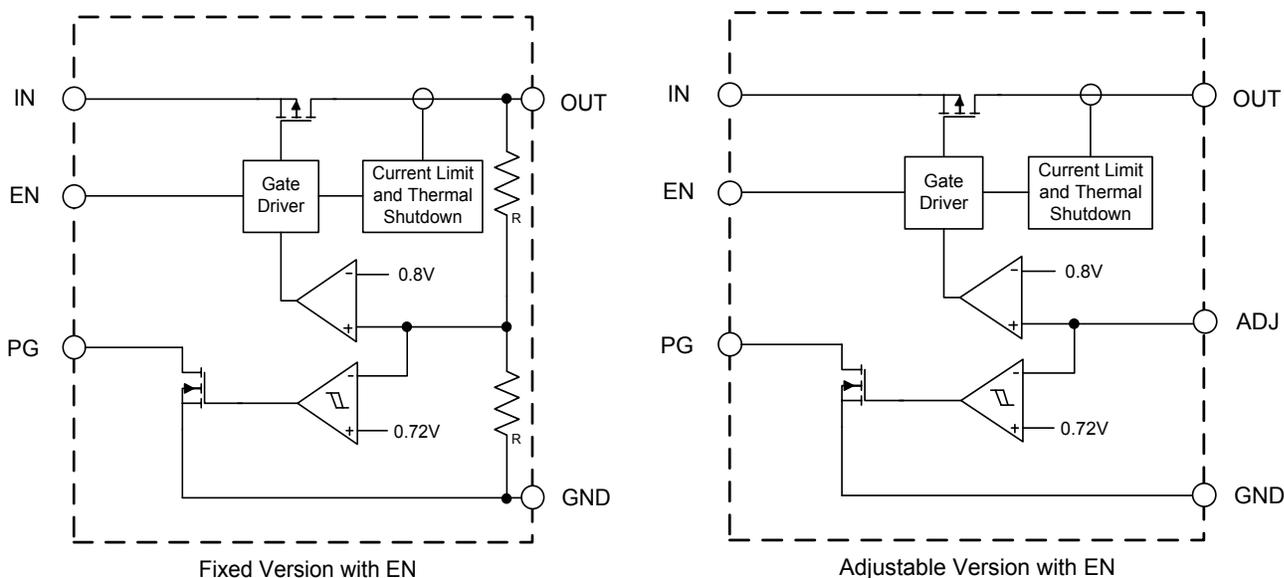
### Typical Applications Circuit



### Pin Descriptions

Pin Number	Pin Name	Function
<b>U-DFN3030-8 (Type E)</b>		
1	OUT	The output of the regulator. Bypass to ground through at least 2.2µF ceramic capacitor. For improved AC load response a larger capacitor is recommended.
2, 6	NC	No connection
3	ADJ/NC	Adjustable voltage version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
4	GND	Ground
5	EN	Enable input, active high
7	PG	Power-Good pin, open-drain output. When the $V_{OUT}$ is below the PG threshold the PG pin is driven low; when the $V_{OUT}$ exceeds the threshold, the PG pin goes into a high-impedance state. To use the PG pin, use a 10kΩ to 1MΩ pull-up resistor to pull it up to a supply of up to 6V, which can be higher than the input voltage.
8	IN	The input of the regulator. Bypass to ground through at least 1µF ceramic capacitor.

## Functional Block Diagram



## Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
$V_{IN}$	Input Voltage	6.5	V
—	OUT, ADJ, EN Voltage	$V_{IN} + 0.3$	V
$T_J$	Operating Junction Temperature Range	-40 to +150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-65 to +150	$^\circ\text{C}$
$P_D$	Power Dissipation	Internally limited by maximum junction temperature of +150 $^\circ\text{C}$	—
$P_D$	Power Dissipation	U-DFN3030-8 (Type E)	mW
ESD HBM	Human Body Model ESD Protection	> 2	kV
ESD CDM	Charge Device Model	$\pm 1500$	V

Note: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

## Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage	2.2	6.0	V
$V_{OUT}$	Output Voltage	0.8	5.0	V
$I_{OUT}$	Output Current (Note 5)	0	1.0	A
$T_A$	Operating Ambient Temperature	-40	+85	$^\circ\text{C}$

Note: 5. The device maintains a stable, regulated output voltage without a load current. When the output current is large, attention should be given to the limitation of the package power dissipation.

**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $C_{IN} = 4.7\mu\text{F}$ ,  $C_{OUT} = 4.7\mu\text{F}$ ,  $V_{EN} = V_{IN}$ , unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
$V_{REF}$	FB Reference Voltage, ADJ Pin	$I_{OUT} = 10\text{mA}$ , $T_A = +25^\circ\text{C}$	0.792	0.8	0.808	V	
$I_{ADJ}$	ADJ Pin Leakage Current	—	—	0.1	0.5	$\mu\text{A}$	
$I_Q$	Input Quiescent Current	Enabled, $I_{OUT} = 0\text{A}$	—	68	91	$\mu\text{A}$	
$I_{SHDN}$	Input Shutdown Current	$V_{EN} = 0\text{V}$ , $I_{OUT} = 0\text{A}$	-1	0.05	1	$\mu\text{A}$	
$V_{OUT}$	Output Voltage Accuracy	$I_{OUT} = 100\text{mA}$ , $T_A = +25^\circ\text{C}$	$1.0\text{V} \leq V_{OUT} < 1.5\text{V}$	$V_{OUT(s)} - 0.015$	$V_{OUT(s)}$	$V_{OUT(s)} + 0.015$	V
			$1.5\text{V} \leq V_{OUT} \leq 3.3\text{V}$	$V_{OUT(s)}^* 0.99$	$V_{OUT(s)}$	$V_{OUT(s)}^* 1.01$	
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	Line Regulation	$V_{IN} = V_{OUT} + 1\text{V}$ to $5.5\text{V}$ , $I_{OUT} = 100\text{mA}$	$T_A = +25^\circ\text{C}$	—	0.01	0.1	%V
			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	—	0.2	
$\Delta V_{OUT} / V_{OUT}$	Load Regulation	$I_{OUT}$ from $1.0\text{mA}$ to $1\text{A}$	$1.2\text{V} < V_{OUT} \leq 3.3\text{V}$	-1.0	—	1.0	%
			$1.0\text{V} \leq V_{OUT} \leq 1.2\text{V}$	-1.5	—	1.5	%
$V_{DROPOUT}$	Dropout Voltage	$I_{OUT} = 300\text{mA}$	$1.0\text{V} \leq V_{OUT} < 1.1\text{V}$	—	710	(Note 6)	mV
			$1.1\text{V} \leq V_{OUT} < 1.2\text{V}$	—	600	(Note 6)	
			$1.2\text{V} \leq V_{OUT} < 1.3\text{V}$	—	500	(Note 6)	
			$1.3\text{V} \leq V_{OUT} < 1.4\text{V}$	—	400	(Note 6)	
			$1.4\text{V} \leq V_{OUT} < 1.5\text{V}$	—	300	(Note 6)	
			$1.5\text{V} \leq V_{OUT} < 2.0\text{V}$	—	200	(Note 6)	
			$2.0\text{V} \leq V_{OUT} < 2.6\text{V}$	—	140	250	
			$2.6\text{V} \leq V_{OUT} \leq 3.3\text{V}$	—	90	140	
		$I_{OUT} = 1\text{A}$	$1.0\text{V} \leq V_{OUT} < 1.1\text{V}$	—	840	(Note 6)	
			$1.1\text{V} \leq V_{OUT} < 1.2\text{V}$	—	780	(Note 6)	
			$1.2\text{V} \leq V_{OUT} < 1.3\text{V}$	—	710	(Note 6)	
			$1.3\text{V} \leq V_{OUT} < 1.4\text{V}$	—	660	(Note 6)	
			$1.4\text{V} \leq V_{OUT} < 1.5\text{V}$	—	610	(Note 6)	
			$1.5\text{V} \leq V_{OUT} < 2.0\text{V}$	—	570	(Note 6)	
			$2.0\text{V} \leq V_{OUT} < 2.6\text{V}$	—	440	600	
			$2.6\text{V} \leq V_{OUT} \leq 3.3\text{V}$	—	340	500	
$t_D$	Output Voltage Turn On Delay Time	$V_{IN} = V_{OUT} + 1\text{V}$ , $V_{EN}$ High to $V_{OUT}$ Rising 10%	—	50	—	$\mu\text{s}$	
$t_{SS}$	Output Voltage Ramp Up Time	$V_{OUT}$ Rising 10% to 90%	—	200	—	$\mu\text{s}$	
$t_{PG}$	PG React Time	$V_{OUT}$ 90% to PG Active	—	30	—	$\mu\text{s}$	
$t_{PGF}$	PG Off Deglitch Time	ADJ Falling to PG Low	—	3	—	$\mu\text{s}$	
		EN Goes Low to PG Low					
$V_{PGR}$	PG Rising Threshold	ADJ Rising	89	92	95	%	
$V_{PGF}$	PG Falling Threshold	ADJ Falling	79	82	85	%	
$V_{PGS}$	PG Sinking Voltage	$V_{IN} = 3.3\text{V}$ , Sinking Current = $5\text{mA}$	—	—	0.4	V	
$V_{IL}$	EN Input Logic Low Voltage	—	0	—	0.3	V	
$V_{IH}$	EN Input Logic High Voltage	—	1.0	—	$V_{IN}$	V	
$R_{ENPD}$	EN Pull-Down Resistor	—	—	3.0	—	M $\Omega$	
$I_{EN}$	EN Input Leakage Current	$V_{IN} = 5.5\text{V}$ , $V_{EN} = 0\text{V}$	-0.1	—	0.1	$\mu\text{A}$	
$R_{PD}$	Output Discharge Resistor	$V_{OL} = 1\text{V}$	—	100	—	$\Omega$	
$I_{OUT}$	Maximum Output Current	$V_{IN} = V_{OUT} + 1\text{V}$	1.0	—	—	A	

Notes: 6. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. This parameter only applies to output voltages above 2.0V since minimum  $V_{IN} = 2.2\text{V}$ .

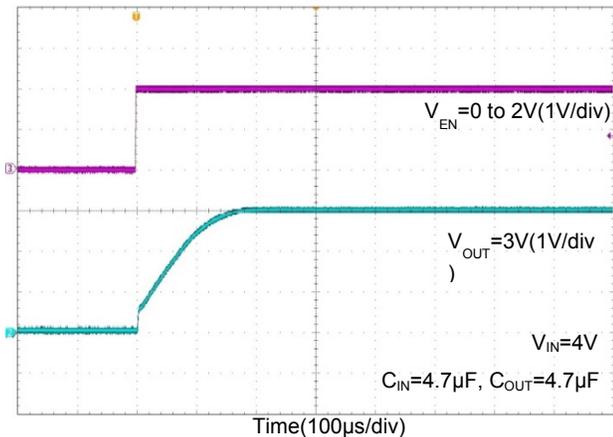
**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $C_{IN} = 4.7\mu\text{F}$ ,  $C_{OUT} = 4.7\mu\text{F}$ ,  $V_{EN} = V_{IN}$ , unless otherwise specified.)  
 (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{LIMIT}$	Current Limit	$V_{IN} = V_{OUT} + 1\text{V}$ ( $V_{IN\ MINI} = 2.2\text{V}$ )	1.3	1.5	—	A
$I_{SHORT}$	Short-Circuit Current	$V_{IN} = V_{OUT} + 1\text{V}$ , Output Voltage < 15% $V_{OUT}$	—	400	—	mA
PSRR	Power Supply Rejection Ratio (Note 7)	$f = 1\text{kHz}$ , $I_{OUT} = 100\text{mA}$ , $V_{OUT} = 1.2\text{V}$	—	75	—	dB
		$f = 10\text{kHz}$ , $I_{OUT} = 100\text{mA}$ , $V_{OUT} = 1.2\text{V}$	—	55	—	
$t_{ST}$	Start-Up Time	$V_{OUT} = 3\text{V}$ , $C_{OUT} = 2.2\mu\text{F}$ , $R_L = 30\Omega$	—	150	—	$\mu\text{s}$
$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	Output Voltage Temperature Coefficient	$I_{OUT} = 100\text{mA}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	$\pm 100$	—	ppm/ $^\circ\text{C}$
$T_{SHDN}$	Thermal Shutdown Threshold	—	—	+150	—	$^\circ\text{C}$
$T_{HYS}$	Thermal Shutdown Hysteresis	—	—	+20	—	$^\circ\text{C}$
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	U-DFN3030-8 (Type E ) (Note 8)	—	70	—	$^\circ\text{C/W}$

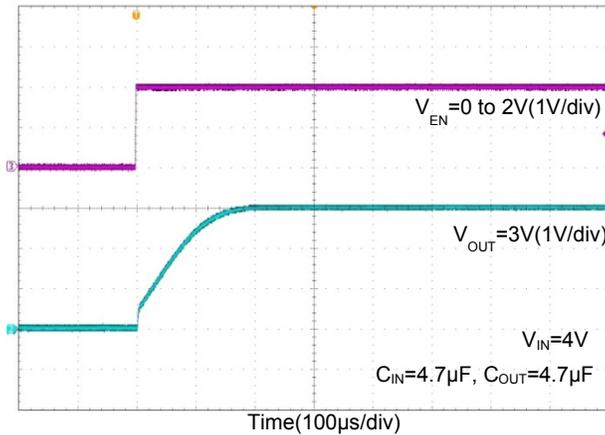
- Notes:
7. For  $V_{IN} \geq 2.5\text{V}$  and  $V_{IN} = V_{OUT} + 1\text{V}$ . For  $V_{IN} < 2.5\text{V}$ , the PSRR performance may be reduced.
  8. Test condition: U-DFN3030-8 (Type E) device is mounted on 2" x 2", FR-4 substrate PCB, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Typical Characteristics**

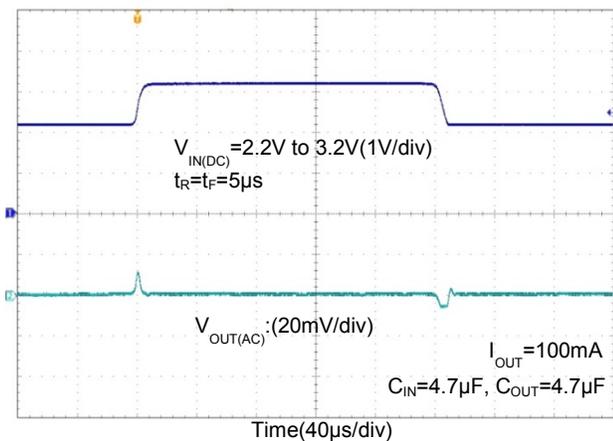
**Start-up Time**  
 $V_{OUT}=3V @ I_{OUT}=50mA$



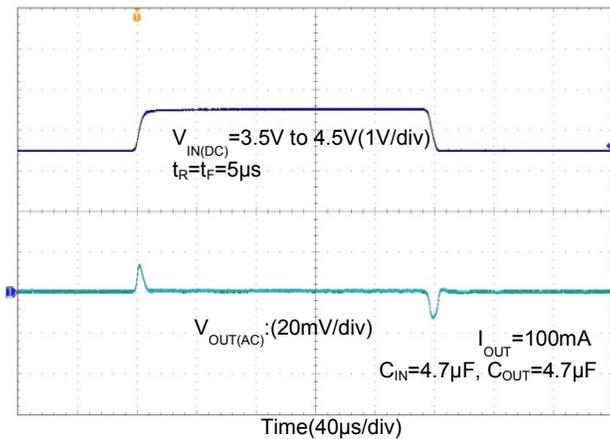
**Start-up Time**  
 $V_{OUT}=3V @ I_{OUT}=100mA$



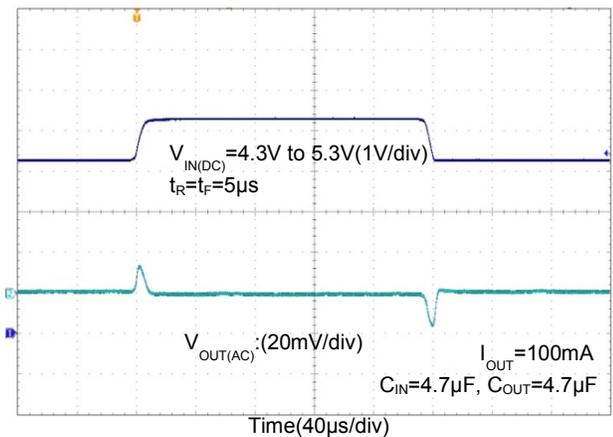
**Line Transient Response**  
 $V_{OUT}=1.2V$



**Line Transient Response**  
 $V_{OUT}=2.5V$



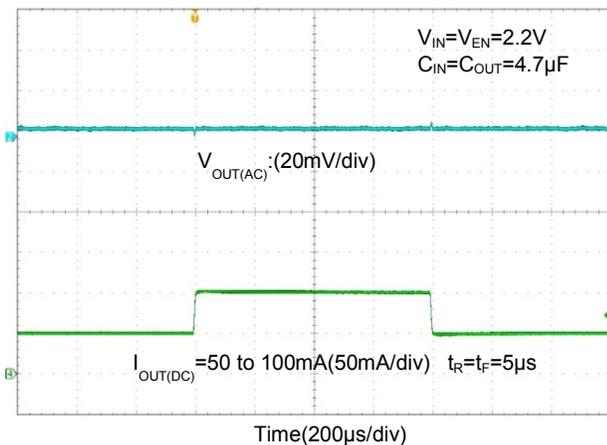
**Line Transient Response**  
 $V_{OUT}=3.3V$



**Typical Characteristics** (continued)

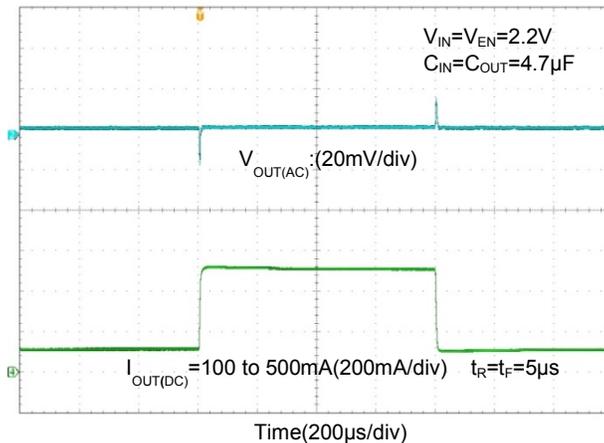
**Load Transient Response**

$V_{OUT}=1.2V$



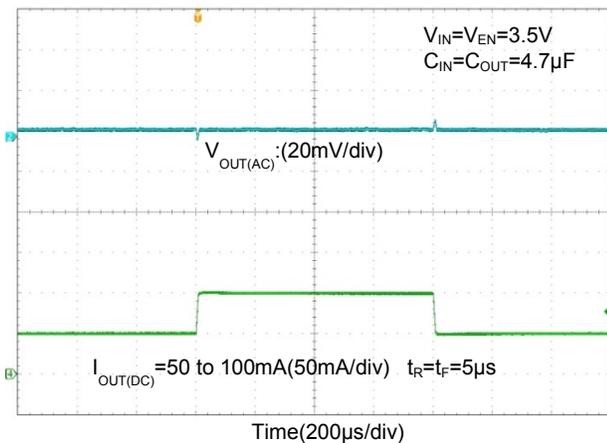
**Load Transient Response**

$V_{OUT}=1.2V$



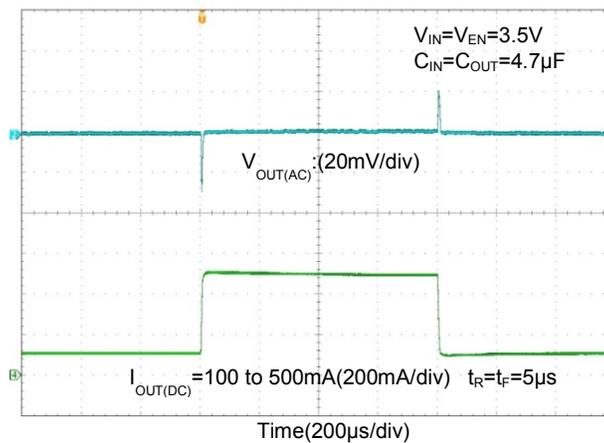
**Load Transient Response**

$V_{OUT}=2.5V$



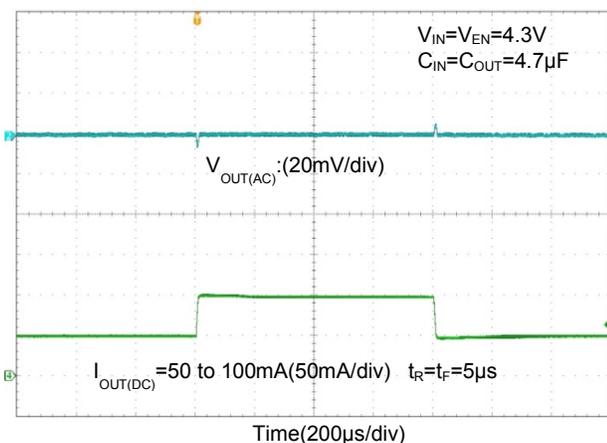
**Load Transient Response**

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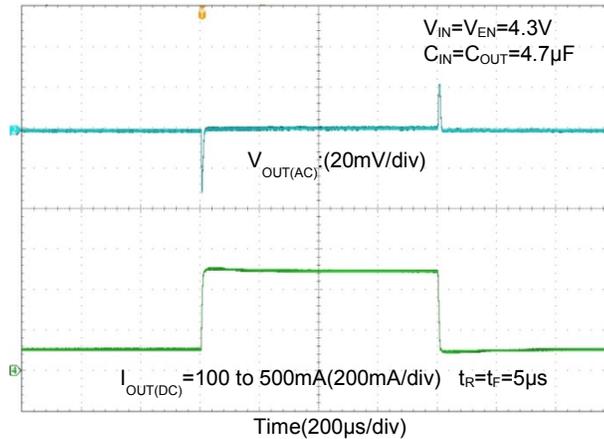
**Load Transient Response**

$V_{OUT}=3.3V$



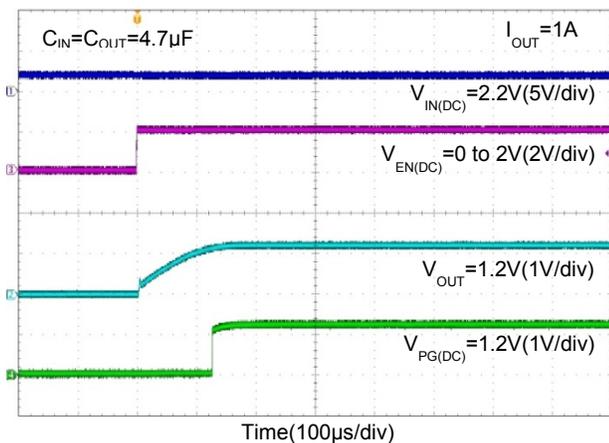
**Load Transient Response**

$V_{OUT}=3.3V$

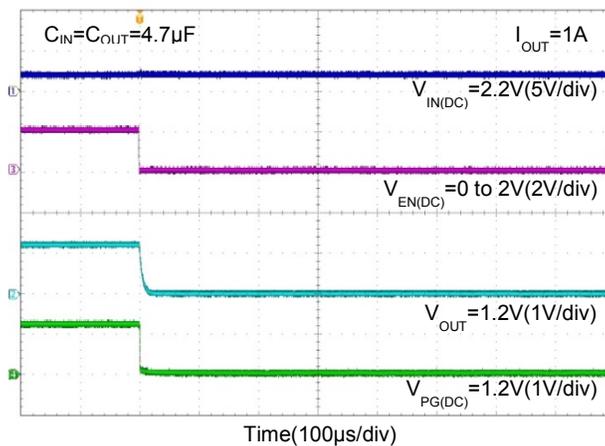


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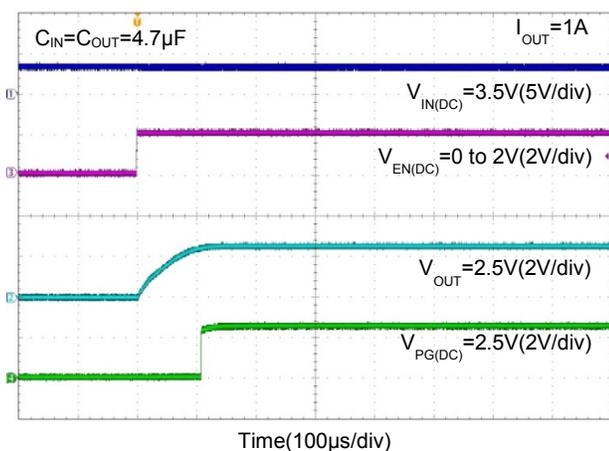
Enable Turn-On Response  
 $V_{OUT}=1.2V$



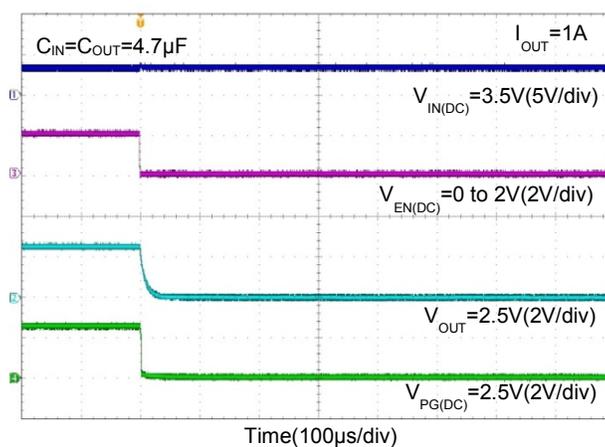
Enable Turn-Off Response  
 $V_{OUT}=1.2V$



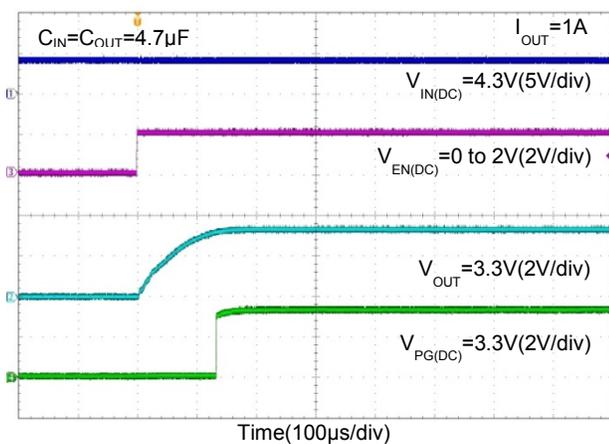
Enable Turn-On Response  
 $V_{OUT}=2.5V$



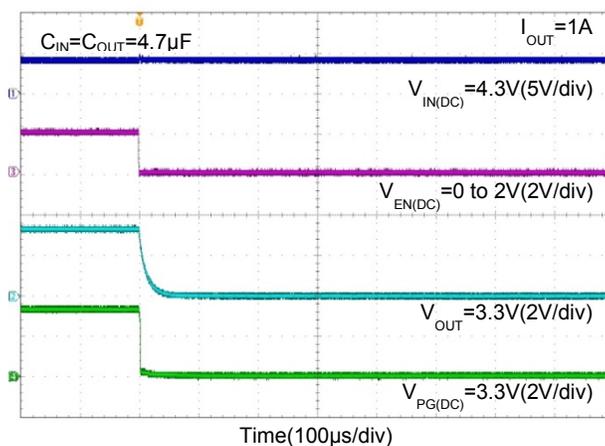
Enable Turn-Off Response  
 $V_{OUT}=2.5V$



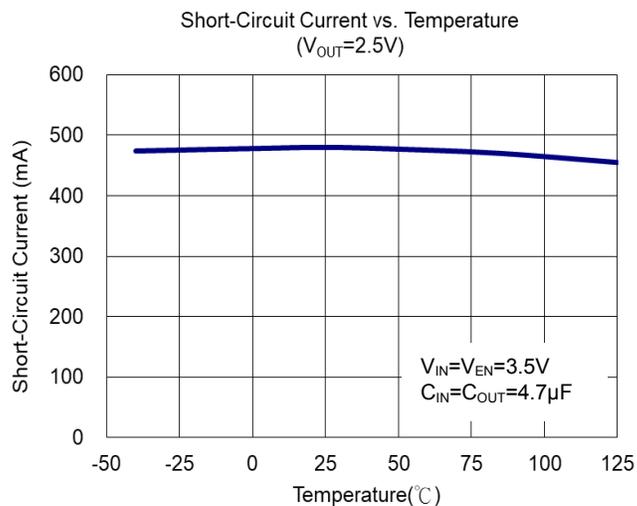
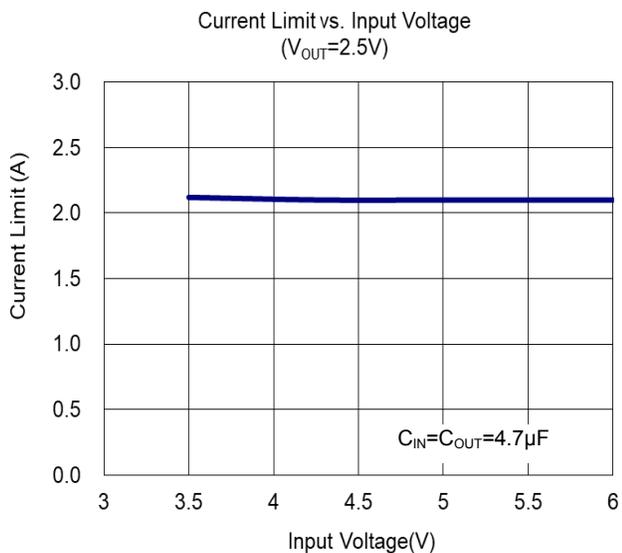
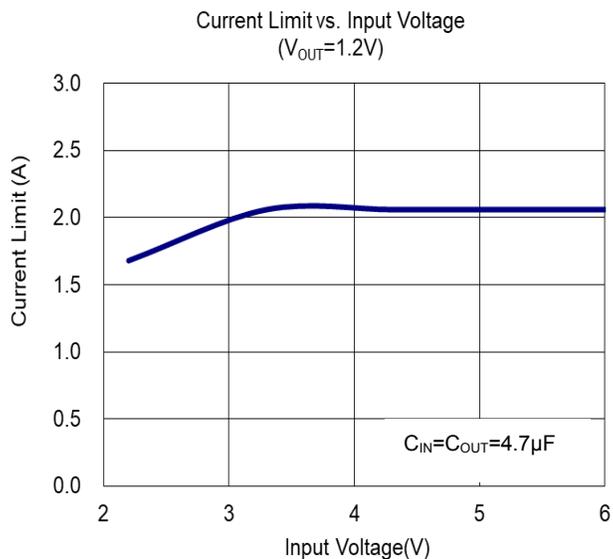
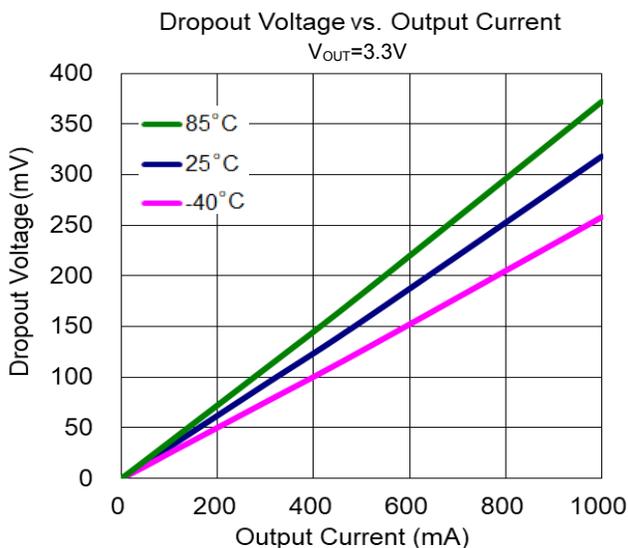
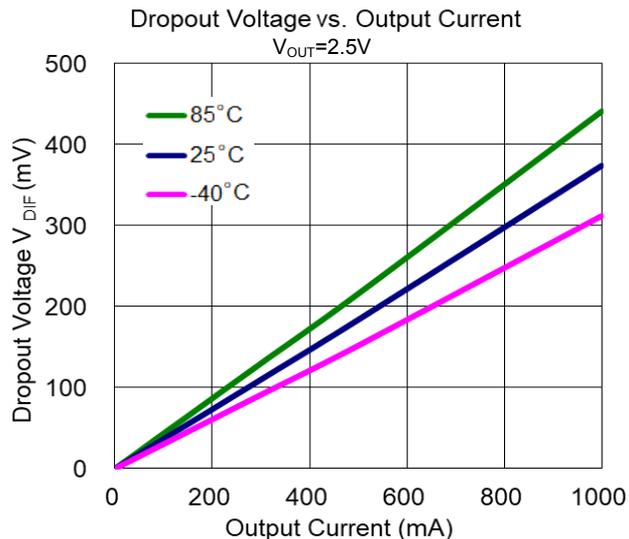
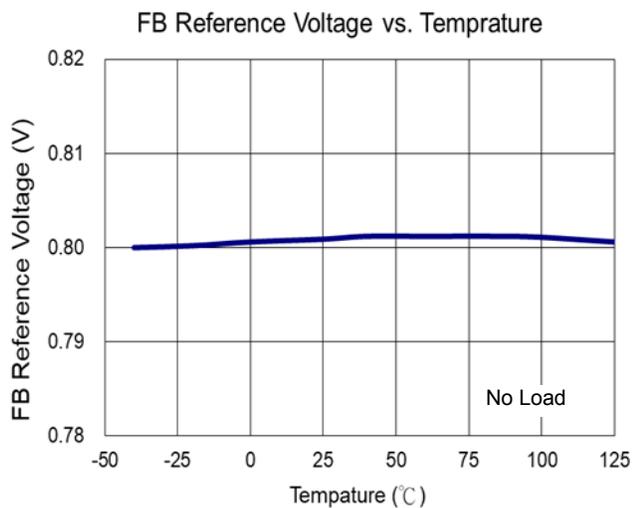
Enable Turn-On Response  
 $V_{OUT}=3.3V$



Enable Turn-Off Response  
 $V_{OUT}=3.3V$

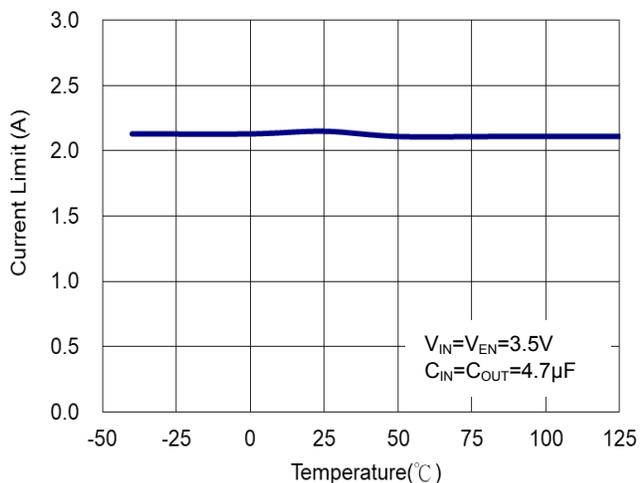


**Typical Characteristics** (continued)

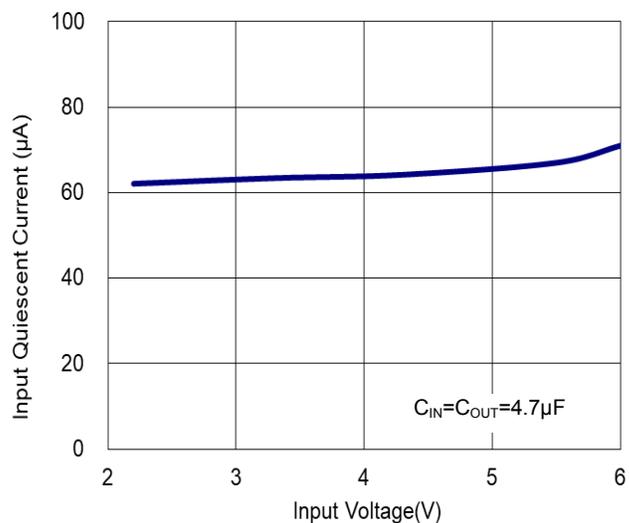


**Typical Characteristics** (continued)

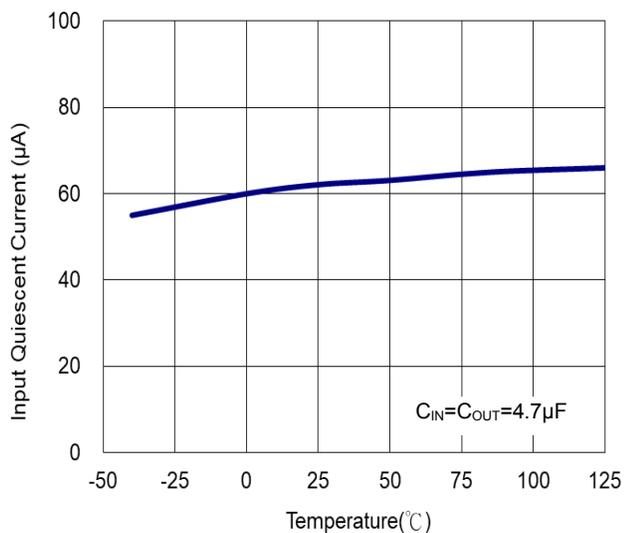
Current Limit vs. Temperature  
( $V_{OUT}=2.5V$ )



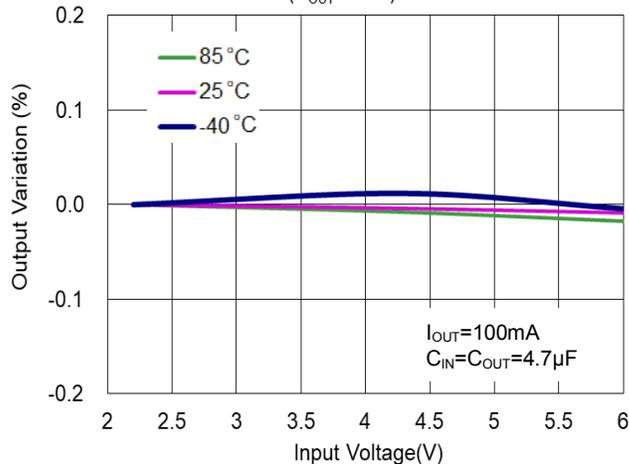
Input Quiescent Current vs. Input Voltage



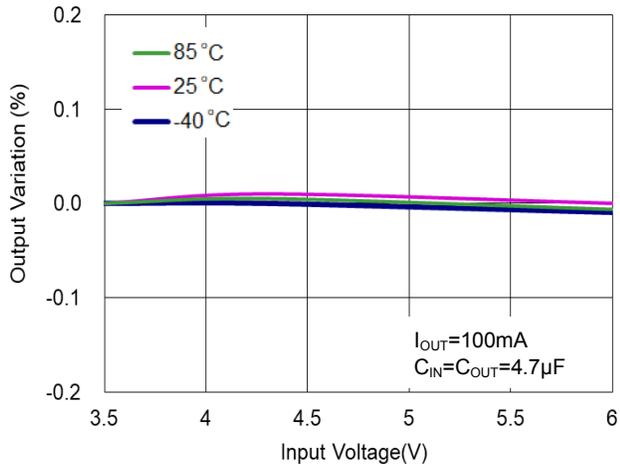
Input Quiescent Current vs. Temperature



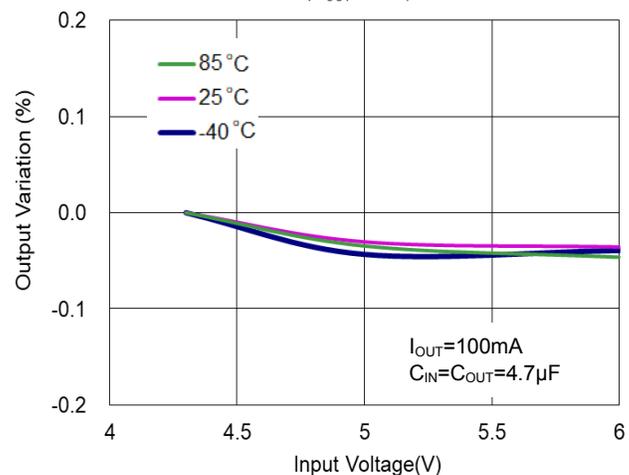
Line Regulation  
( $V_{OUT}=1.2V$ )



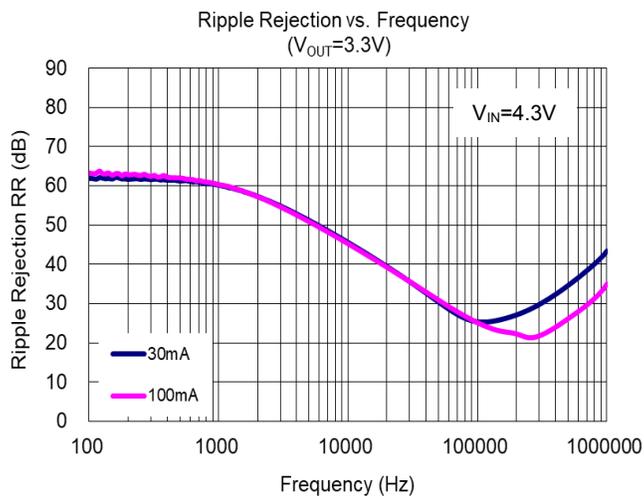
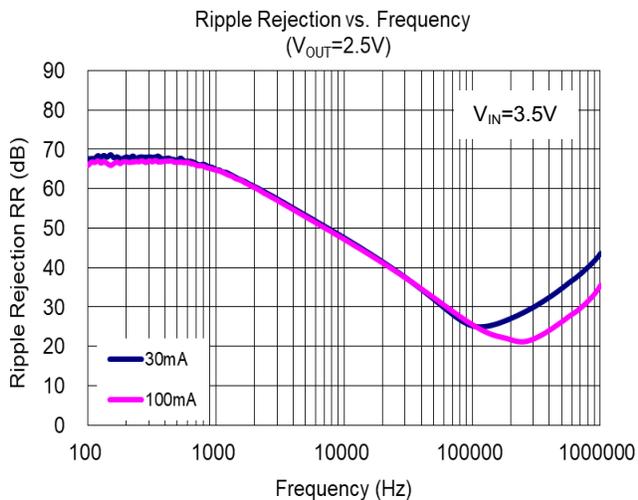
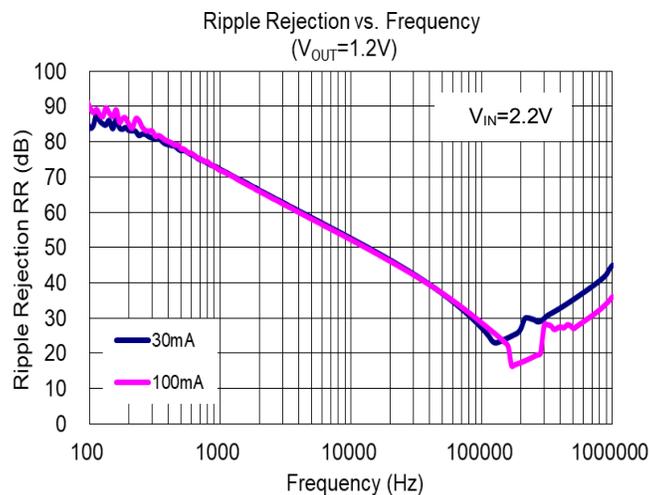
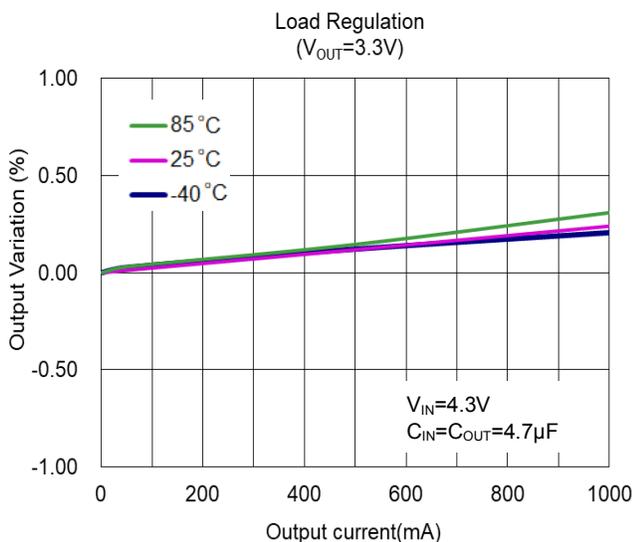
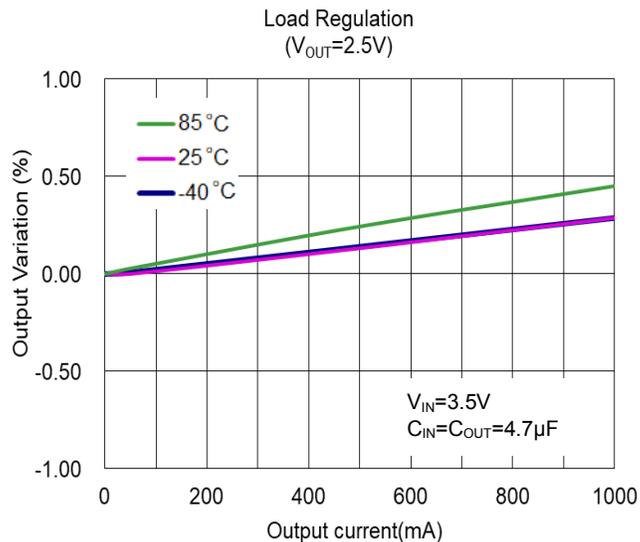
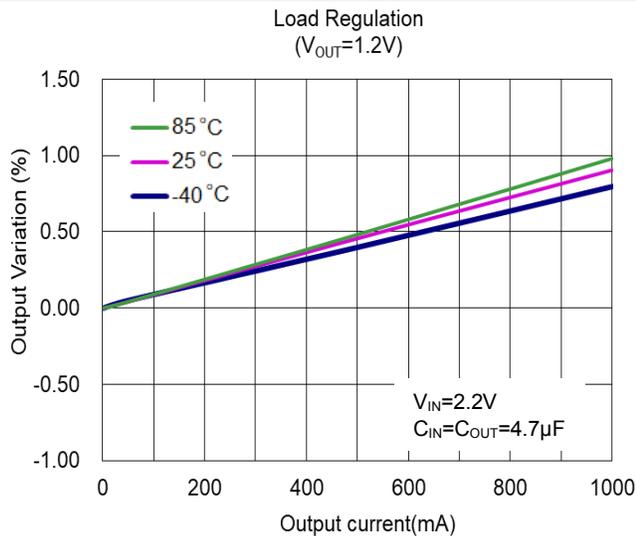
Line Regulation  
( $V_{OUT}=2.5V$ )



Line Regulation  
( $V_{OUT}=3.3V$ )



**Typical Characteristics** (continued)



## Application Information

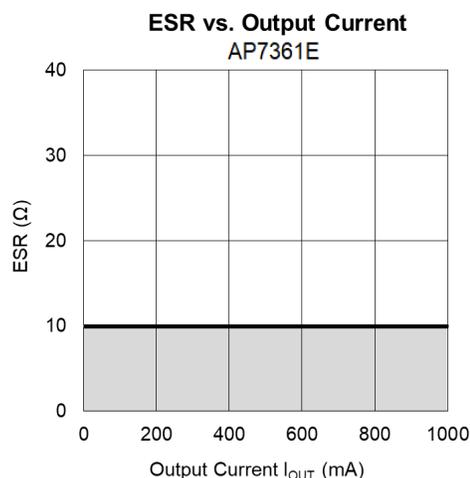
### Input Capacitor

A 1 $\mu$ F ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

### Output Capacitor

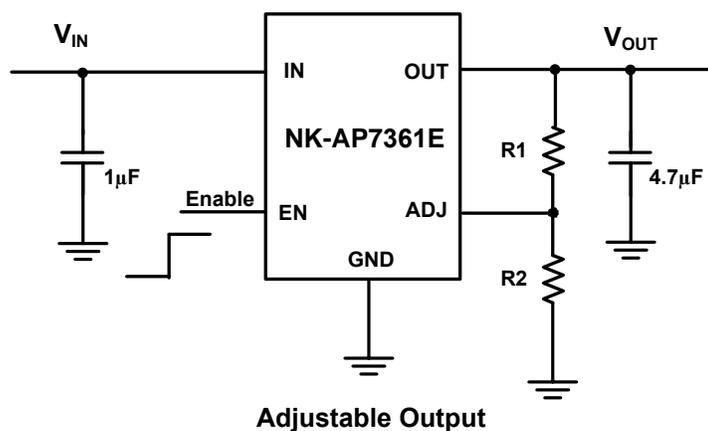
Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between  $I_{OUT}$  (Output Current) and ESR of an output capacitor are shown below. The stable region for the safety operating temperature (-40°C ~ +85°C) is marked as the gray area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +85°C.



### Adjustable Operation

The NK-AP7361E provides output voltage from 0.8V to 5.0V through external resistor divider as shown below.



## Application Information (continued)

The output voltage is calculated by:

$$V_{OUT} = V_{REF} \left( 1 + \frac{R_1}{R_2} \right)$$

Where  $V_{REF} = 0.8V$  (the internal reference voltage).

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R1 = R2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right)$$

To maintain the stability of the internal reference voltage, R2 needs to be kept smaller than 80kΩ.

### No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

### ON/OFF Input Operation

The NK-AP7361E is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under  $V_{IL}$  and  $V_{IH}$ .

### Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to prevent over-current and to protect the regulator from damage due to overheating.

### Short Circuit Protection

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 400mA. Full current is restored when the output voltage exceeds 15% of  $V_{OUT}$ . This feature protects the regulator from over-current and damage due to overheating.

### Power Good

The power-good (PG) pin is an open-drain output and can be pulled up through a resistor of 10kΩ to 1MΩ to  $V_{IN}$ ,  $V_{OUT}$  or any other rail that is 6V or lower. When the  $V_{OUT} \geq V_{PGR}$ , the PG output is high-impedance; if the  $V_{OUT}$  drops to below  $V_{PGF}$ , or the device is disabled, the PG pin is pulled to low by an internal MOSFET.

### Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

### Ultra Fast Start-up

After enabled, the NK-AP7361E is able to provide full power in as little as tens of microseconds, typically 200μs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

### Low Quiescent Current

The NK-AP7361E, consuming only around 60μA for all input range, provides great power saving in portable and low power applications.

### Power Dissipation

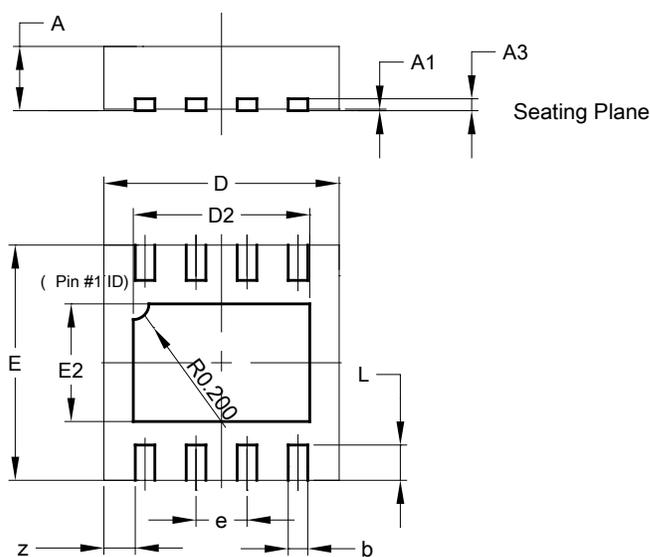
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

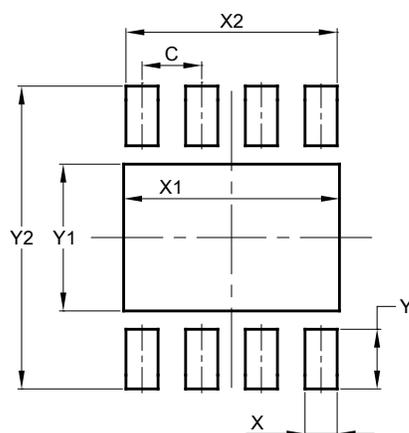
$$P_D(\max@T_A) = \frac{(+150^\circ\text{C} - T_A)}{R_{\theta JA}}$$

## Package Outline Dimensions

**U-DFN3030-8 (Type E)**


U-DFN3030-8 (Type E)			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.65
L	0.30	0.60	0.45
z	-	-	0.40
All Dimensions in mm			

## Suggested Pad Layout

**U-DFN3030-8 (Type E)**


Dimensions	Value (in mm)
C	0.650
X	0.350
X1	2.350
X2	2.300
Y	0.650
Y1	1.600
Y2	3.300

## Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 ④
- Weight: 0.0164 grams (Approximate)