优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Description

The NK-AP7363 is a 1.5A, adjustable output voltage, linear regulator with ultra-low dropout. The device includes pass element, error amplifier, band-gap, current limit, and thermal shutdown circuitry.

The device's characteristics of low dropout voltage and fast transient response to step changes in load make the device suitable for low-voltage microprocessor applications. The typical quiescent current is approximately 0.5mA and changes little with load current. The built-in current-limit and thermal-shutdown functions prevent IC damage in fault conditions.

This device is available in the U-DFN2030-8, SO-8EP, SOT223, and TO252 packages.

Features

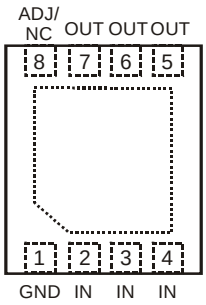
- 1.5A Ultra-Low Dropout Linear Regulator
- Ultra-Low Dropout: 190mV at 1.5A
- Stable With 10μF Input/Output Capacitor, Any Types
- Wide Input Voltage Range: 2.2V to 5.5V
- Adjustable Output Voltage: 0.6V to 5.0V
- Fixed Output Options: 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V
- Low Ground Pin Current
- 25nA Quiescent Current in Shutdown Mode
- Excellent Load/Line Transient Response
- Current Limit and Thermal Shutdown Protection
- Ambient Temperature Range: -40°C to +85°C
- U-DFN2030-8, SO-8EP, SOT223 and TO252: Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- ASIC Power Supplies In Printers, Graphics Cards, DVD Players, STBs, Routers, etc.
- FPGA and DSP Core or I/O Power Supplies
- SMPS Regulators
- Conversion From 3.3V or 5V Rail

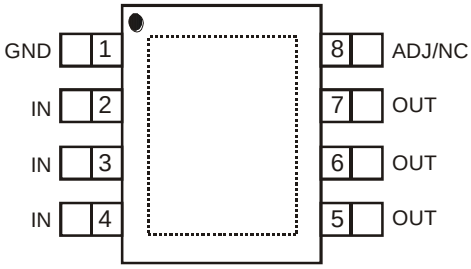
Pin Assignments

(Top View)



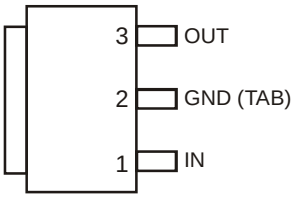
U-DFN2030-8

(Top View)



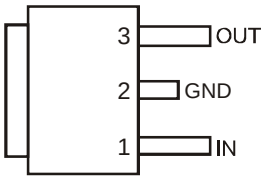
SO-8EP

(Top View)



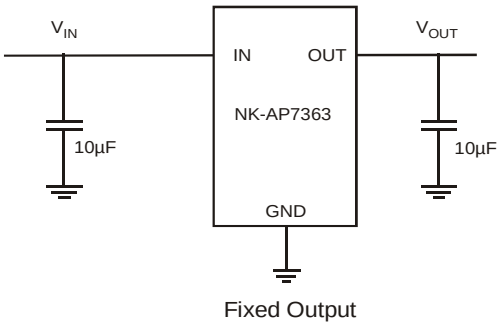
SOT223
(Fixed Output)

(Top View)

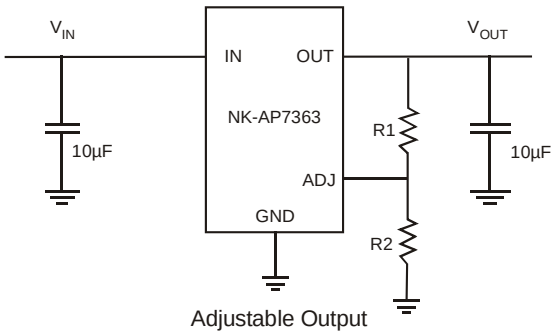


TO252

Typical Applications Circuit



Fixed Output



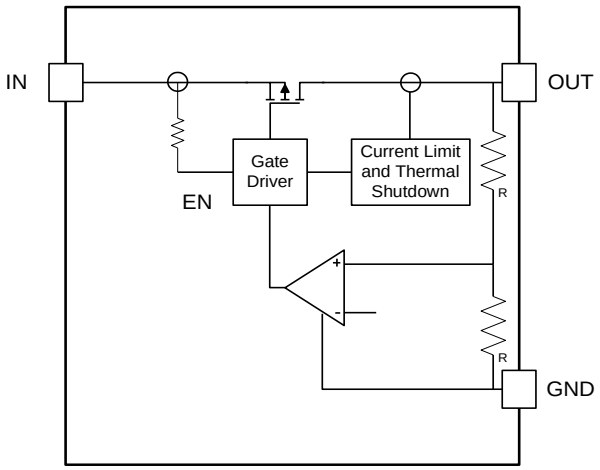
Adjustable Output

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right) \text{ where } R_2 \le 10k\Omega$$

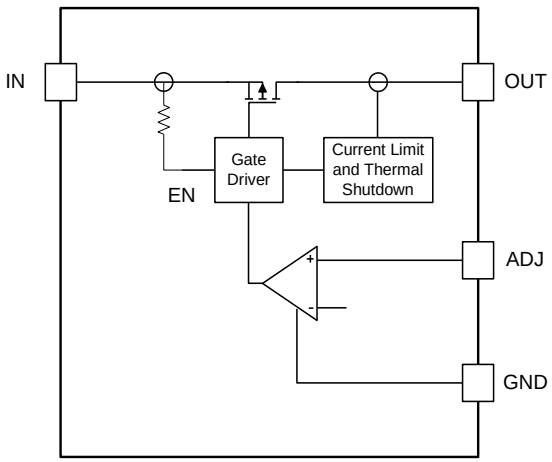
Pin Descriptions

Pin Name	Pin Number		Function
	SOT223 TO252	U-DFN2030-8 SO-8EP	
GND	2	1	Ground
IN	1	2, 3, 4	Voltage Input Pin
OUT	3	5, 6, 7	Voltage Output Pin
ADJ	NA	8	Output feedback pin for adjustable version only—a resistor divider from this pin to the OUT pin and ground sets the output voltage.
NC	NA	8	No connection for fixed output version.
EP/TAB	—	—	The exposed pad (EP) removes heat from the package, and it is recommended that the EP is connected to a copper area. The die is electrically connected to the exposed pad. It is recommended to connect the EP externally to GND, but it should not be the only ground connection.

Functional Block Diagram



Fixed Version



Adjustable Version

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	2000	V
ESD MM	Machine Model ESD Protection	200	V
V_{IN}	Input Voltage	-0.3 to +6.0	V
V_{OUT}	OUT Voltage	-0.3 to V_{IN} +0.3	V
I_{OUT}	Continuous Load Current	Internal Limited	—
T_{ST}	Storage Temperature Range	-65 to +150	°C
T_J	Maximum Junction Temperature	150	°C

Recommended Operating Conditions (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.2	5.5	V
I_{OUT}	Output Current	0	1.5	A
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature (Note 5)	-40	+125	°C

Notes:
4. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated are not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
5. Operating junction temperature must be evaluated and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature (T_{J-MAX}), and package thermal resistance (θ_{JA}).

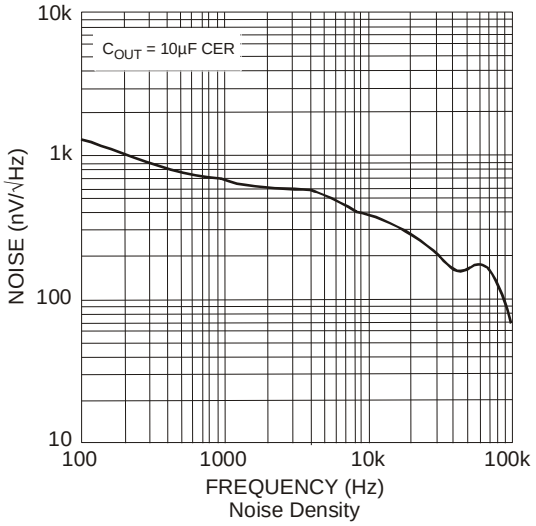
Electrical Characteristics (@ T_A = +25°C, V_{IN} = 3.3V, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 10µF, unless otherwise specified.)

Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = +25°C, and are provided for reference purposes only.

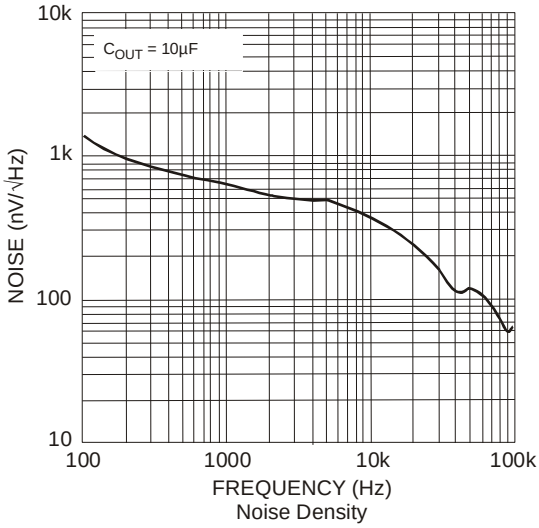
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{ADJ}	ADJ Pin Voltage	V_{IN} = V_{IN-MIN} to V_{IN-MAX}, I_{OUT} = 10mA to 1.5A	T_A = +25°C	0.584	0.605	0.626	V
			Over temp	0.575	—	0.635	
I_{ADJ}	ADJ Pin Bias Current	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	T_A = +25°C	—	50	—	nA
			Over temp	—	—	750	
$V_{DROPOUT}$	Dropout Voltage (Note 6)	I_{OUT} = 1.5A, V_{OUT} = 2.5V	T_A = +25°C	—	190	240	mV
			Over temp	—	—	280	
ΔV_{OUT} / ΔV_{IN}	Line Regulation (Note 7)	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	T_A = +25°C	—	0.04	—	%/V
			Over temp	—	0.05		
ΔV_{OUT} / ΔI_{OUT}	Load Regulation (Note 7)	I_{OUT} = 10mA to 1.5A	T_A = +25°C	—	0.18	—	%/A
			Over temp	—	0.33		
I_{GND}	Ground Pin Current in Normal Operation Mode	I_{OUT} = 10mA to 1.5A	T_A = +25°C	—	1.0	1.2	mA
			Over temp	—	—	1.3	
I_{OUT-PK}	Peak Output Current	V_{OUT} ≥ $V_{OUT-NOM}$ -5%			—	—	A
I_{SC}	Short Circuit Current	OUT Grounded	T_A = +25°C	—	3.7	—	A
			Over temp	2	—	—	
$t_{d(off)}$	Turn-Off Delay	From V_{EN} < V_{IL} to V_{OUT} = OFF, I_{OUT} = 1.5A		—	25	—	µs
$t_{d(on)}$	Turn-On Delay	From V_{EN} > V_{IH} to V_{OUT} = ON, I_{OUT} = 1.5A		—	25	—	µs
PSRR	Ripple Rejection	V_{IN} = 3.0V, I_{OUT} = 1.5A, f = 120Hz		—	65	—	dB
		V_{IN} = 3.0V, I_{OUT} = 1.5A, f = 1kHz		—	61	—	
$\rho_{n(l/f)}$	Output Noise Density	F = 120Hz, C_{OUT} = 10µF Ceramic		—	1.0	—	µV/√Hz
e_n	Output Noise Voltage	BW = 100Hz – 100kHz, C_{OUT} = 10µF Ceramic		—	100	—	µV(rms)
T_{SHDN}	Thermal Shutdown Threshold	T_J Rising		—	170	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	T_J Falling From T_{SHDN}		—	10	—	
Θ_{JA}	Thermal Resistance Junction-to-Ambient	U-DFN2030-8 (Note 8)		—	85.0	—	°C/W
		SO-8EP (Note 8)		—	52.8	—	
		SOT223 (Note 8)		—	105.7	—	
		TO252 (Note 8)		—	87.8	—	
Θ_{JC}	Thermal Resistance Junction-to-Case	U-DFN2030-8 (Note 8)		—	17.0	—	°C/W
		SO-8EP (Note 8)		—	10.0	—	
		SOT223 (Note 8)		—	18.5	—	
		TO252 (Note 8)		—	17.3	—	

Notes:
6. Dropout voltage is the minimum voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.
7. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.
8. Device mounted on 2" × 2" FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

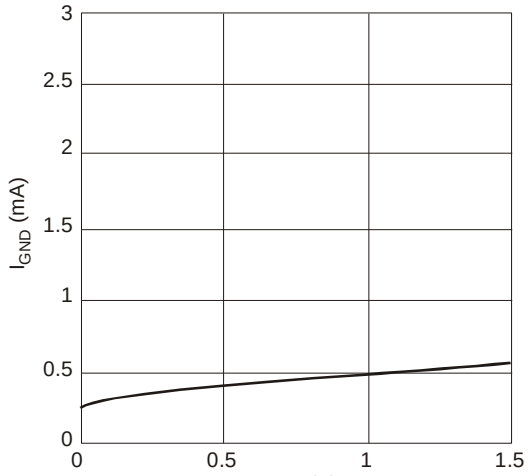
Typical Performance Characteristics (@ T_J = +25°C, V_{IN} = 2.7V, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 10mA, V_{OUT} = 1.8V)



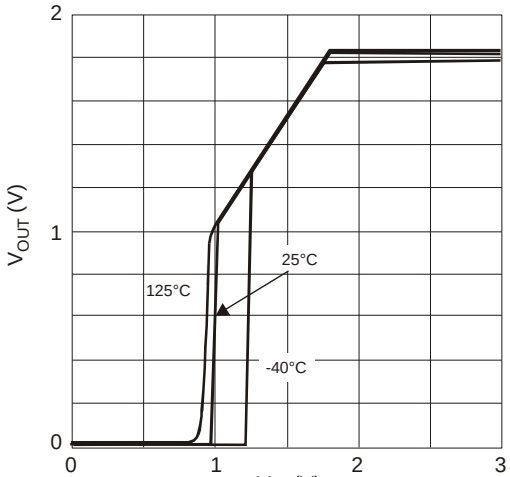
Noise Density



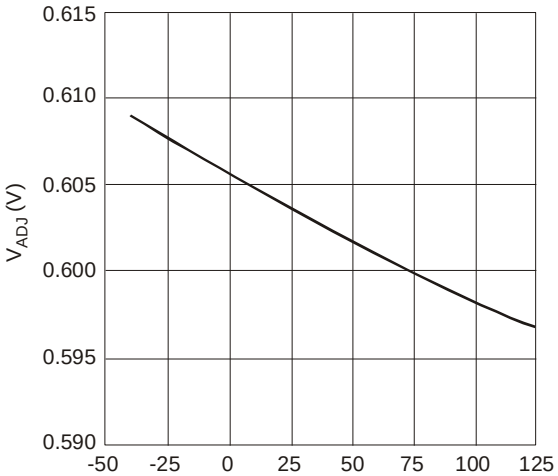
Noise Density



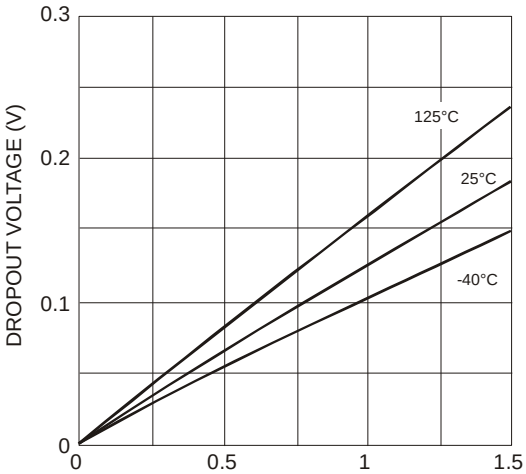
I_{GND} vs. Load Current



Turn-On Characteristics



V_{ADJ} vs. Temperature

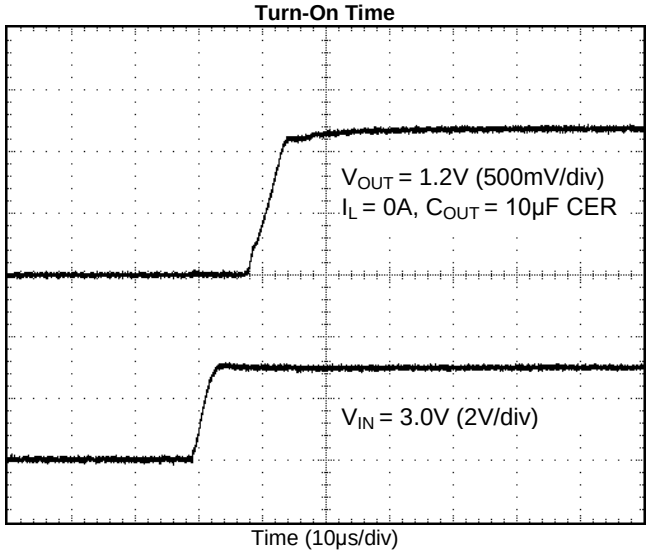


Dropout Voltage vs. Load Current

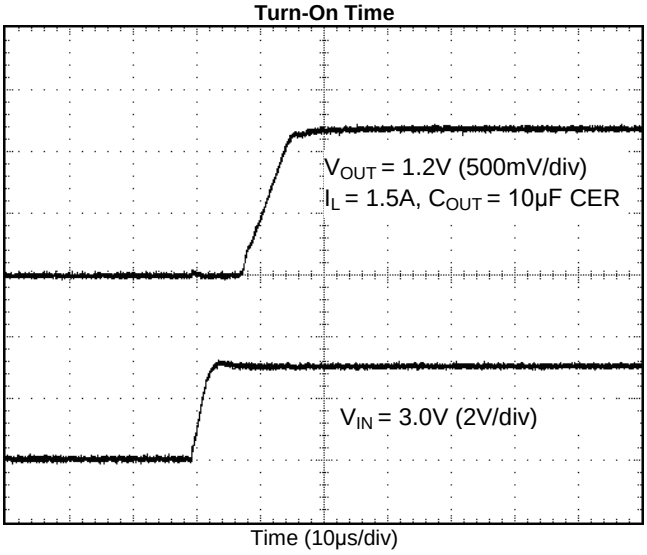
Typical Performance Characteristics (continued)

(@ T_J = +25°C, V_{IN} = 2.7V, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 10mA, V_{OUT} = 1.8V)

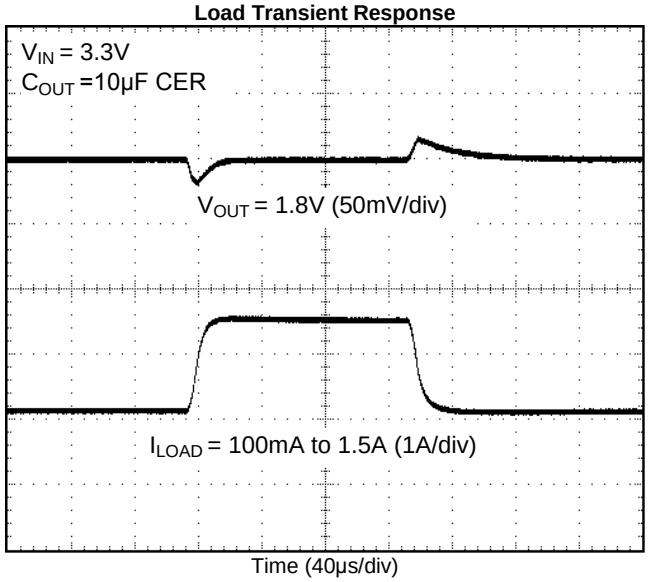
Turn-On Time

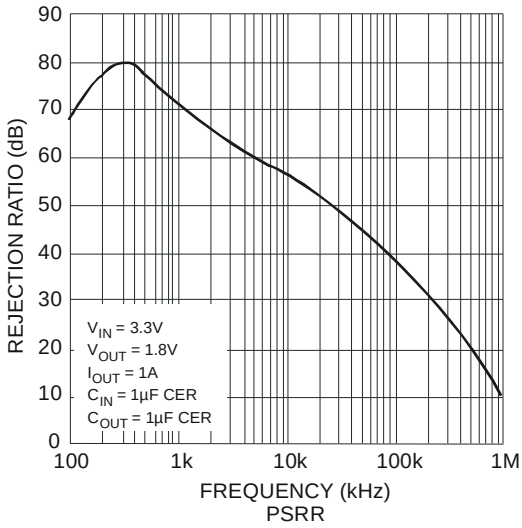


Turn-On Time



Load Transient Response





Application Note

Input Capacitor

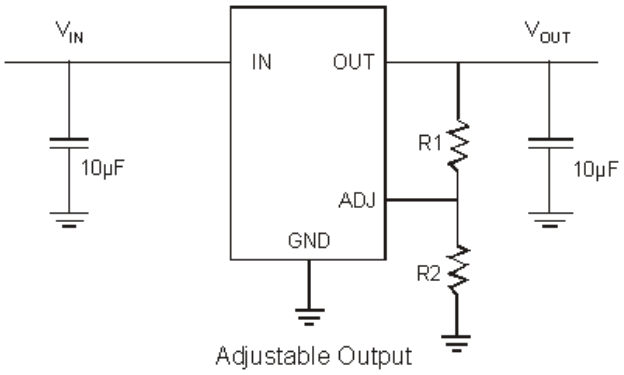
A minimum 2.2μF ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance can be increased without limit. A larger input capacitor, like 10μF, provides better load transient response. This input capacitor must be located as close as possible to the device to assure input stability and to reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while a higher ESR type requires more capacitance.

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The NK-AP7363 is stable with any type of capacitor with no limitations on minimum or maximum ESR. The device is designed to have excellent transient response for most applications with a small amount of output capacitance. The device is also stable with multiple capacitors in parallel, which can be of any type of value. Additional capacitance helps reduce undershoot and overshoot during transient loads. This capacitor must be placed as close as possible to OUT and GND pins for optimum performance.

Adjustable Operation

The NK-AP7363 provides output voltage from 0.6V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by the following equation:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Where V_{REF} = 0.6V (the internal reference voltage)

Rearranging the previous equation gives the following equation that is used for adjusting the output to a particular voltage:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}}-1\right)$$

To maintain the stability of the internal reference voltage, R_2 must be kept smaller than 10kΩ.

No Load Stability

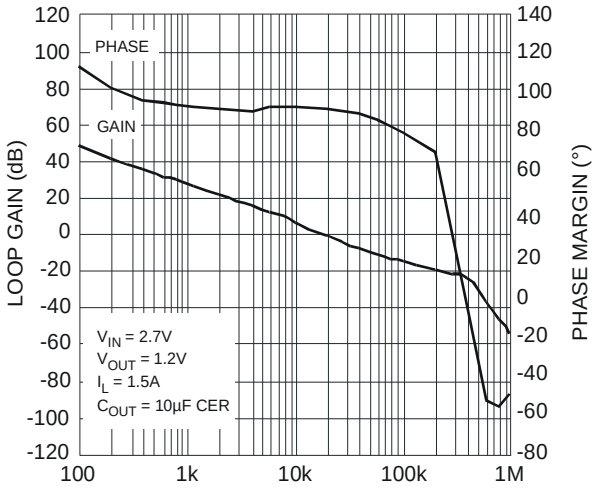
Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

Application Note (continued)

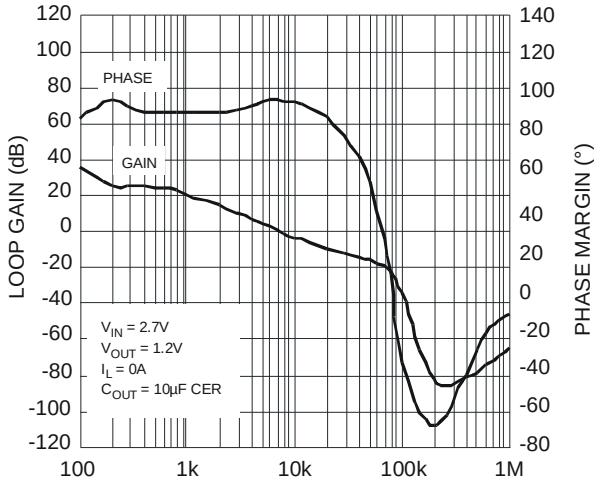
Stability and Phase Margin

Any regulator that operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and -180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The NK-AP7363 has an internal compensation circuit that maintains phase margin regardless of the ESR of the output capacitor—any type of capacitors can be used.

The following charts show the gain/phase plot of the NK-AP7363 with an output of 1.2V, 10μF ceramic output capacitor, and delivering 1.5A load current and no load. The phase margin is about 90°, which is very stable.



Gain-Bandwidth Plot for 1.5A Load



Gain-Bandwidth Plot for no Load

Short-Circuit Protection

When the output current at the OUT pin is higher than the current limit threshold, the current limit protection triggers and clamps the output current to prevent overcurrent and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +170°C, which allows the device to cool down. When the junction temperature reduces to approximately +160°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator and protects it from damage due to overheating.

Low Quiescent Current

The NK-AP7363, consuming only around 0.5mA for all input range, provides great power saving in portable and low-power applications.

Output Noise

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in μVrms or $\mu V\sqrt{Hz}$.

The NK-AP7363 is a low-noise regulator and requires no external noise reduction capacitor. Output voltage noise is typically 100μVrms, and overall noise level is between 100 Hz and 100 kHz.

Noise is specified in two ways:

Output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Output noise voltage is the RMS sum of spot noise over a specified bandwidth. Spot noise is measured in units μV/√Hz or nV/√Hz, and total output noise is measured in μV(rms). The primary source of noise in low-dropout regulators is the internal reference.

Application Note (continued)

Power Dissipation

The device power dissipation and proper sizing of the thermal plane connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

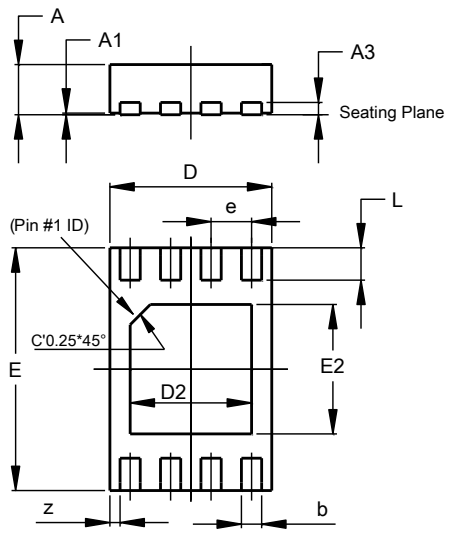
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the junction-to-ambient thermal resistance and maximum ambient temperature, which can be calculated by the following equation:

$$P_{D\_max} = \frac{(+150°C - T_A)}{R_{\theta JA}}$$

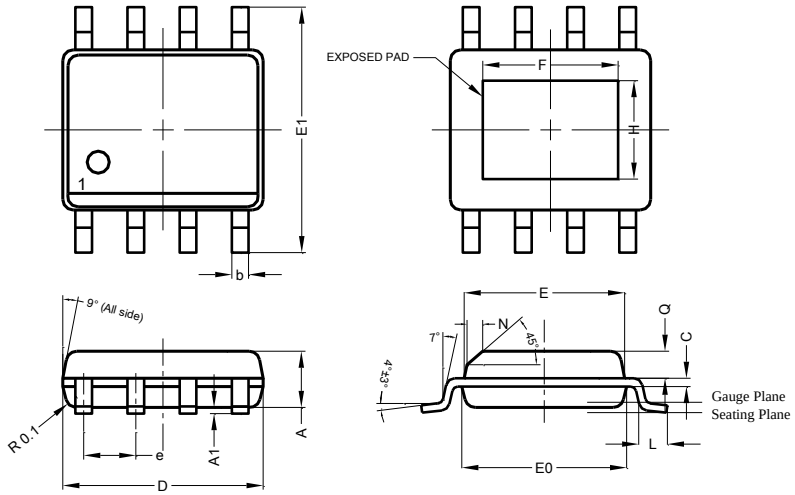
Package Outline Dimensions (All dimensions in mm.)

1) U-DFN2030-8



U-DFN2030-8			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.95	2.05	2.00
D2	1.40	1.60	1.50
e	-	-	0.50
E	2.95	3.05	3.00
E2	1.50	1.70	1.60
L	0.35	0.45	0.40
Z	-	-	0.125
All Dimensions in mm			

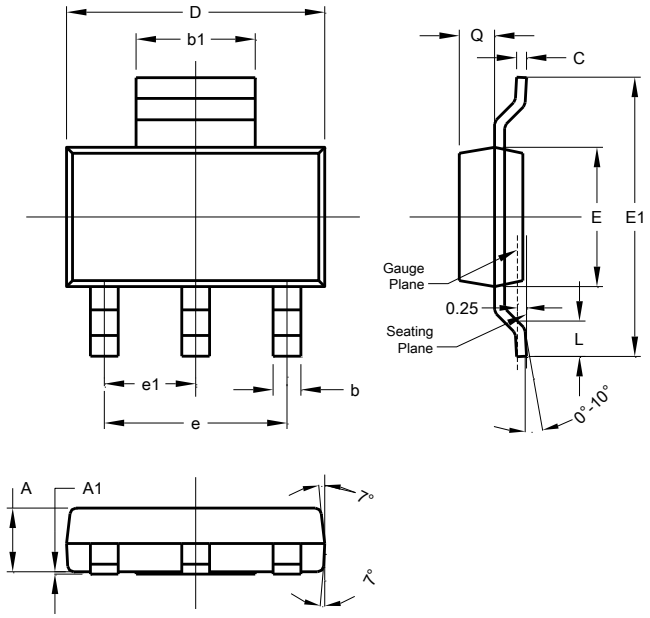
2) SO-8EP



SO-8EP			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

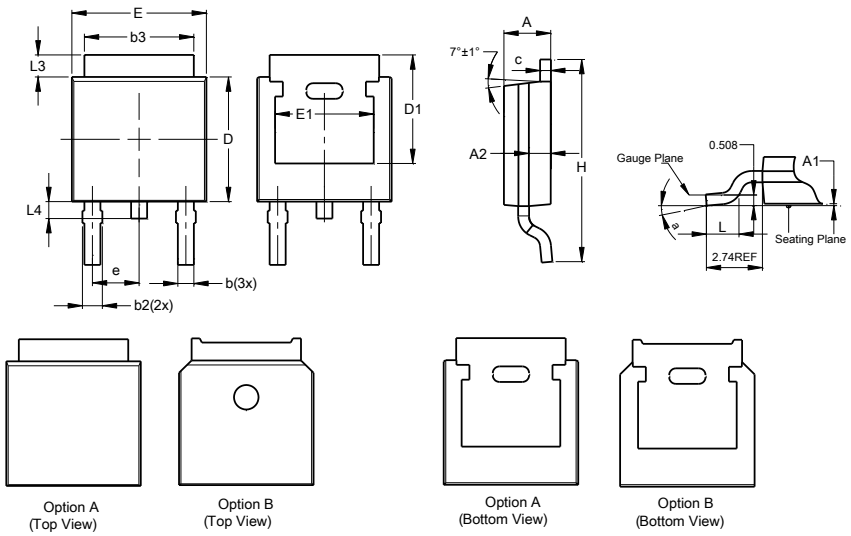
Package Outline Dimensions (continued) (All dimensions in mm.)

3) SOT223



SOT223			
Dim	Min	Max	Typ
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b	0.60	0.80	0.70
b1	2.90	3.10	3.00
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	-	-	4.60
e1	-	-	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

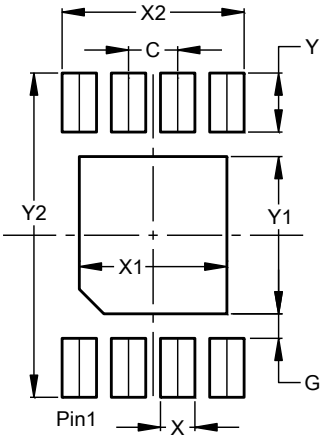
4) TO252 (Standard)



TO252 (Standard)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.60	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

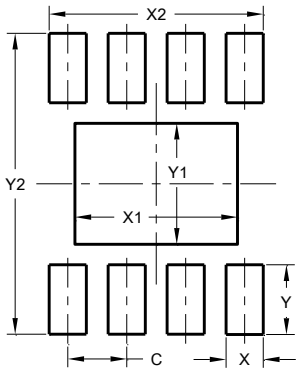
Suggested Pad Layout

1) U-DFN2030-8



Dimensions	Value (in mm)
C	0.500
G	0.250
X	0.350
X1	1.500
X2	1.850
Y	0.600
Y1	1.600
Y2	3.300

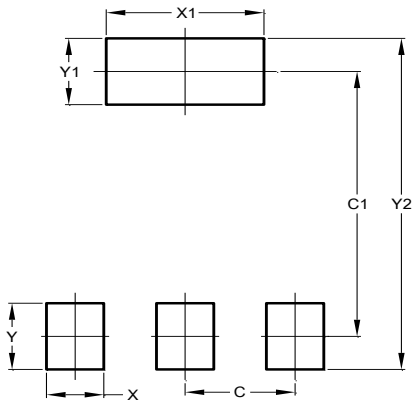
2) SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

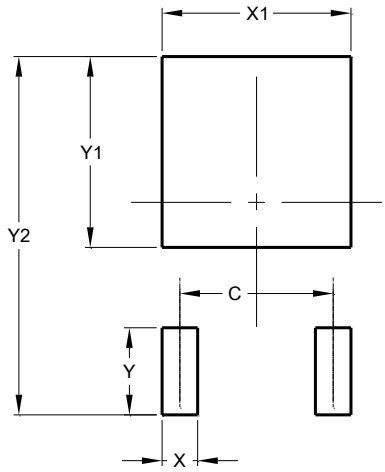
Suggested Pad Layout (continued)

3) SOT223



Dimensions	Value (in mm)
C	2.30
C1	6.40
X	1.20
X1	3.30
Y	1.60
Y1	1.60
Y2	8.00

4) TO252 (Standard)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

Mechanical Data

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals:
  - SOT223/ SO-8EP/ TO252 : Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
  - U-DFN2030-8: Finish - NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 e4
- Weight:
  - U-DFN2030-8: 0.0105 grams (Approximate)
  - SOT223: 0.113 grams (Approximate)
  - SO-8EP: 0.081 grams (Approximate)
  - TO252: 0.315 grams (Approximate)