优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码　企业QQ二维码

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_A = +25°C
Q1 N-Channel	100V	220mΩ @ V_{GS} = 10V	1.7A
		260mΩ @ V_{GS} = 4.5V	1.6A
Q2 P-Channel	-100V	250mΩ @ V_{GS} = -10V	-1.7A
		300mΩ @ V_{GS} = -4.5V	-1.6A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed

Description and Applications

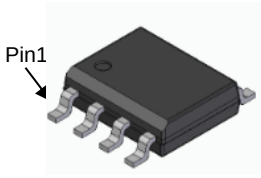
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions
- Backlighting

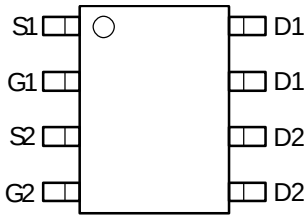
Mechanical Data

- Package: SO-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)

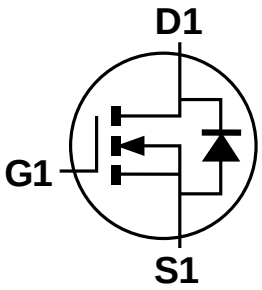
SO-8



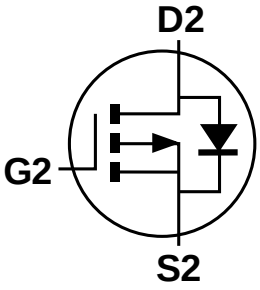
Top View



Top View
Pin Configuration



Q1 N-Channel MOSFET



Q2 P-Channel MOSFET

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1	Q2	Unit
Drain-Source Voltage			V_{DSS}	100	-100	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current (Note 6) N-Channel: V_{GS} = 10V P-Channel: V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	1.7 1.4	-1.7 -1.4	A
Maximum Body Diode Forward Current (Note 6)			I_S	1.7	-1.7	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	9	-13	A
Avalanche Current, L = 0.1mH			I_{AS}	3.2	-11	A
Avalanche Energy, L = 0.1mH			E_{AS}	0.5	6	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	110	°C/W
Total Power Dissipation (Note 6)		P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	80	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics N-Channel Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 100V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	170	220	mΩ	V_{GS} = 10V, I_D = 1.6A
		—	210	260		V_{GS} = 4.5V, I_D = 1.3A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1.1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	340	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	18	—		
Reverse Transfer Capacitance	C_{rss}	—	12	—		
Gate Resistance	R_g	—	2.1	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	4.1	—	nC	V_{DS} = 50V, I_D = 1.6A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	8.3	—		
Gate-Source Charge	Q_{gs}	—	1.5	—		
Gate-Drain Charge	Q_{gd}	—	2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	6.8	—	ns	V_{DS} = 50V, V_{GS} = 4.5V, R_G = 6.8Ω, I_D = 1A
Turn-On Rise Time	t_R	—	8.2	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	7.9	—		
Turn-Off Fall Time	t_F	—	3.6	—		
Body Diode Reverse Recovery Time	t_{RR}	—	17	—	ns	I_F = 1.1A, di/dt =100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	9.8	—	nC	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

Electrical Characteristics P-Channel Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-100	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -100V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-3.0	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	200	250	mΩ	V_{GS} = -10V, I_D = -1A
		—	210	300		V_{GS} = -4.5V, I_D =-1A
Diode Forward Voltage	V_{SD}	—	-0.9	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1030	—	pF	V_{DS} = -50V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	33	—		
Reverse Transfer Capacitance	C_{rss}	—	24	—		
Gate Resistance	R_g	—	13	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	8.4	—	nC	V_{DS} = -60V, I_D = -1A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	17.5	—		
Gate-Source Charge	Q_{gs}	—	2.8	—		
Gate-Drain Charge	Q_{gd}	—	3.2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	9.1	—	ns	V_{DD} = -50V, R_G = 9.1Ω, I_D = -1A
Turn-On Rise Time	t_R	—	14.9	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	57.4	—		
Turn-Off Fall Time	t_F	—	34.4	—		
Body Diode Reverse Recovery Time	t_{RR}	—	25.2	—	ns	V_{GS} = 0V, I_S = -1A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	24.5	—	nC	V_{GS} = 0V, I_S = -1A, di/dt = 100A/μs

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

N-Channel Q1

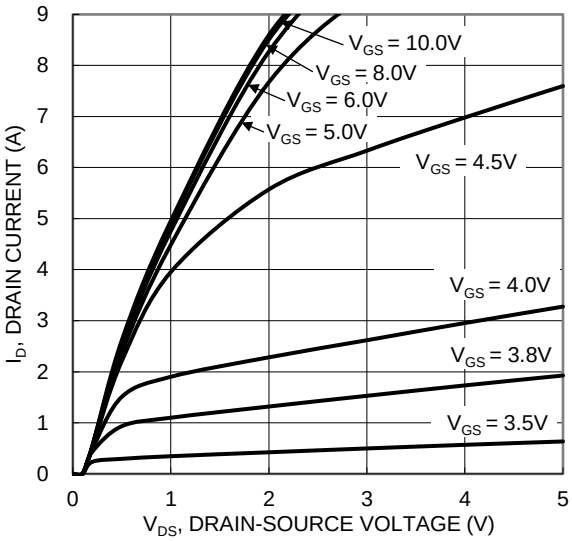


Figure 1. Typical Output Characteristic

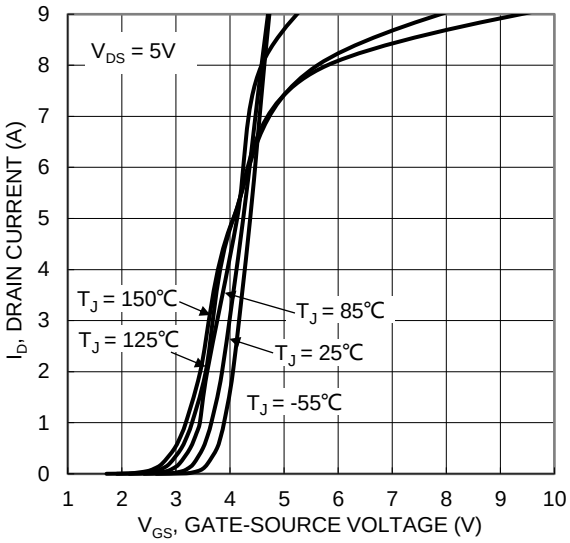


Figure 2. Typical Transfer Characteristic

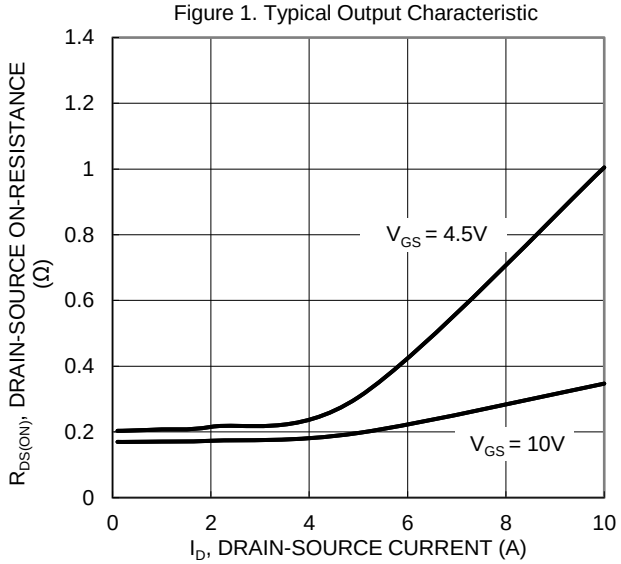


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

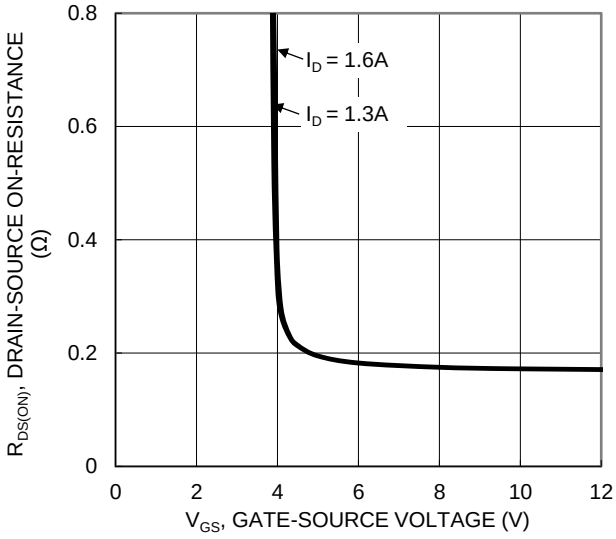


Figure 4. Typical Transfer Characteristic

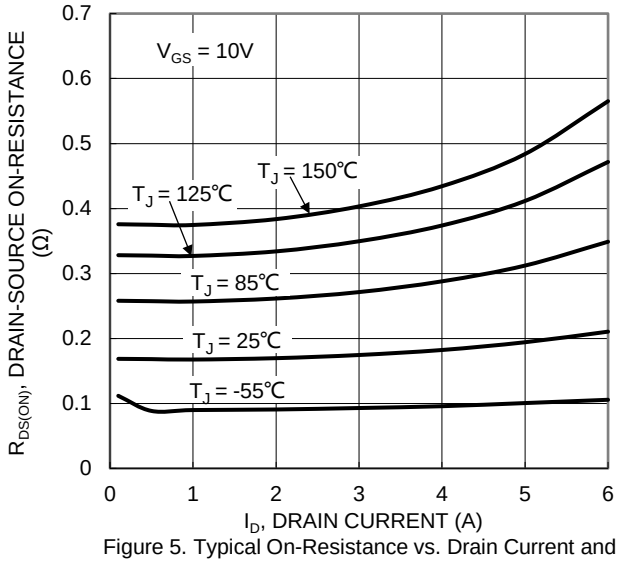


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

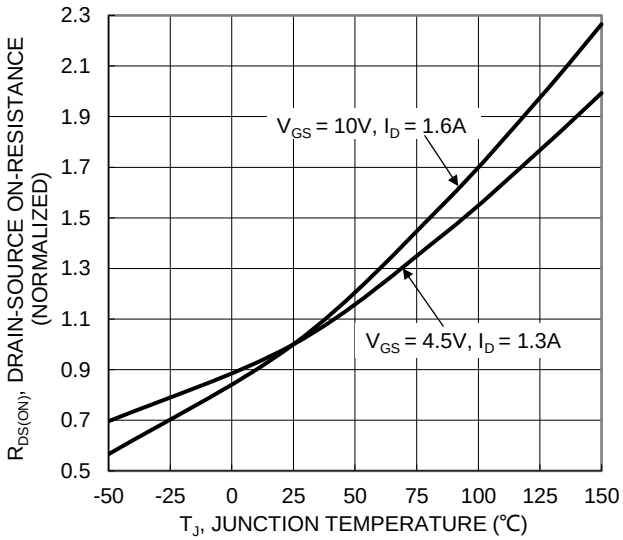


Figure 6. On-Resistance Variation with Temperature

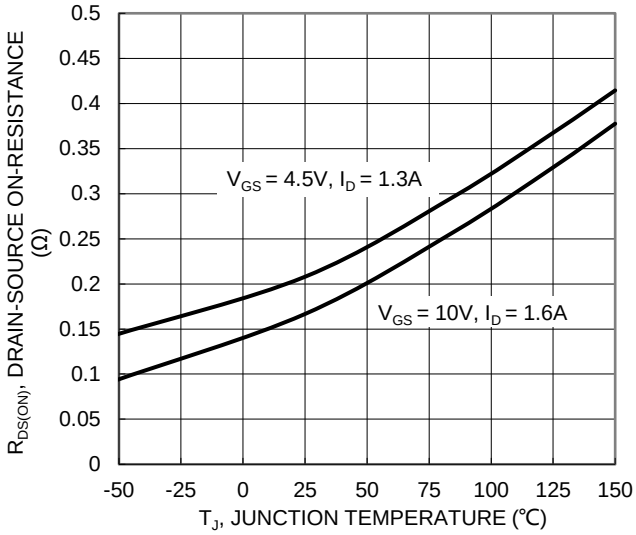


Figure 7. On-Resistance Variation with Temperature

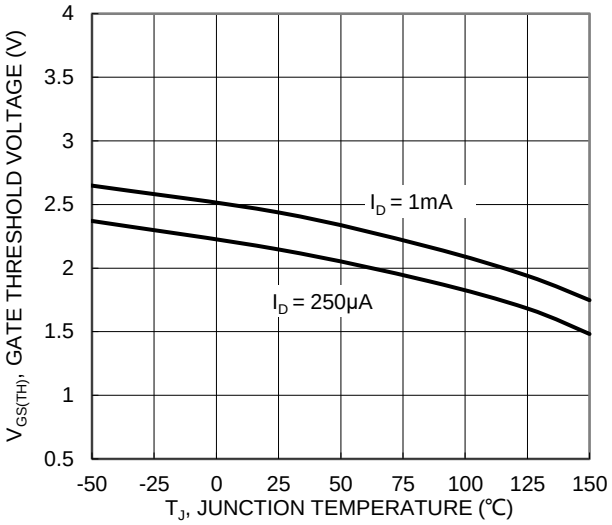


Figure 8. Gate Threshold Variation vs. Junction Temperature

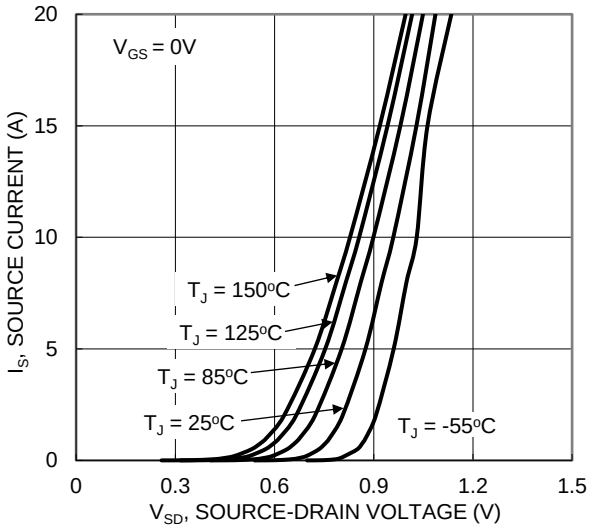


Figure 9. Diode Forward Voltage vs. Current

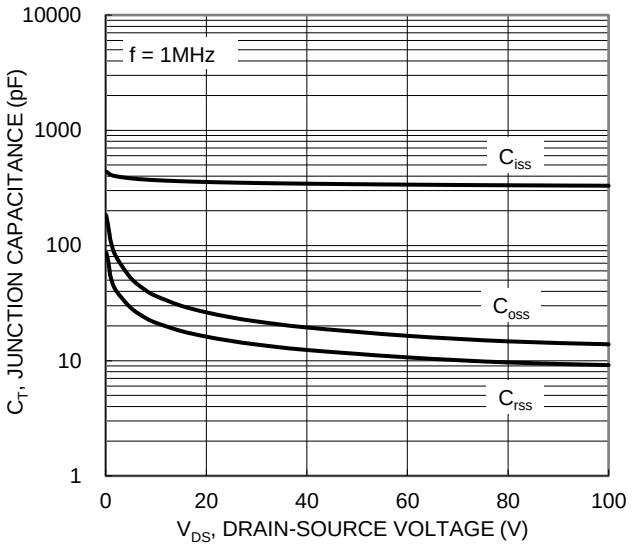


Figure 10. Typical Junction Capacitance

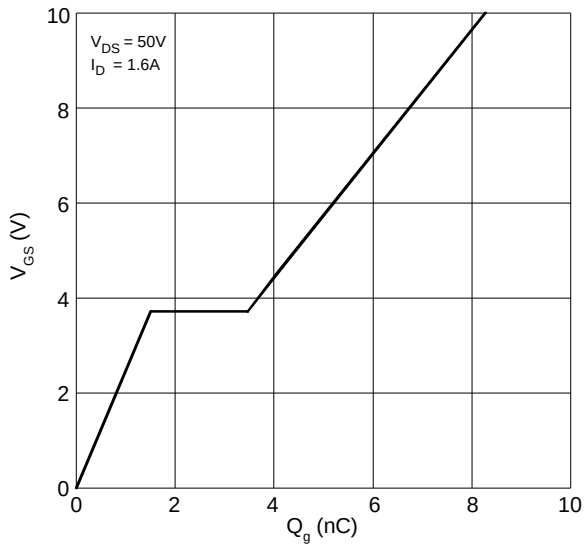


Figure 11. Gate Charge

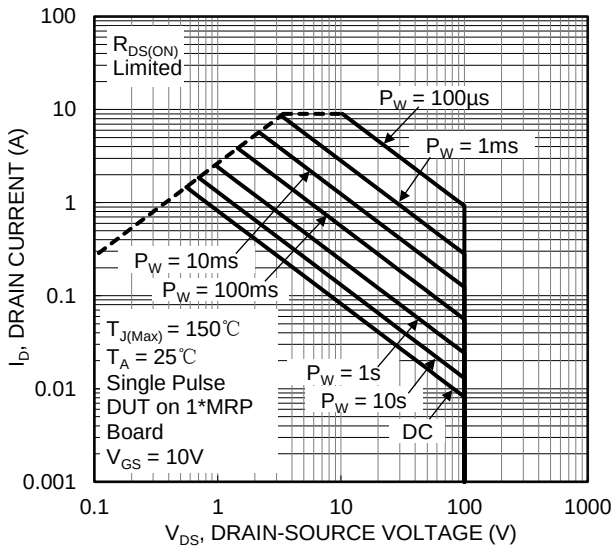


Figure 12. SOA, Safe Operation Area

P-Channel Q2

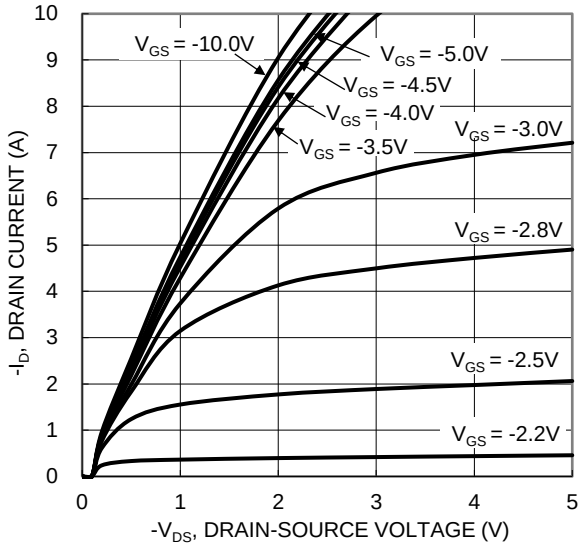


Figure 13. Typical Output Characteristic

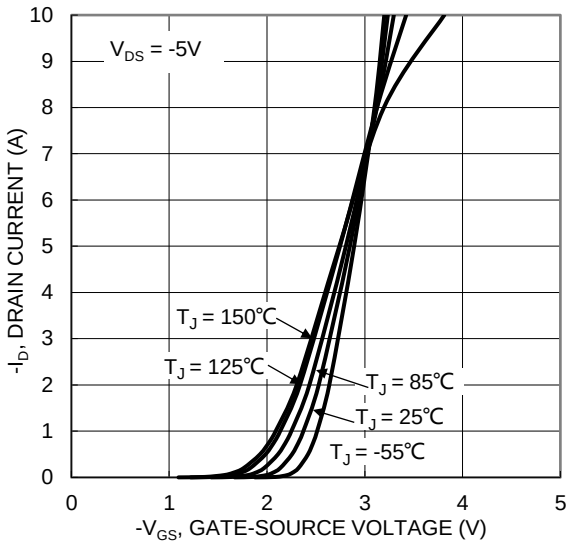


Figure 14. Typical Transfer Characteristic

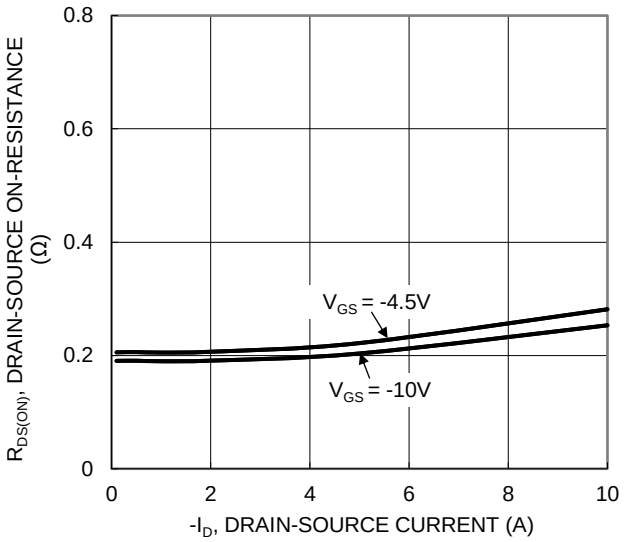


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

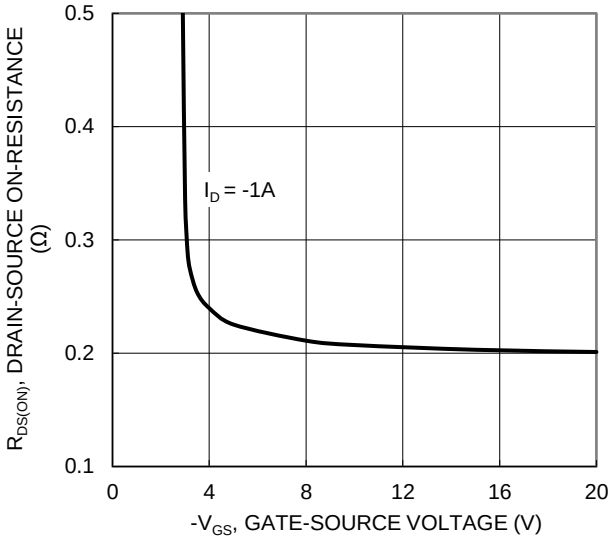


Figure 16. Typical Transfer Characteristic

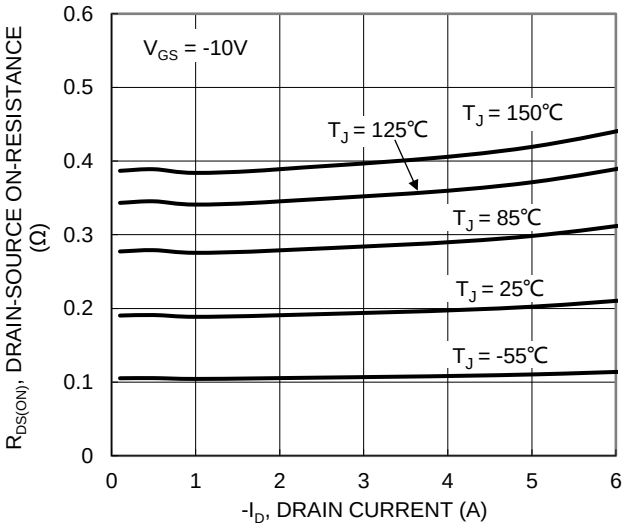


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

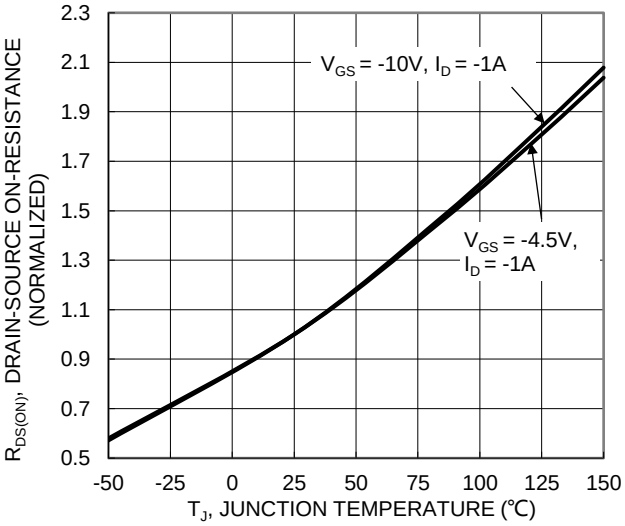


Figure 18. On-Resistance Variation with Temperature

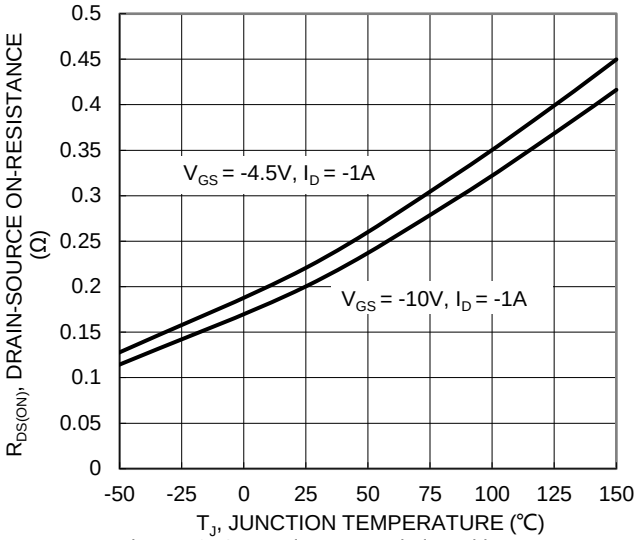


Figure 19. On-Resistance Variation with Temperature

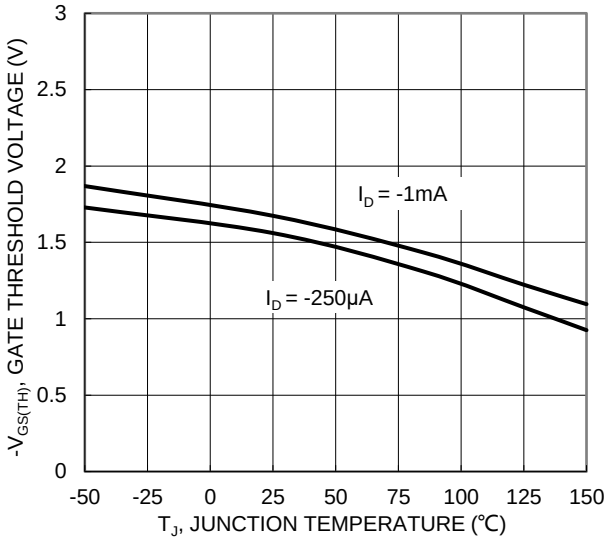


Figure 20. Gate Threshold Variation vs. Junction Temperature

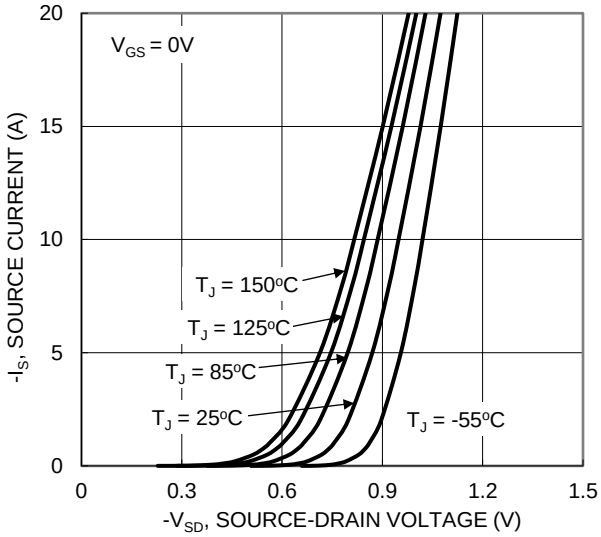


Figure 21. Diode Forward Voltage vs. Current

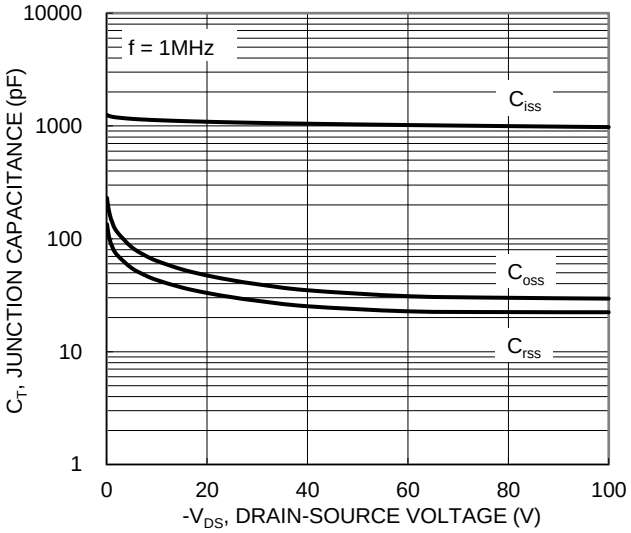


Figure 22. Typical Junction Capacitance

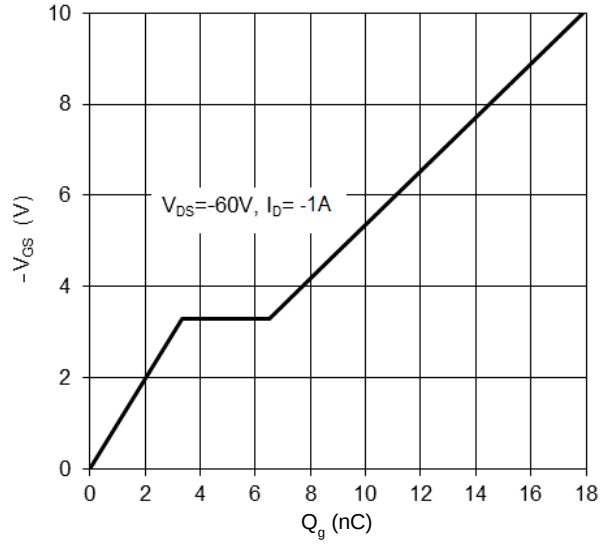


Figure 23. Gate Charge

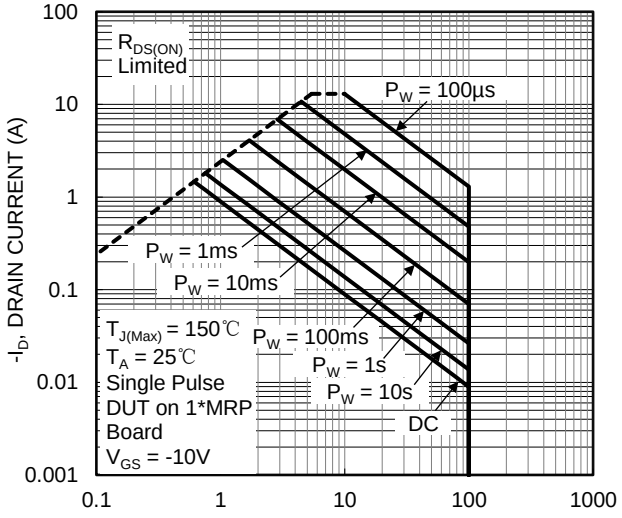


Figure 24. SOA, Safe Operation Area

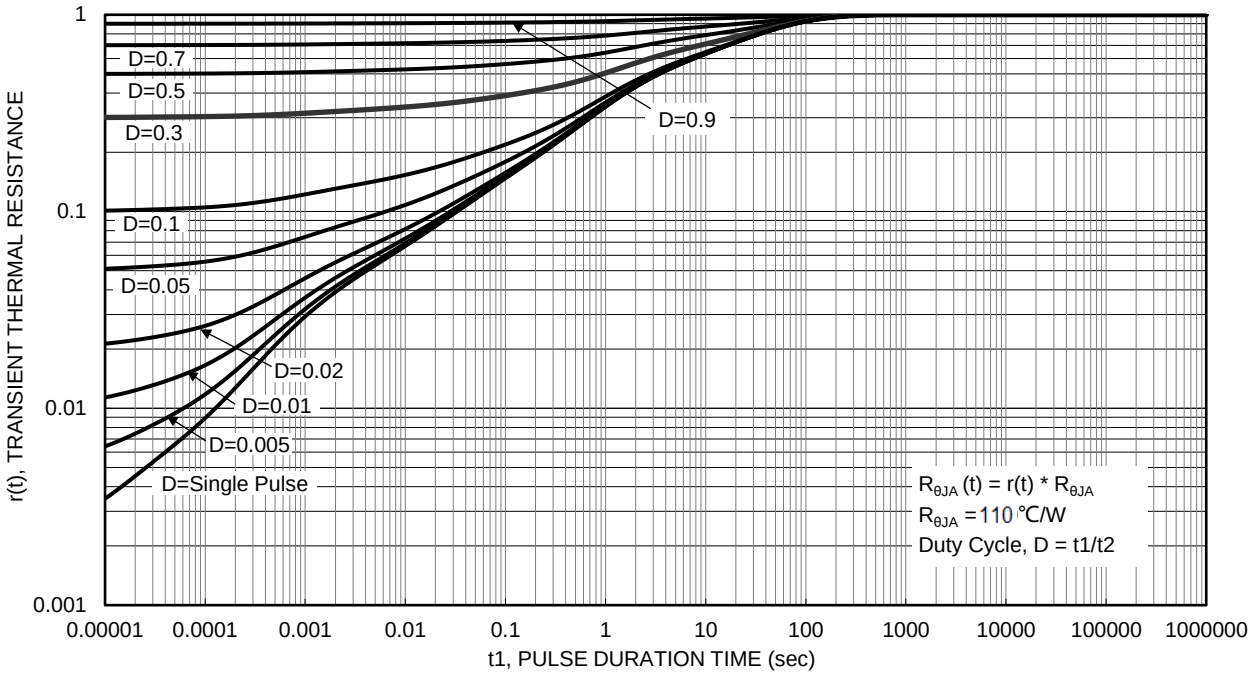
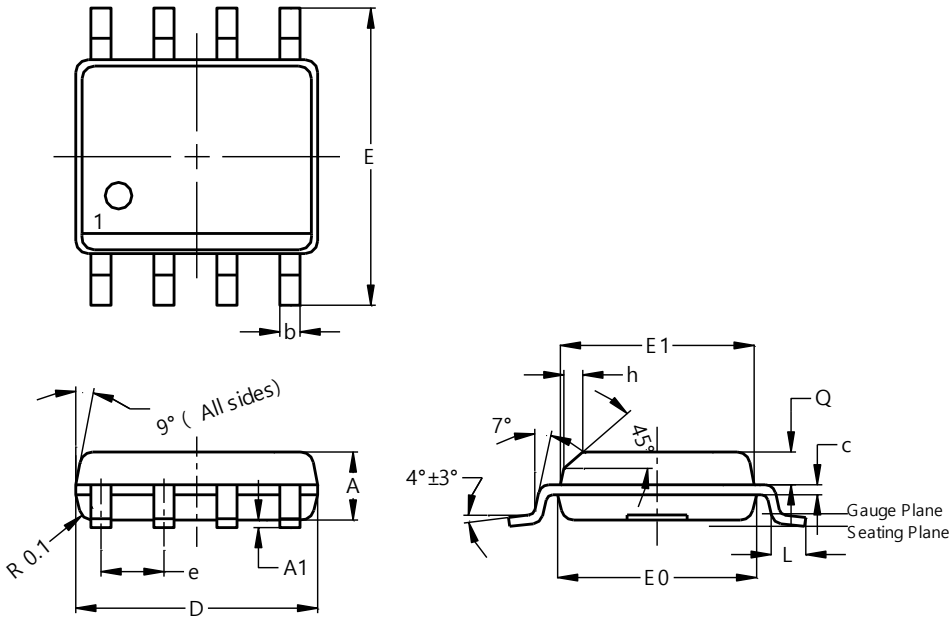


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

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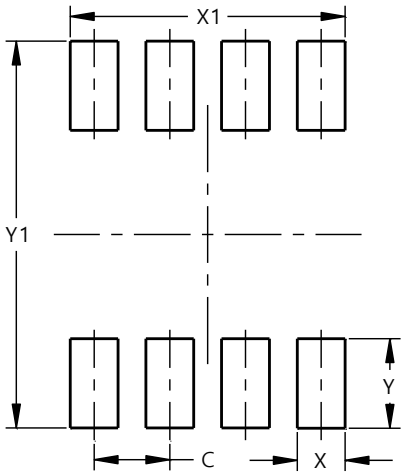
SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50