



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



企业QQ二维码

Product Summary

Device	BV _{DSS}	R _{DS(ON)} Max	I _D MAX T _A = +25°C
Q1 N-Channel	20V	25mΩ @ V _{GS} = 4.5V	6.0A
		35mΩ @ V _{GS} = 2.5V	5.1A
Q2 P-Channel	-20V	75mΩ @ V _{GS} = -4.5V	-3.5A
		140mΩ @ V _{GS} = -2.5V	-2.5A

Features

- PCB Footprint of 4mm²
- Low On-Resistance
- Low Input Capacitance
- Low Profile, 0.6mm Maximum Height
- ESD Protected Gate

Description and Applications

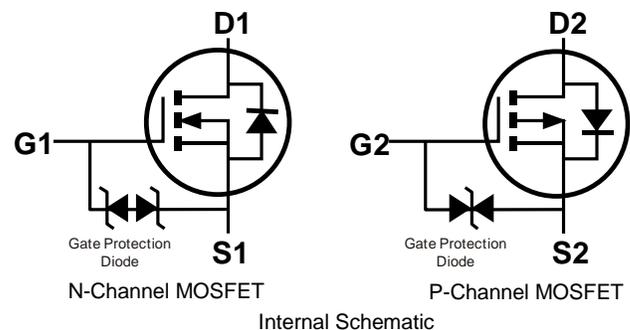
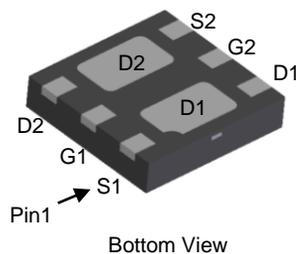
This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, which makes it ideal for high-efficiency power management applications.

- Load Switch
- Power Management Functions
- Portable Power Adaptors

Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound.
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe.
Solderable per MIL-STD-202, Method 208 
- Terminals Connections: See Diagram Below
- Weight: 0.0065 grams (Approximate)

U-DFN2020-6 (Type B)



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Q1 N-CHANNEL	Q2 P-CHANNEL	Unit
Drain-Source Voltage			V_{DSS}	20	-20	V
Gate-Source Voltage			V_{GSS}	± 10	± 8	V
Continuous Drain Current (Note 6)	Steady State	$T_A = +25^\circ\text{C}$	I_D	6.0	-3.5	A
		$T_A = +70^\circ\text{C}$		4.8	-2.8	
N-Channel: $V_{GS} = 4.5\text{V}$						
P-Channel: $V_{GS} = -4.5\text{V}$						
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	2	-1.0	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	20	-10	A
Avalanche Current (L = 0.1mH) (Note 7)			I_{AS}	8	-13	A
Avalanche Energy (L = 0.1mH) (Note 7)			E_{AS}	8	8.5	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.7	W
	Steady State	$R_{\theta JA}$	178	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (Note 5)				
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.4	W
	Steady State	$R_{\theta JA}$	92	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (Note 6)				
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	30	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics Q1 N-CHANNEL (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1	μA	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	25	m Ω	$V_{GS} = 4.5\text{V}, I_D = 4\text{A}$
		—	—	35		$V_{GS} = 2.5\text{V}, I_D = 4\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 5\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	486	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	92	—		
Reverse Transfer Capacitance	C_{rss}	—	77	—		
Gate Resistance	R_g	—	3.2	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	5.9	—	nC	$V_{DS} = 10\text{V}, I_D = 6.5\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	12.3	—		
Gate-Source Charge	Q_{gs}	—	0.8	—		
Gate-Drain Charge	Q_{gd}	—	2.2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	3.4	—	ns	$V_{DS} = 10\text{V}, V_{GS} = 4.5\text{V}, R_g = 6\Omega, R_L = 10\Omega, I_D = 1\text{A}$
Turn-On Rise Time	t_r	—	5.4	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	17.6	—		
Turn-Off Fall Time	t_f	—	9.3	—		
Reverse Recovery Time	t_{RR}	—	7.7	—	ns	$I_F = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	1.5	—	nC	$I_F = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PCB, 2oz copper, with 1inch square copper plate.
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

Electrical Characteristics Q2 P-CHANNEL (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.35	—	-1.4	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	75	m Ω	$V_{GS} = -4.5V, I_D = -2.9A$
		—	—	140		$V_{GS} = -2.5V, I_D = -2.3A$
Diode Forward Voltage	V_{SD}	—	—	-1.2	V	$V_{GS} = 0V, I_S = -3.0A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	642	—	pF	$V_{DS} = -10V, V_{GS} = 0V,$ $f = 1.0MHz$
Output Capacitance	C_{oss}	—	98	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	87	—	pF	
Gate Resistance	R_g	—	26.5	—	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge ($V_{GS} = -4.5V$)	Q_g	—	8.8	—	nC	$V_{DS} = -10V, I_D = -3.7A$
Total Gate Charge ($V_{GS} = -8V$)		—	15	—	nC	
Gate-Source Charge	Q_{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.9	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.5	—	ns	$V_{DD} = -10V, V_{GS} = -4.5V,$ $R_L = 3.3\Omega, R_g = 1\Omega$
Turn-On Rise Time	t_R	—	22.6	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	34.1	—	ns	
Turn-Off Fall Time	t_F	—	34.3	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	13	—	ns	$I_S = -3.0A, di/dt = 100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{RR}	—	3.3	—	nC	$I_S = -3.0A, di/dt = 100A/\mu s$

Notes: 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.

Typical Characteristics - N-CHANNEL

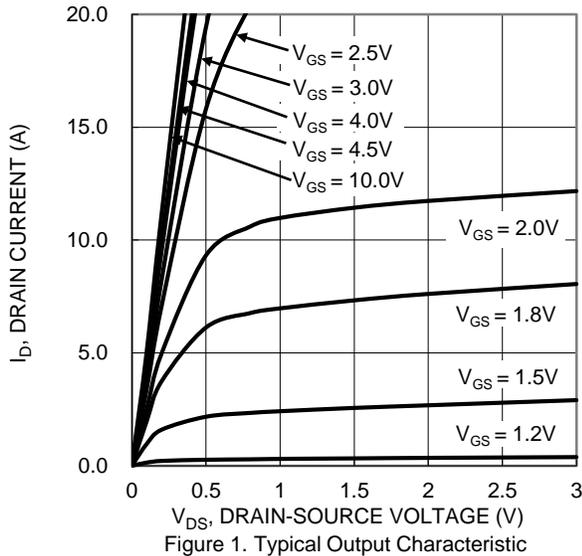


Figure 1. Typical Output Characteristic

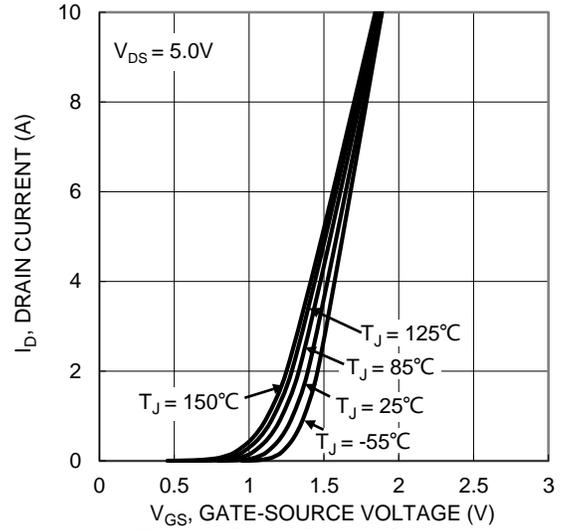


Figure 2. Typical Transfer Characteristic

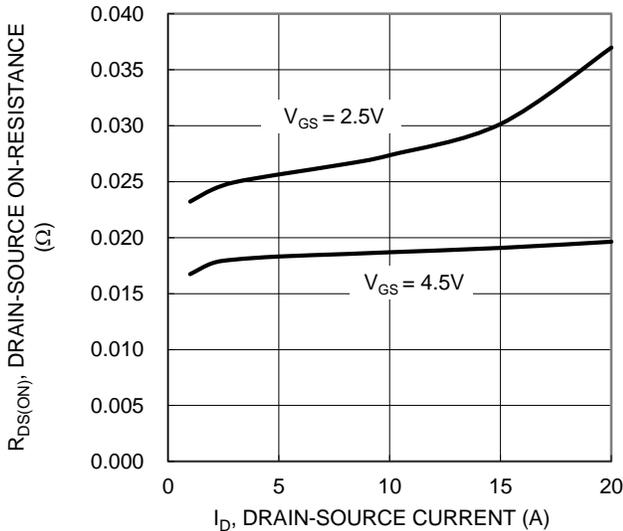


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

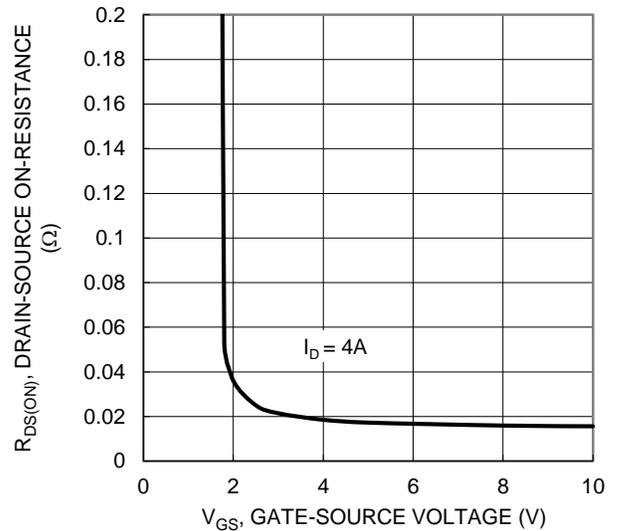


Figure 4. Typical Transfer Characteristic

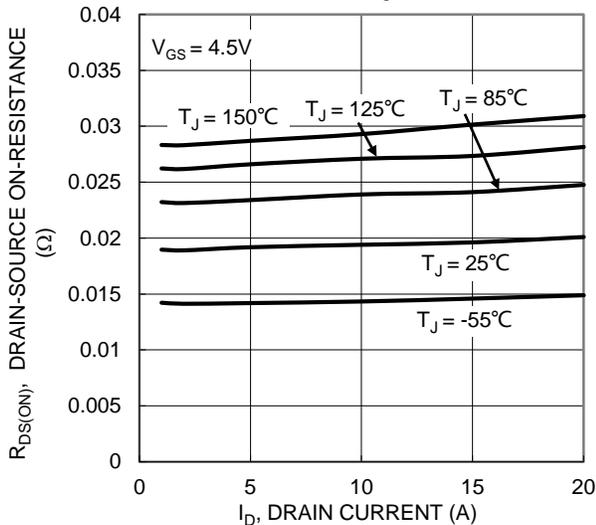


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

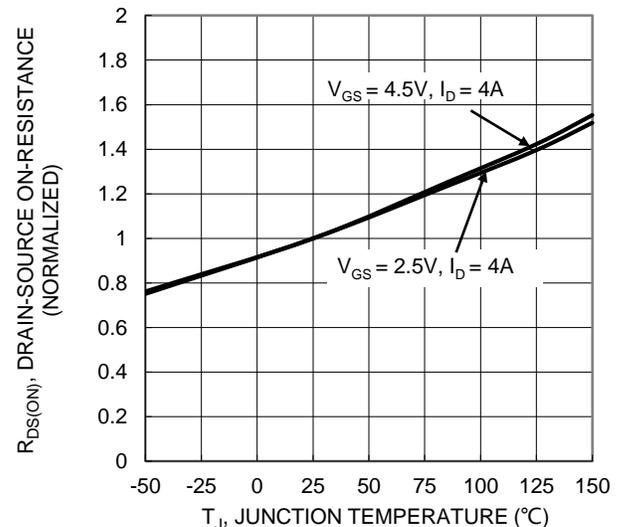


Figure 6. On-Resistance Variation with Temperature

Typical Characteristics - N-CHANNEL (continued)

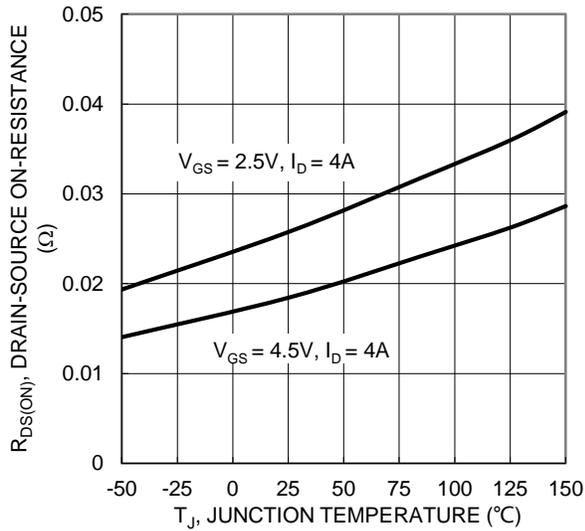


Figure 7. On-Resistance Variation with Temperature

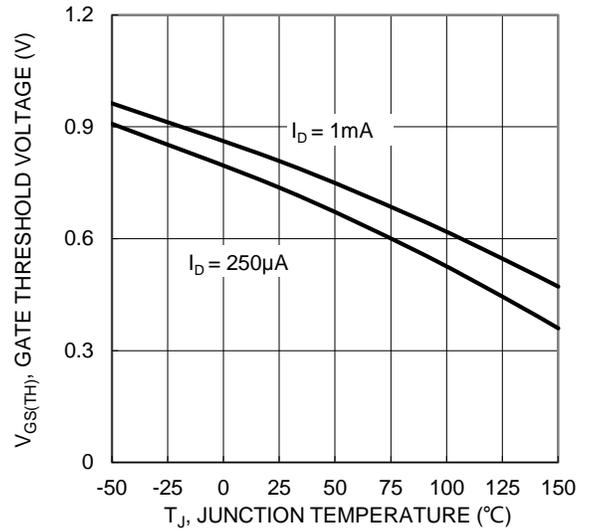


Figure 8. Gate Threshold Variation vs. Junction Temperature

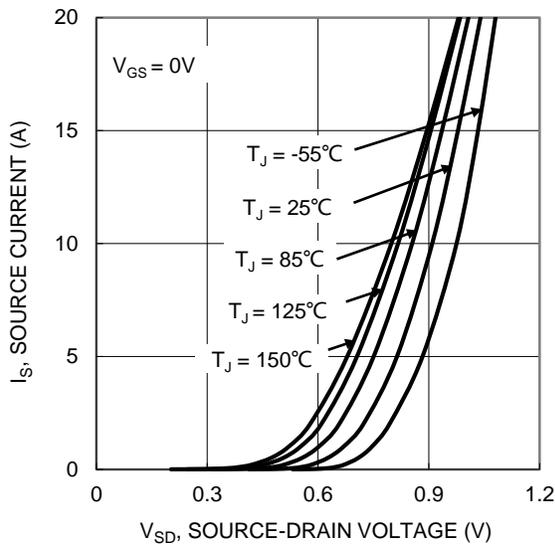


Figure 9. Diode Forward Voltage vs. Current

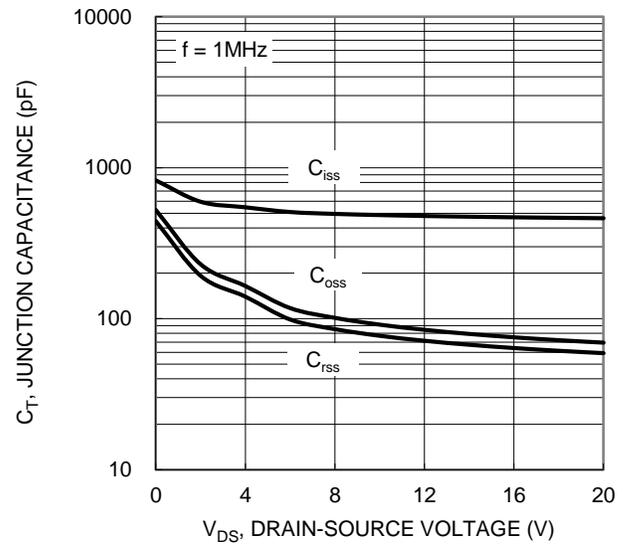


Figure 10. Typical Junction Capacitance

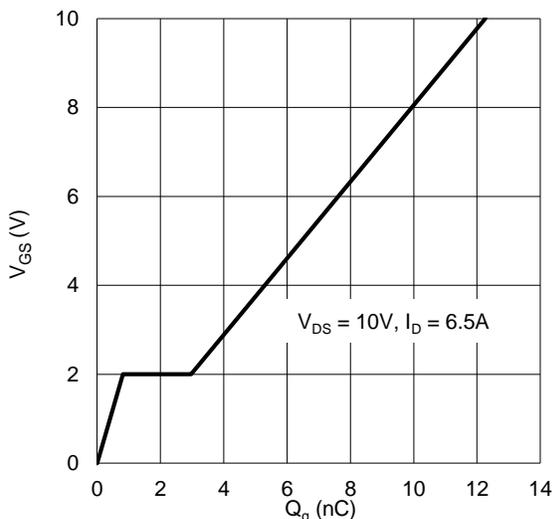


Figure 11. Gate Charge

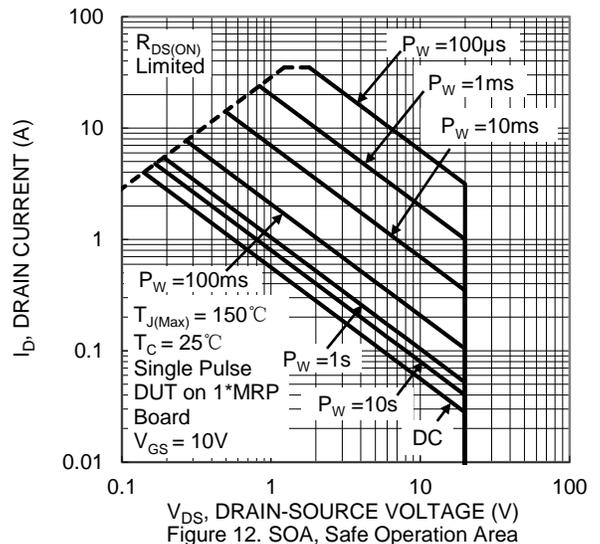


Figure 12. SOA, Safe Operation Area

Typical Characteristics - P-CHANNEL

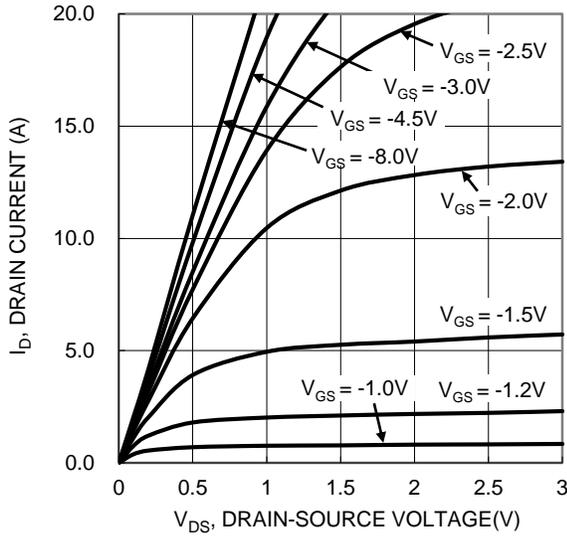


Figure 13. Typical Output Characteristic

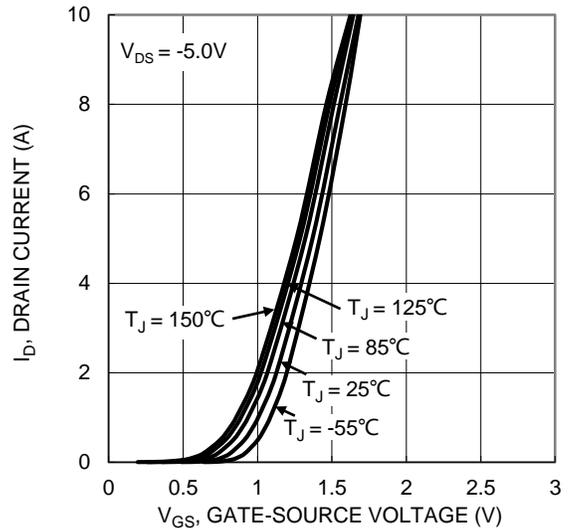


Figure 14. Typical Transfer Characteristic

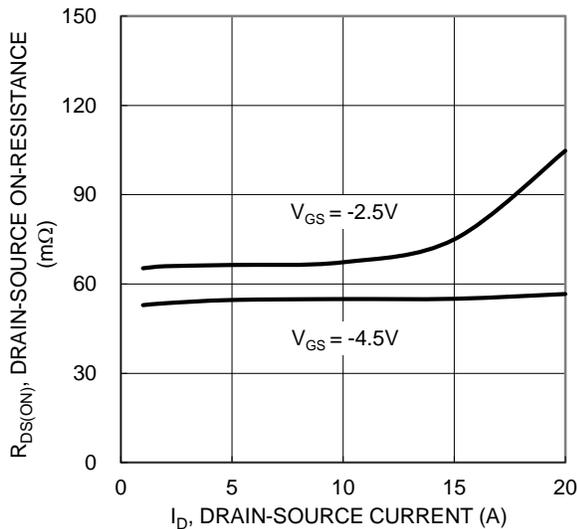


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

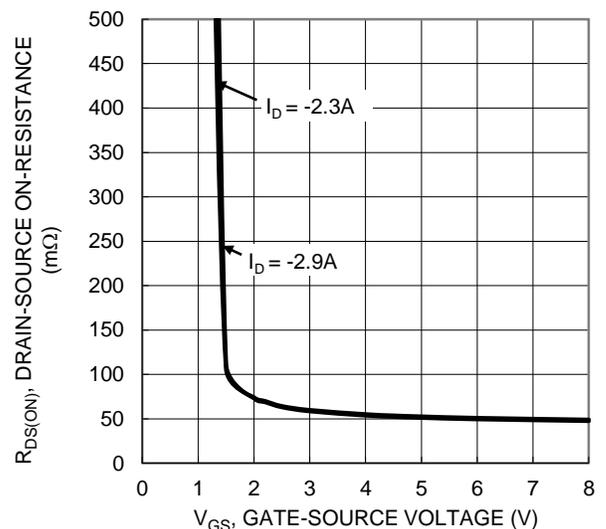


Figure 16. Typical Transfer Characteristic

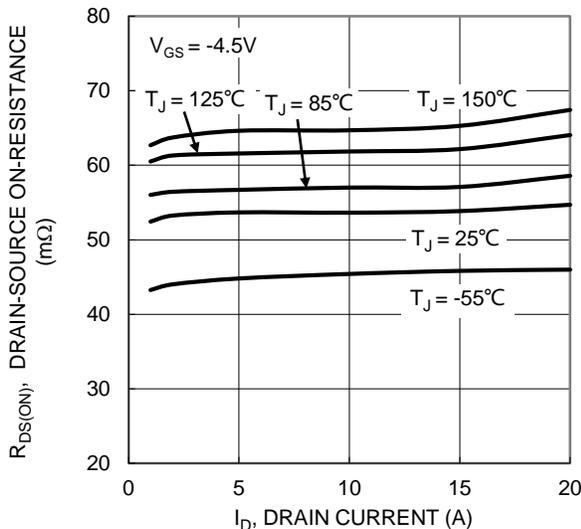


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

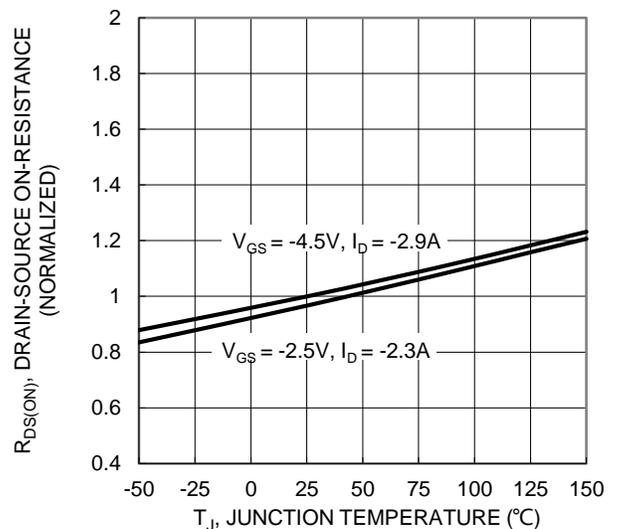


Figure 18. On-Resistance Variation with Temperature

Typical Characteristics - P-CHANNEL (continued)

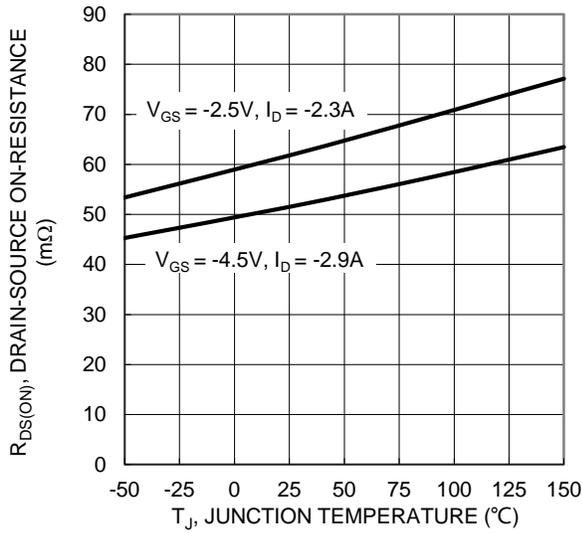


Figure 19. On-Resistance Variation with Temperature

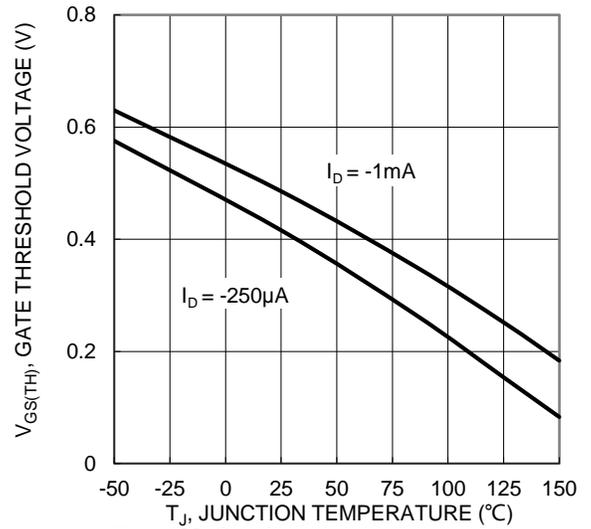


Figure 20. Gate Threshold Variation vs. Junction Temperature

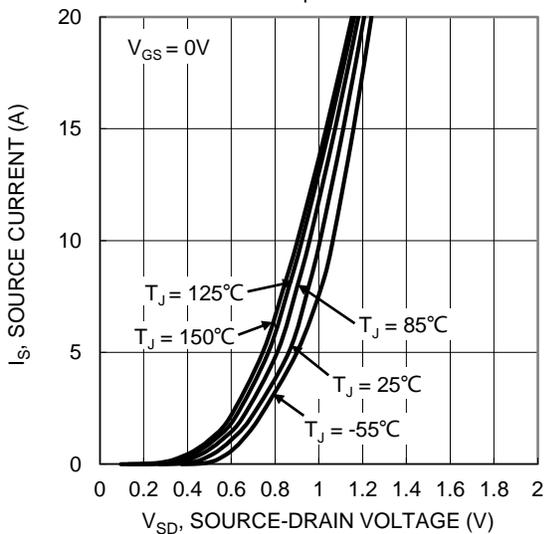


Figure 21. Diode Forward Voltage vs. Current

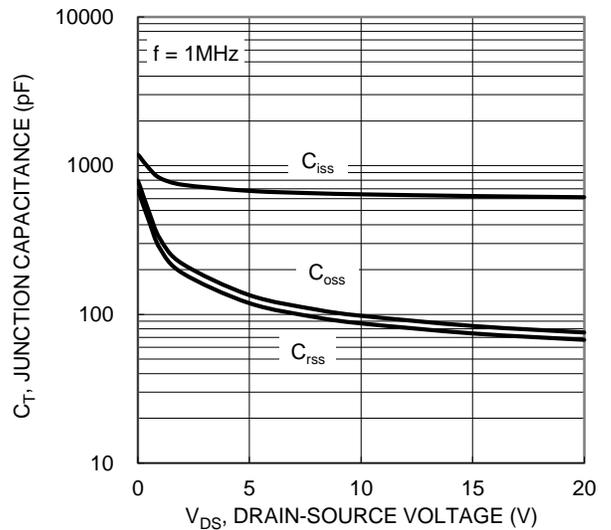


Figure 22. Typical Junction Capacitance

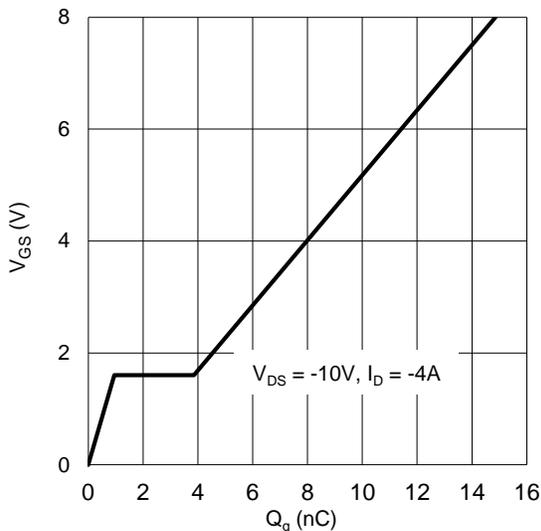


Figure 23. Gate Charge

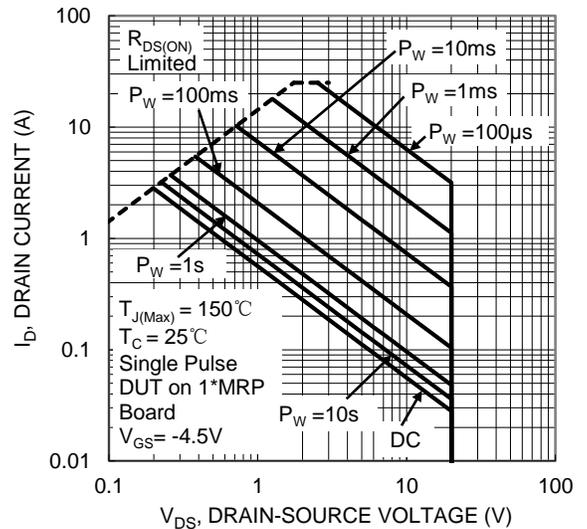


Figure 24. SOA, Safe Operation Area

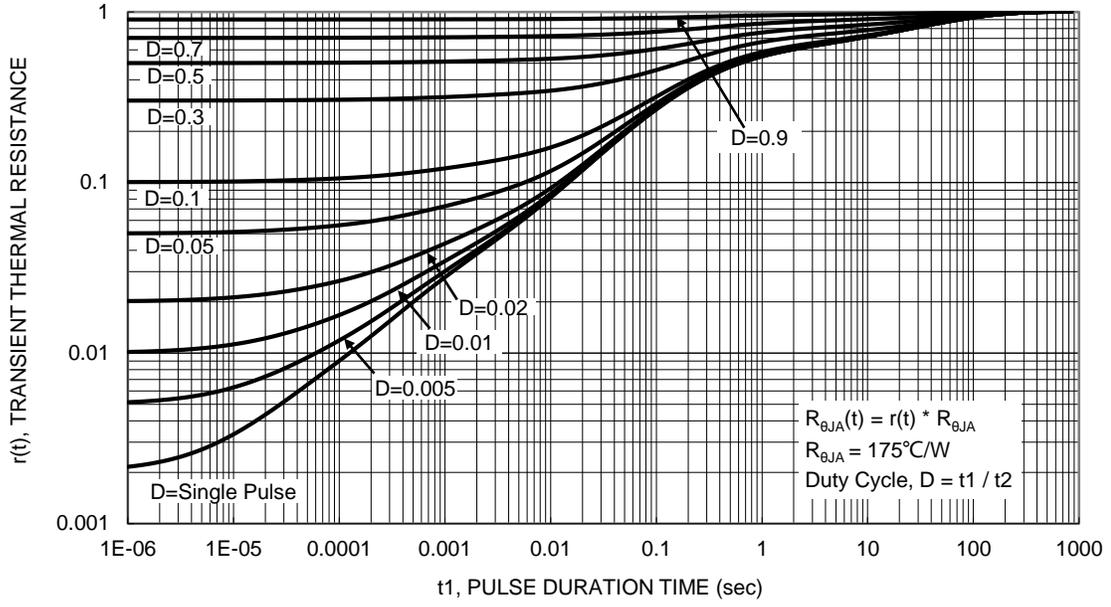
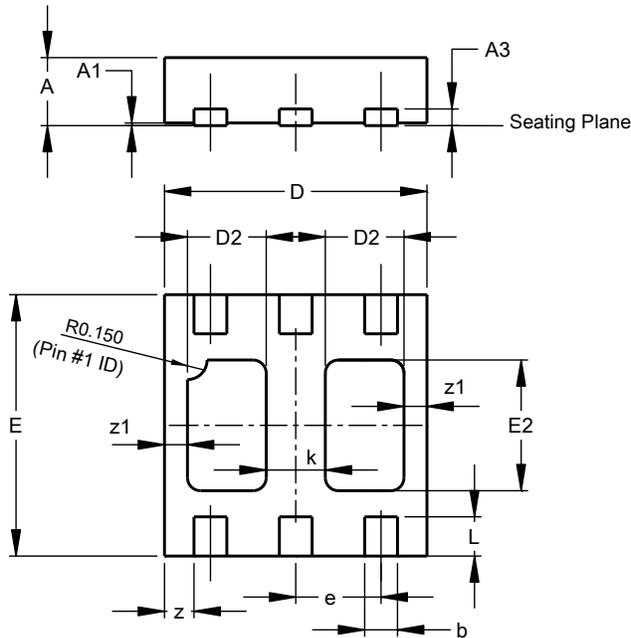


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

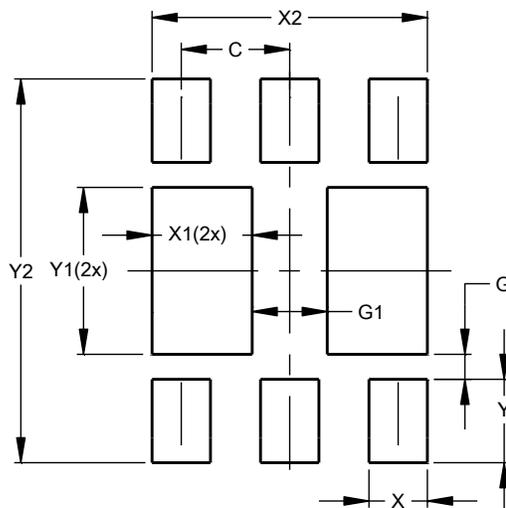
U-DFN2020-6 (Type B)



U-DFN2020-6 Type B			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0.00	0.05	0.02
A3	—	—	0.13
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	0.50	0.70	0.60
e	—	—	0.65
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
k	—	—	0.45
L	0.25	0.35	0.30
z	—	—	0.225
z1	—	—	0.175
All Dimensions in mm			

Suggested Pad Layout

U-DFN2020-6 (Type B)



Dimensions	Value (in mm)
C	0.650
G	0.150
G1	0.450
X	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2.300