



YOUSHANG SEMICONDUCTOR

**设计研发新型功率器件**

**各类小信号开关**

**中低压及高压大电流等场效应管**

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## Product Summary

Device	$BV_{DSS}$	$R_{DS(ON) MAX}$	$I_D$ $T_A = +25^\circ C$
N-Channel	20V	35m $\Omega$ @ $V_{GS} = 4.5V$	4.6A
		43m $\Omega$ @ $V_{GS} = 2.5V$	4.2A
P-Channel	-20V	74m $\Omega$ @ $V_{GS} = -4.5V$	-3.2A
		110m $\Omega$ @ $V_{GS} = -2.5V$	-2.7A

## Description

This new generation MOSFET is designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## Applications

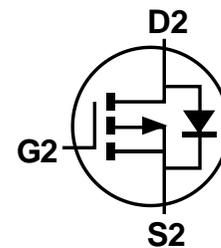
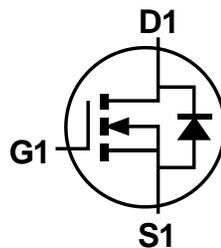
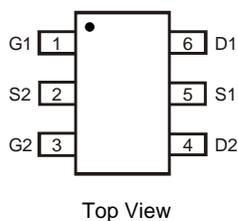
- Backlighting
- DC-DC Converters
- Power Management Functions

## Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

## Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.013 grams (Approximate)



**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Q1 Value	Q2 Value	Unit
Drain-Source Voltage			$V_{DSS}$	20	-20	V
Gate-Source Voltage			$V_{GSS}$	$\pm 12$	$\pm 12$	V
Continuous Drain Current (Note 6) N-Channel: $V_{GS} = 4.5\text{V}$ P-Channel: $V_{GS} = -4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	$I_D$	4.6	-3.2	A
		$T_A = +70^\circ\text{C}$		3.7	-2.6	
Maximum Continuous Body Diode Forward Current (Note 6)			$I_S$	1.4	-1.3	A
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	22	-20	A

**Thermal Characteristics**

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$		$P_D$	0.7	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		$R_{\theta JA}$	173	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$		$P_D$	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		$R_{\theta JA}$	108	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case			$R_{\theta JC}$	37	
Operating and Storage Temperature Range			$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics Q1 N-CHANNEL** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1.0	$\mu\text{A}$	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	35	m $\Omega$	$V_{GS} = 4.5\text{V}, I_D = 5.0\text{A}$
		—	—	43		$V_{GS} = 2.5\text{V}, I_D = 4.0\text{A}$
		—	—	56		$V_{GS} = 1.8\text{V}, I_D = 2.0\text{A}$
Diode Forward Voltage	$V_{SD}$	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	$C_{iss}$	—	369	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	—	54	—		
Reverse Transfer Capacitance	$C_{rss}$	—	32	—		
Gate Resistance	$R_g$	—	4.1	—	$\Omega$	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ( $V_{GS} = 4.5\text{V}$ )	$Q_g$	—	3.6	—	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V}, I_D = 6\text{A}$
Gate-Source Charge	$Q_{gs}$	—	0.4	—		
Gate-Drain Charge	$Q_{gd}$	—	1.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	2.6	—	ns	$V_{DS} = 10\text{V}, V_{GS} = 5\text{V},$ $R_G = 6\Omega, I_D = 6\text{A}$
Turn-On Rise Time	$t_R$	—	3.0	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	12.5	—		
Turn-Off Fall Time	$t_F$	—	3.6	—		
Reverse Recovery Time	$t_{RR}$	—	6.0	—	ns	$I_F = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{RR}$	—	0.9	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

**Electrical Characteristics Q2 P-CHANNEL** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1.0	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.45	—	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	—	74	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.5A
				110		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.0A
				168		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -2.0A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.8	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	440	—	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	60	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	48	—		
Gate Resistance	R <sub>g</sub>	—	8.5	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	5.9	—	nC	V <sub>DS</sub> = -4V, I <sub>D</sub> = -3.5A
Gate-Source Charge	Q <sub>gs</sub>	—	0.6	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	2.1	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	3.2	—	ns	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -4V, R <sub>G</sub> = 6Ω, R <sub>L</sub> = 4Ω
Turn-On Rise Time	t <sub>R</sub>	—	7.8	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	31	—		
Turn-Off Fall Time	t <sub>F</sub>	—	18	—		
Reverse Recovery Time	t <sub>RR</sub>	—	10.5	—	ns	I <sub>F</sub> = -2.0A, di/dt = -100A/μs
Reverse Recovery Charge	Q <sub>RR</sub>	—	3.0	—	nC	I <sub>F</sub> = -2.0A, di/dt = -100A/μs

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
 8. Guaranteed by design. Not subject to production testing.

**Typical Characteristics - N-CHANNEL**

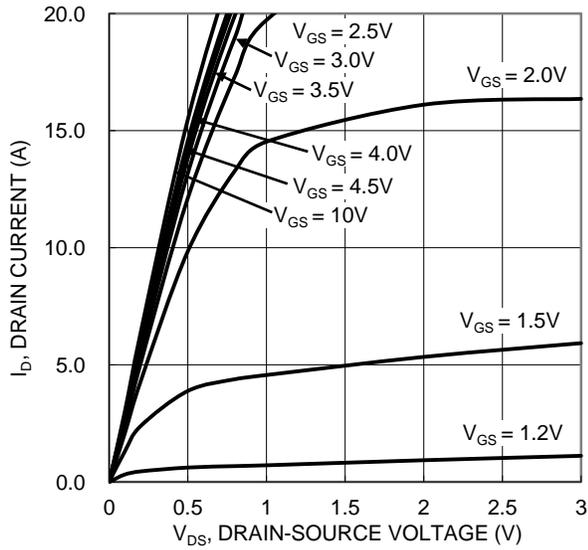


Figure 1. Typical Output Characteristic

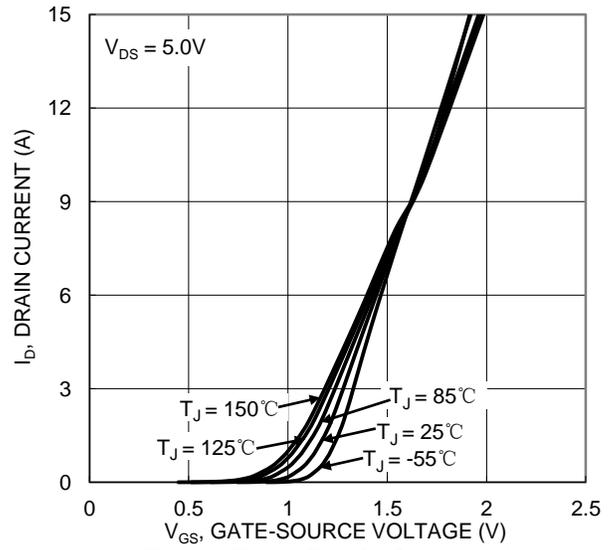


Figure 2. Typical Transfer Characteristic

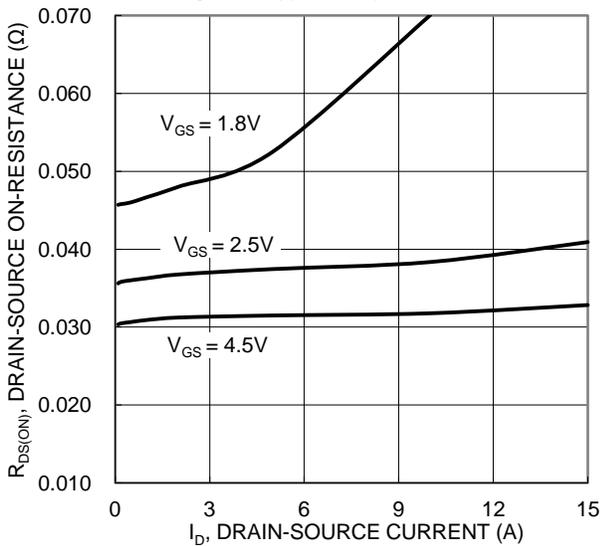


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

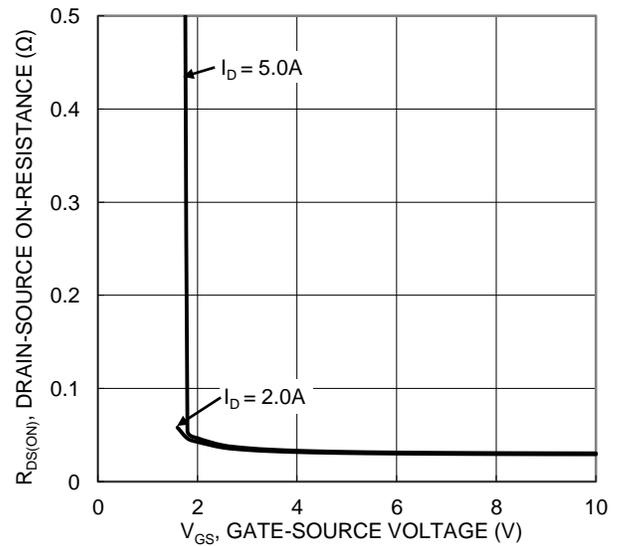


Figure 4. Typical Transfer Characteristic

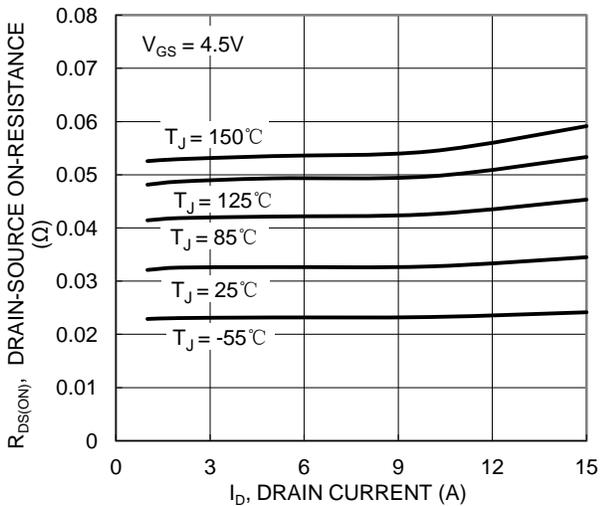


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

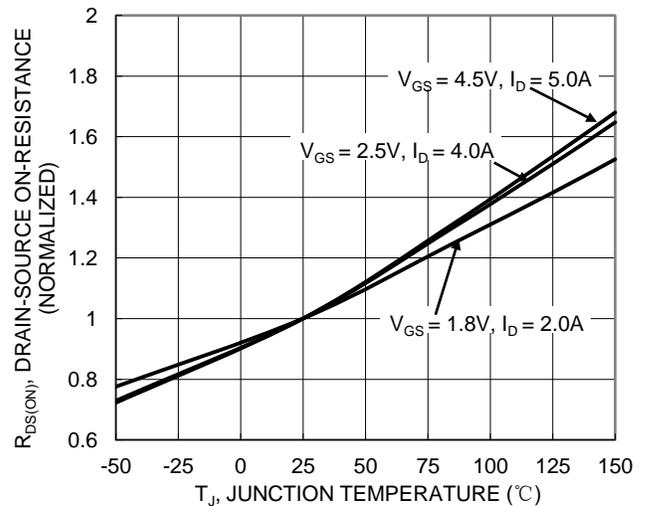


Figure 6. On-Resistance Variation with Temperature

**Typical Characteristics - N-CHANNEL** (continued)

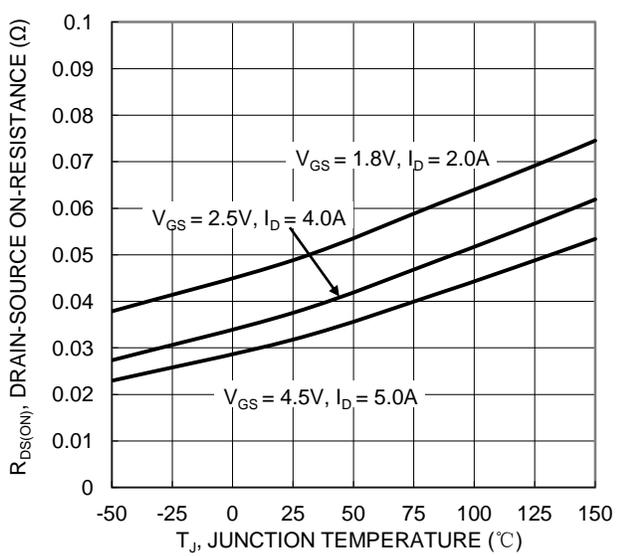


Figure 7. On-Resistance Variation with Temperature

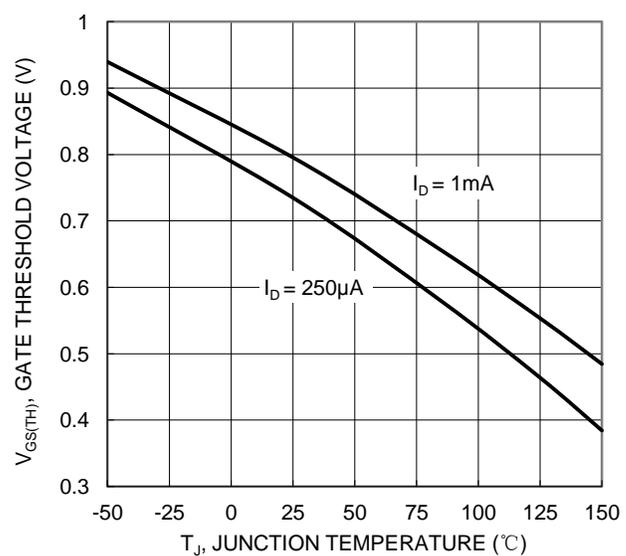


Figure 8. Gate Threshold Variation vs. Junction Temperature

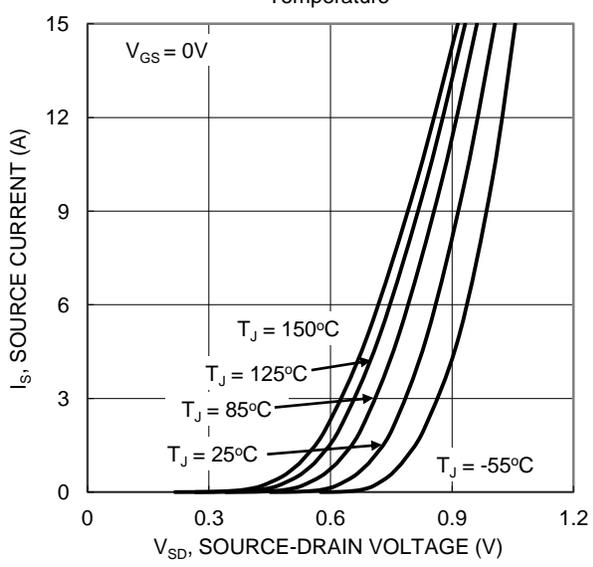


Figure 9. Diode Forward Voltage vs. Current

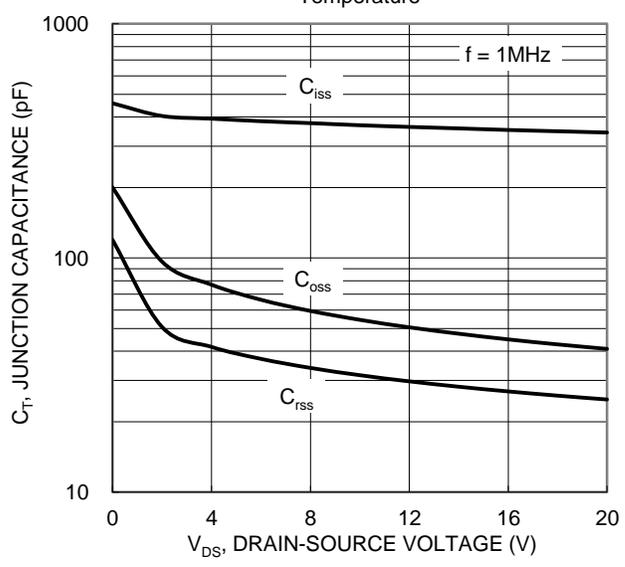


Figure 10. Typical Junction Capacitance

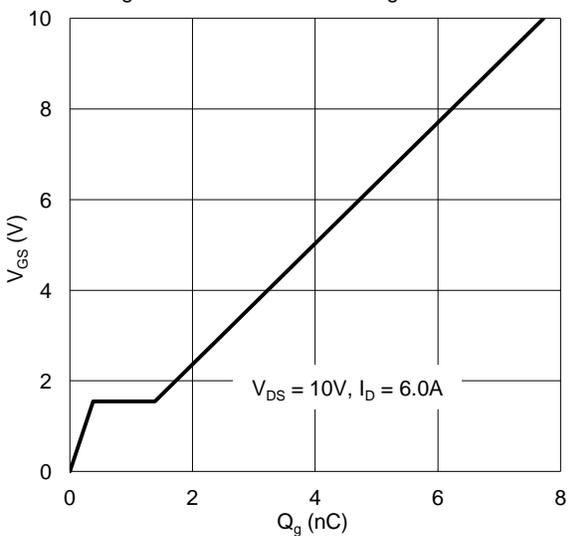


Figure 11. Gate Charge

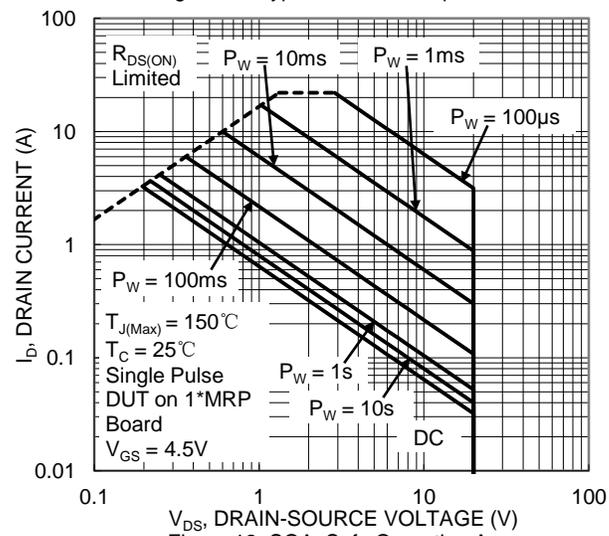


Figure 12. SOA, Safe Operation Area

**Typical Characteristics - P-CHANNEL**

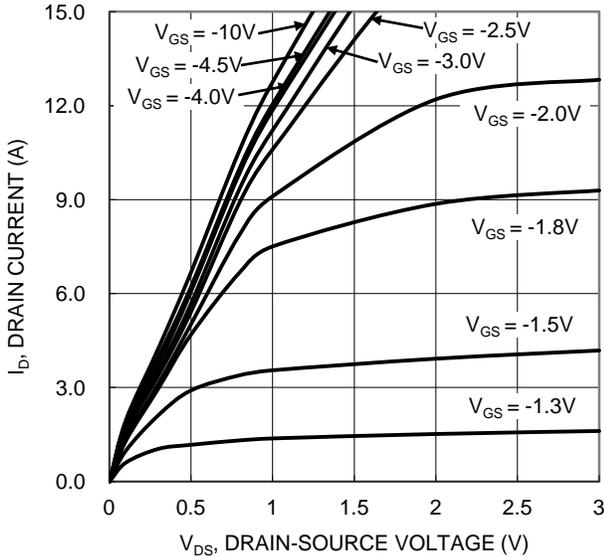


Figure 13. Typical Output Characteristic

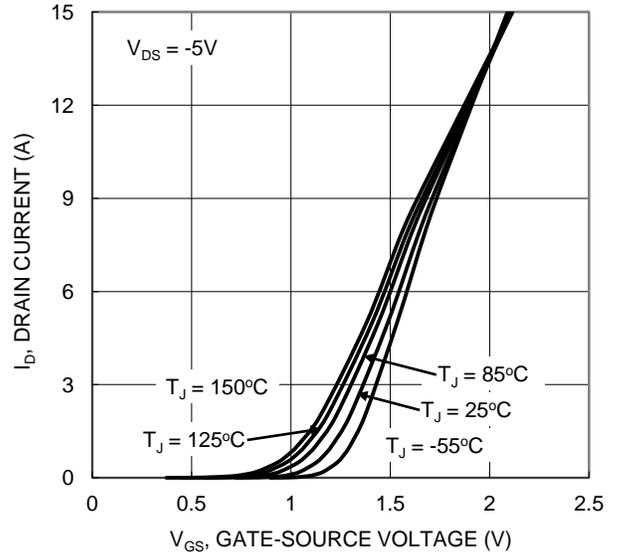


Figure 14. Typical Transfer Characteristic

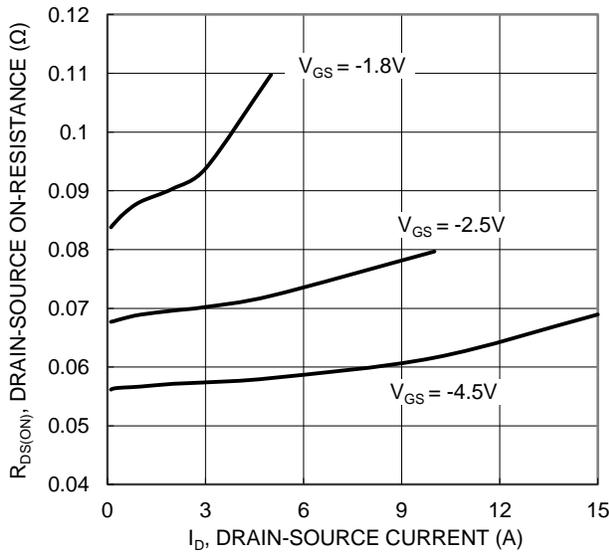


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

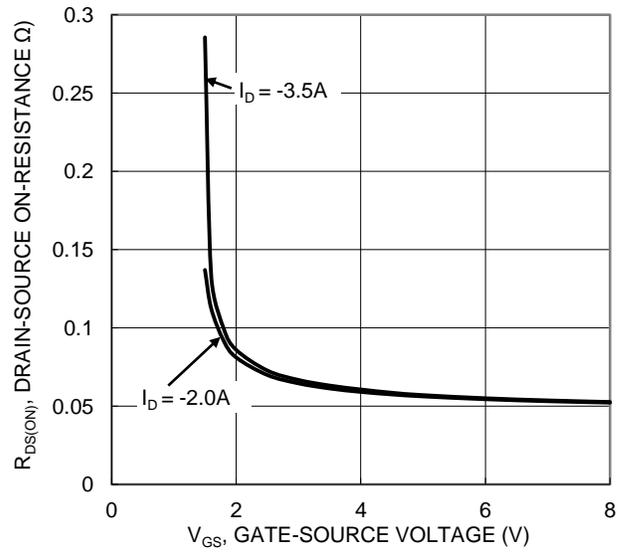


Figure 16. Typical Transfer Characteristic

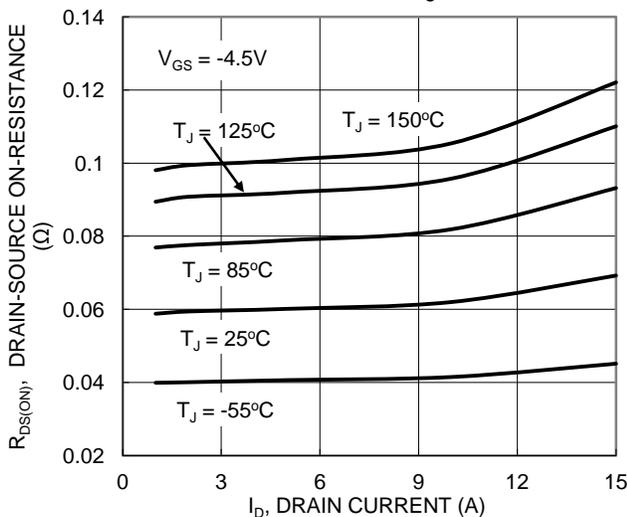


Figure 17. Typical On-Resistance vs. Drain Current and Junction Temperature

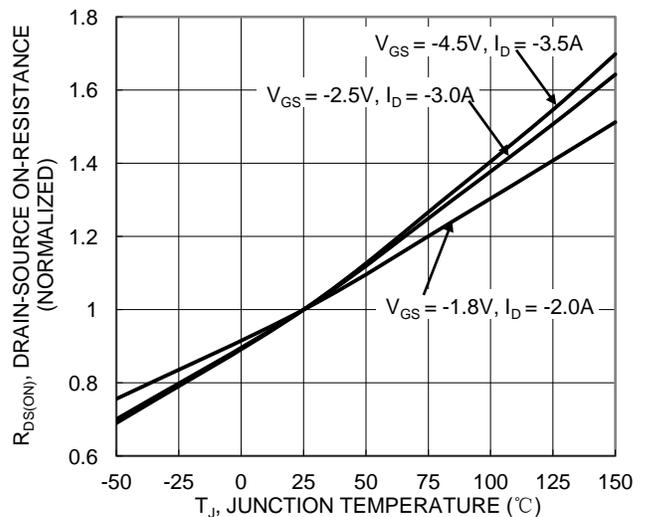


Figure 18. On-Resistance Variation with Junction Temperature

Typical Characteristics - P-CHANNEL (continued)

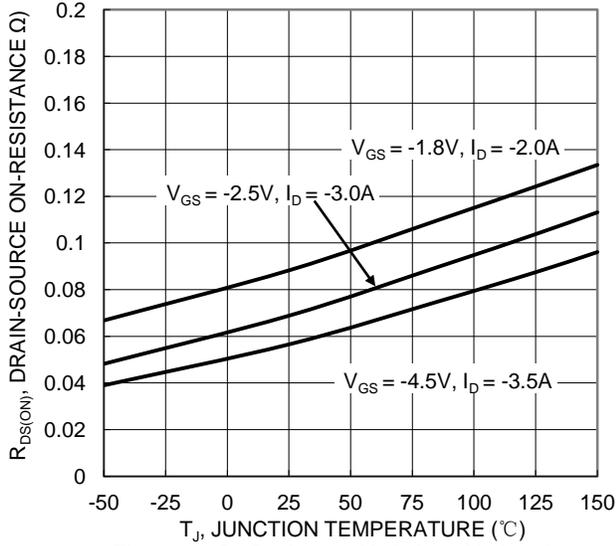


Figure 19. On-Resistance Variation with Junction Temperature

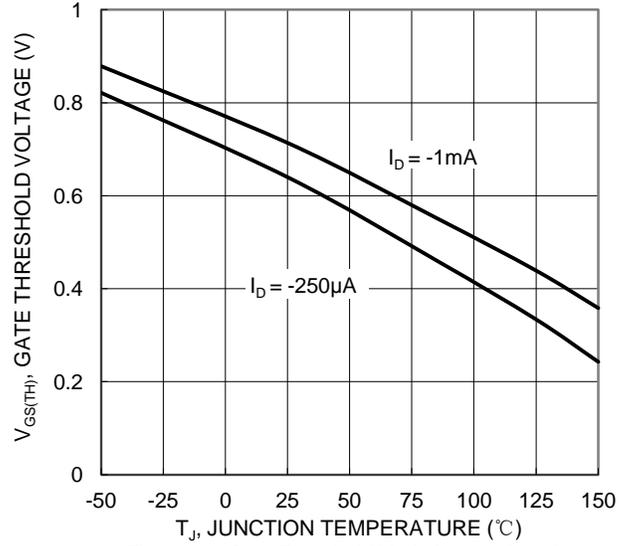


Figure 20. Gate Threshold Variation vs. Junction Temperature

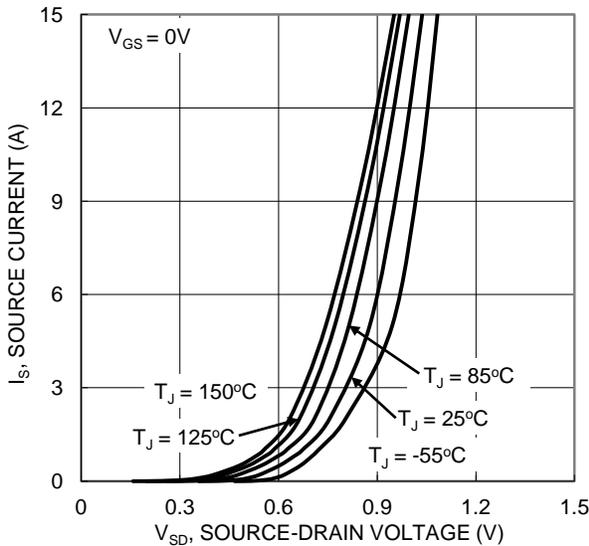


Figure 21. Diode Forward Voltage vs. Current

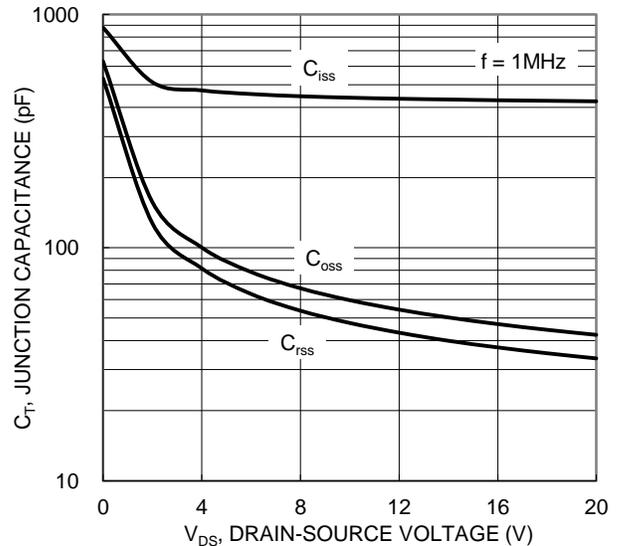


Figure 22. Typical Junction Capacitance

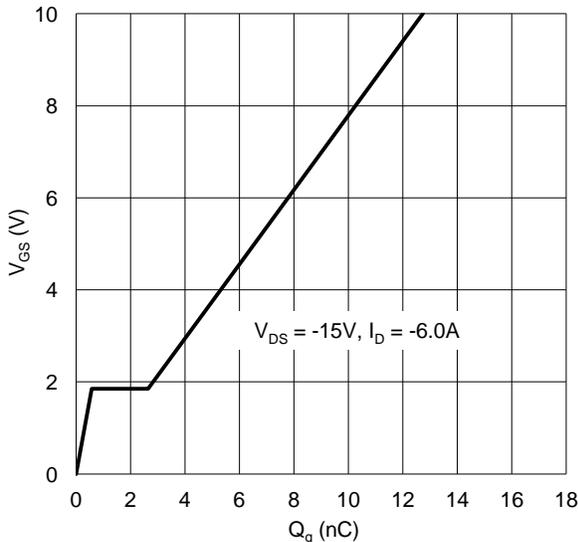


Figure 23. Gate Charge

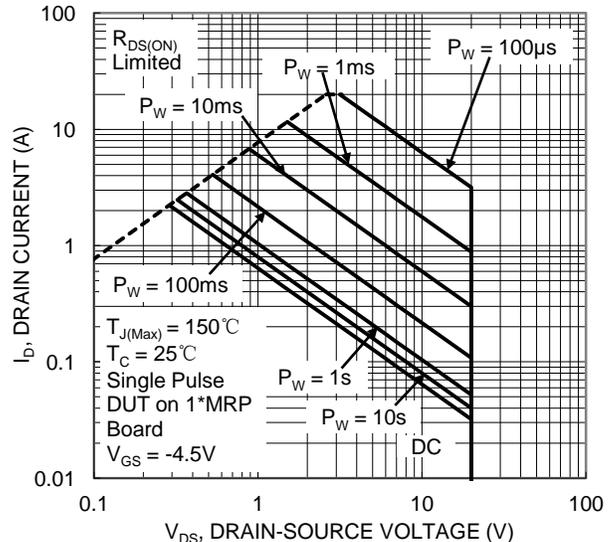


Figure 24. SOA, Safe Operation Area

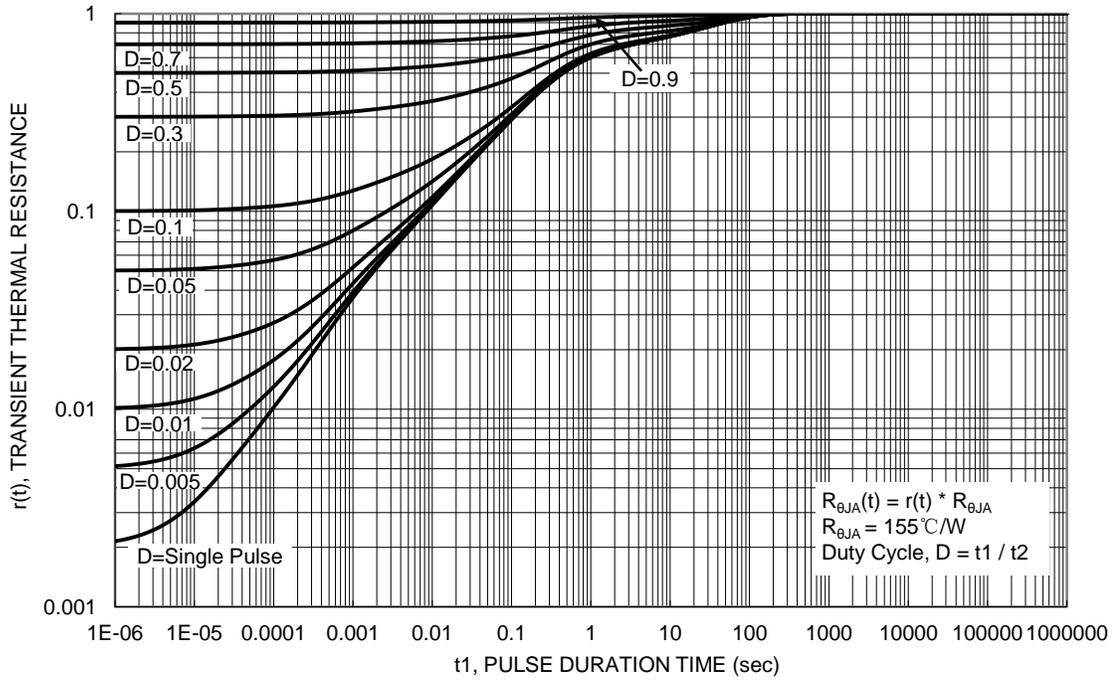
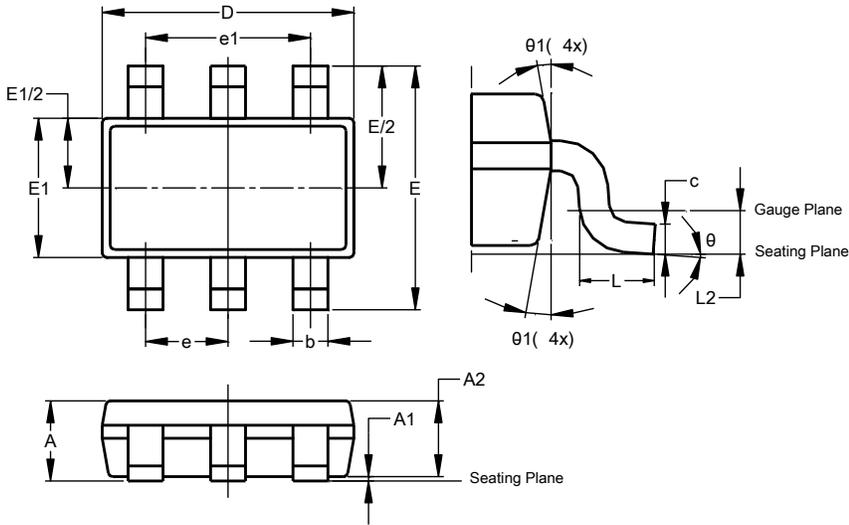


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

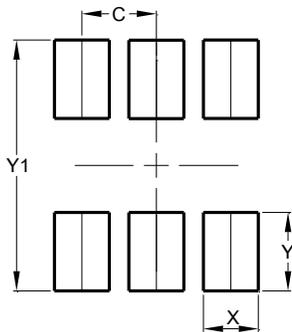
TSOT26



TSOT26			
Dim	Min	Max	Typ
A	-	1.00	-
A1	0.010	0.100	-
A2	0.840	0.900	-
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	-
c	0.120	0.200	-
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	-
L2	0.250 BSC		
$\theta$	0°	8°	4°
$\theta1$	4°	12°	-
All Dimensions in mm			

Suggested Pad Layout

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199