



YOUSHANG SEMICONDUCTOR

**设计研发新型功率器件**

**各类小信号开关**

**中低压及高压大电流等场效应管**

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企业微信二维码



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## Product Summary

Device	V <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C
Q1	30V	31mΩ @ V <sub>GS</sub> = 10V	20A
		40mΩ @ V <sub>GS</sub> = 4.5V	18A
Q2	-30V	42mΩ @ V <sub>GS</sub> = -10V	-17A
		75mΩ @ V <sub>GS</sub> = -4.5V	-13A

## Features

- Rated to +150°C – Ideal for High Ambient Temperature Environments
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Wettable Flank for Improved Optical Inspection

## Description

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

## Applications

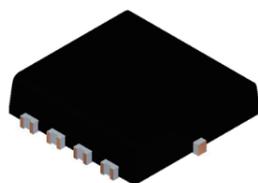
- Power-management functions
- Analog switches

## Mechanical Data

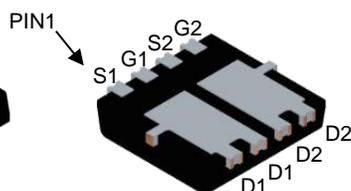
- Package: POWERDI®3333-8
- Package Material: Molded Plastic, “Green” Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.072 grams (Approximate)



POWERDI3333-8/SWP (Type UXD)

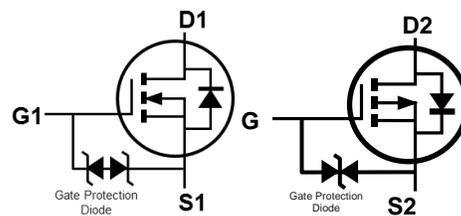


Top View



Bottom View

Equivalent Circuit



N-Channel MOSFET

P-Channel MOSFET

**Maximum Ratings Q1 – N-Channel** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DS}$	30	V
Gate-Source Voltage			$V_{GS}$	$\pm 12$	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6)	Steady State	$T_C = +25^\circ\text{C}$	$I_D$	20	A
		$T_C = +70^\circ\text{C}$		16	
Maximum Body Diode Forward Current (Note 6)			$I_S$	2.2	A
Pulsed Drain Current (380 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	16.7	A
Avalanche Current (L = 0.1mH) (Note 7)			$I_{AS}$	13.5	A
Avalanche Energy (L = 0.1mH) (Note 7)			$E_{AS}$	9.1	mJ

**Maximum Ratings Q2 – P-Channel** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DS}$	-30	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current, $V_{GS} = -10\text{V}$ (Note 6)	Steady State	$T_C = +25^\circ\text{C}$	$I_D$	-17	A
		$T_C = +70^\circ\text{C}$		-14	
Maximum Body Diode Forward Current (Note 6)			$I_S$	-2.32	A
Pulsed Drain Current (380 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	-22	A
Avalanche Current (L = 0.1mH) (Note 7)			$I_{AS}$	-19.8	A
Avalanche Energy (L = 0.1mH) (Note 7)			$E_{AS}$	19.7	mJ

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			$P_D$	1.18	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		$R_{\theta JA}$	106	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)			$P_D$	2.21	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		$R_{\theta JA}$	56.6	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 6)			$R_{\theta JC}$	7	$^\circ\text{C/W}$
Operating and Storage Temperature Range			$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
  - $I_{AS}$  and  $E_{AS}$  ratings are based on low frequency and duty cycles to keep  $T_J = +25^\circ\text{C}$ .

**Electrical Characteristics Q1 – N-Channel** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

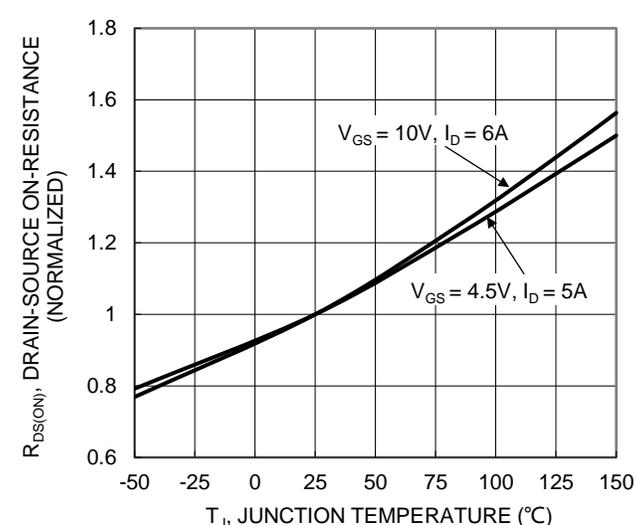
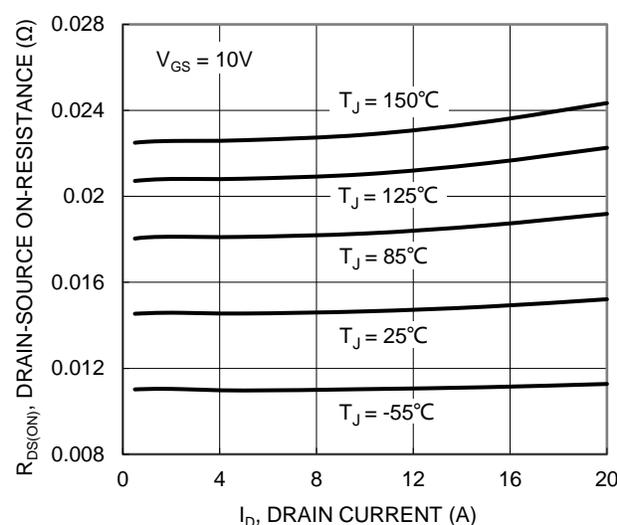
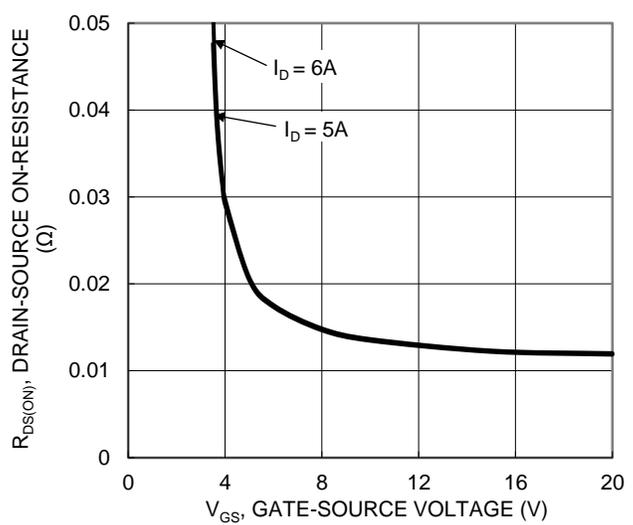
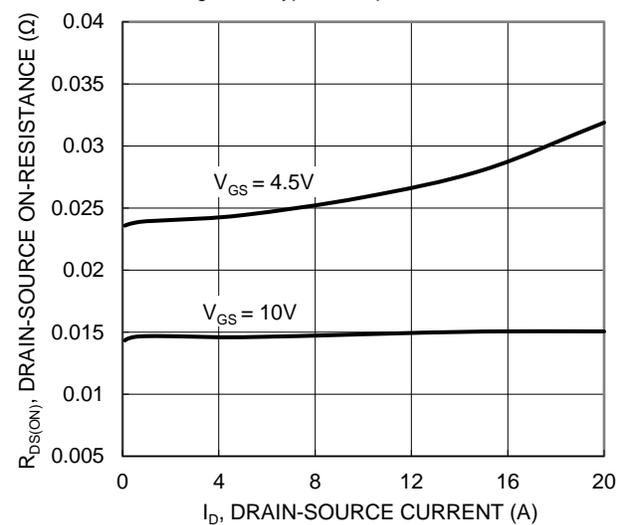
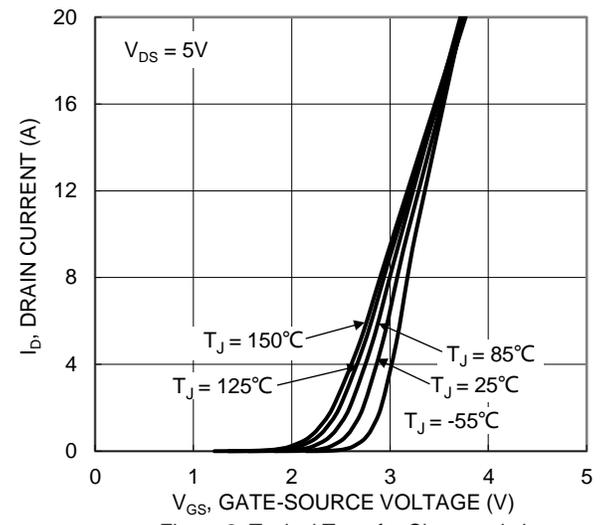
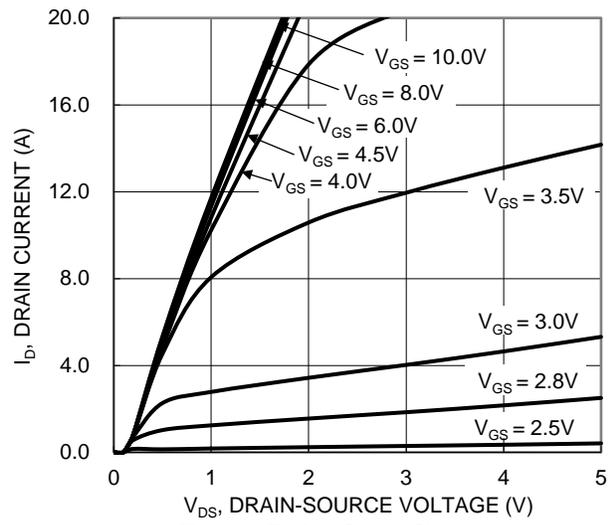
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b> (Note 8)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.4	—	1.85	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	15	31	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.0A
			24	40		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.0A
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2A
<b>DYNAMIC CHARACTERISTICS</b> (Note 9)						
Input Capacitance	C <sub>iss</sub>	—	383	—	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	186	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	41	—		
Gate Resistance	R <sub>g</sub>	—	1.5	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	8.8	—	nC	V <sub>DS</sub> = 15V, I <sub>D</sub> = 6A
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	4.6	—		
Gate-Source Charge	Q <sub>gs</sub>	—	2.1	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	1.6	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	6	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 9A, R <sub>G</sub> = 6Ω
Turn-On Rise Time	t <sub>R</sub>	—	1	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	11	—		
Turn-Off Fall Time	t <sub>F</sub>	—	4	—		

**Electrical Characteristics Q2 – P-Channel** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1.0	μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b> (Note 8)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-1	—	-2.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	31	42	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.9A
			54	75		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.7A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.7	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A
<b>DYNAMIC CHARACTERISTICS</b> (Note 9)						
Input Capacitance	C <sub>iss</sub>	—	782	—	pF	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	110	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	74	—		
Gate Resistance	R <sub>g</sub>	—	10.4	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -10V)	Q <sub>g</sub>	—	13.6	—	nC	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.9A
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	6.6	—		
Gate-Source Charge	Q <sub>gs</sub>	—	2.1	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	2.7	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	4.1	—	ns	V <sub>DD</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.9A, R <sub>G</sub> = 6Ω
Turn-On Rise Time	t <sub>R</sub>	—	6.1	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	24.6	—		
Turn-Off Fall Time	t <sub>F</sub>	—	13.1	—		

- Notes:
8. Short duration pulse test used to minimize self-heating effect.
  9. Guaranteed by design. Not subject to product testing.

**Q1 – N-Channel**



**Q1 – N-Channel** (continued)

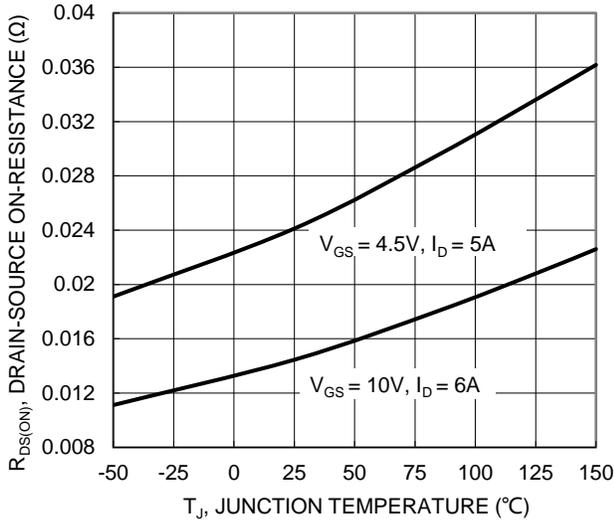


Figure 7. On-Resistance Variation with Junction Temperature

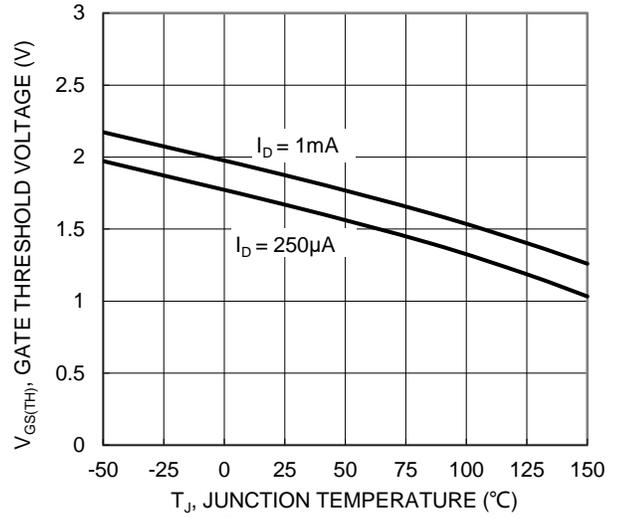


Figure 8. Gate Threshold Variation vs. Junction Temperature

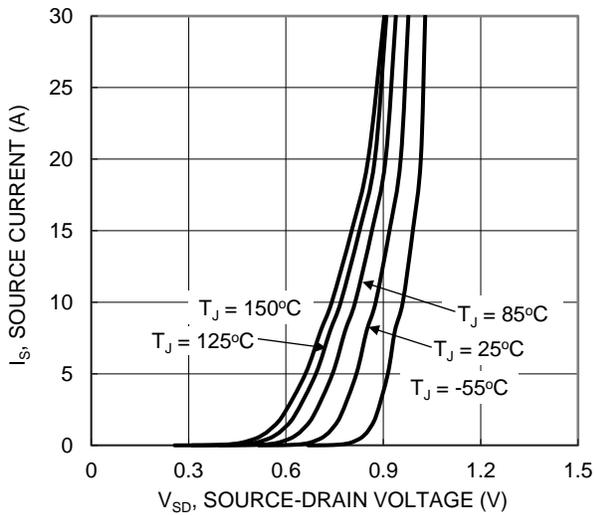


Figure 9. Diode Forward Voltage vs. Current

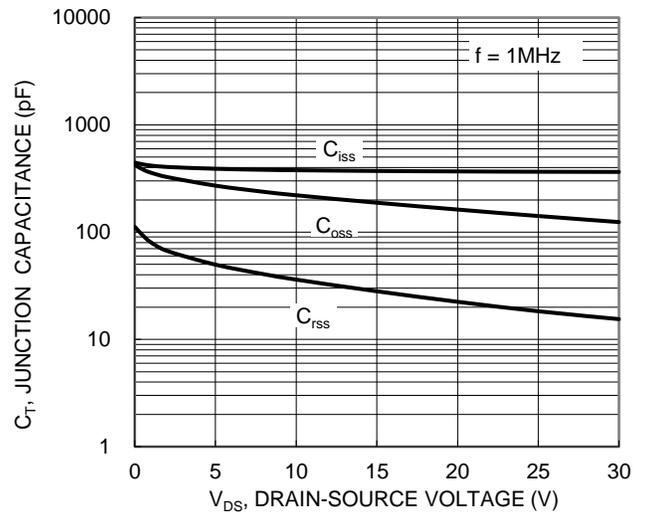


Figure 10. Typical Junction Capacitance

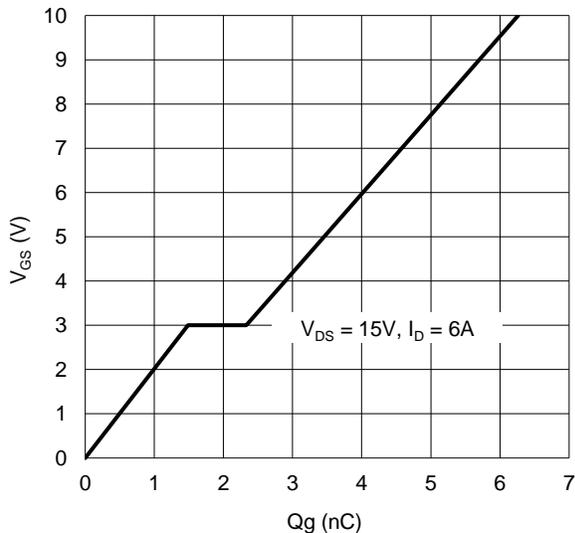


Figure 11. Gate Charge

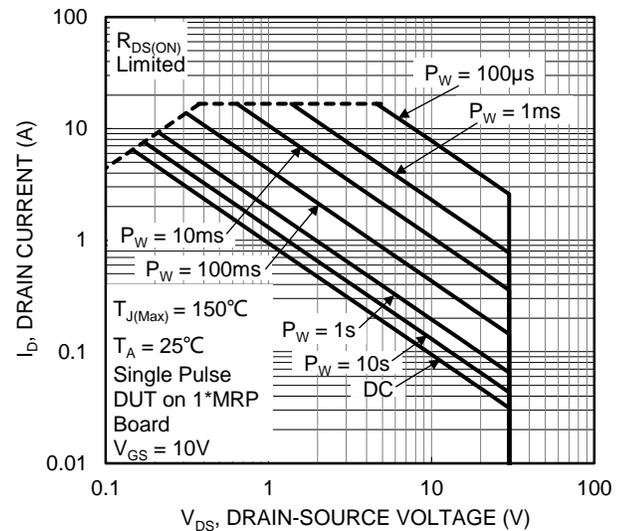


Figure 12. SOA, Safe Operation Area

**Q1 – N-Channel** (continued)

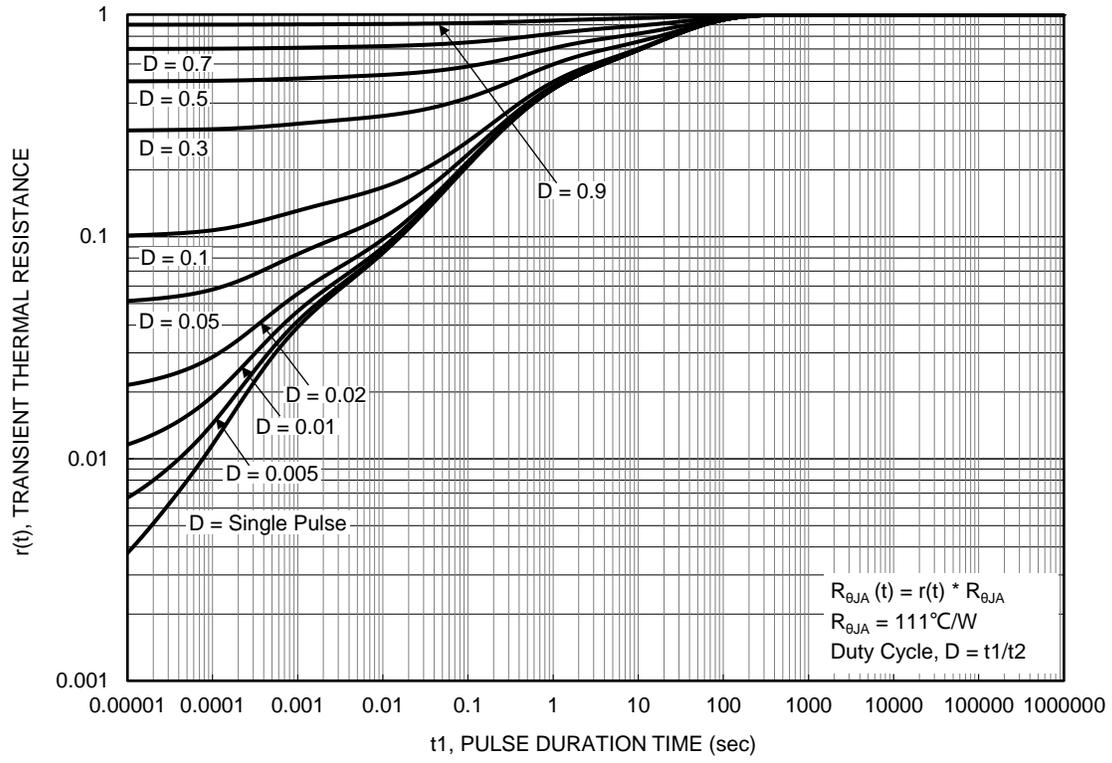


Figure 13. Transient Thermal Resistance

**Q2 – P-Channel**

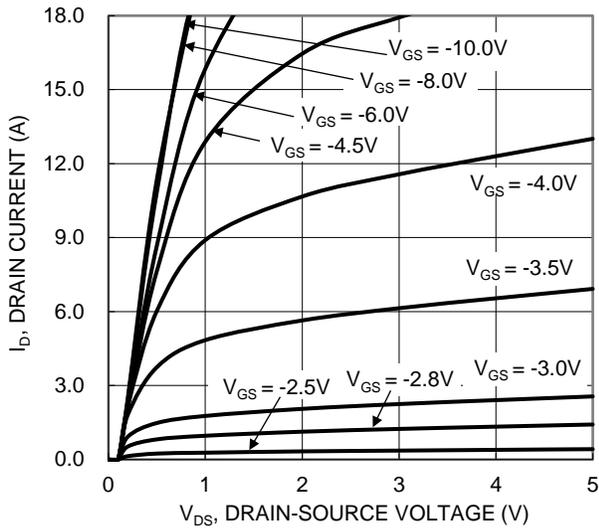


Figure 14. Typical Output Characteristic

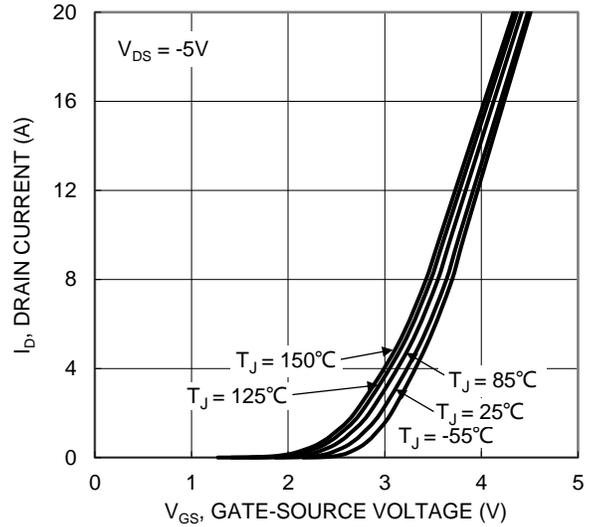


Figure 15. Typical Transfer Characteristic

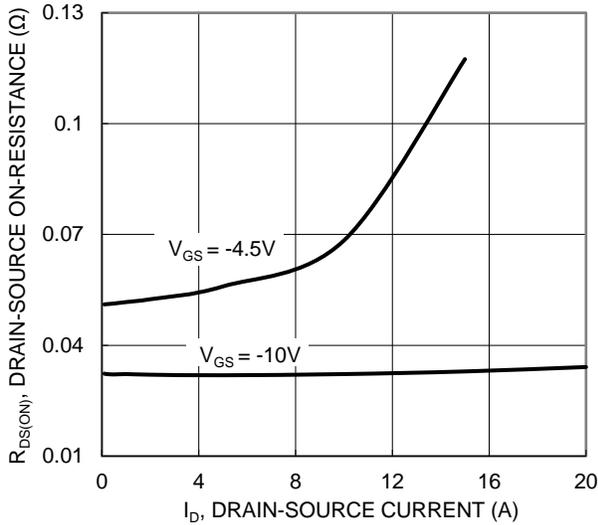


Figure 16. Typical On-Resistance vs. Drain Current and Gate Voltage

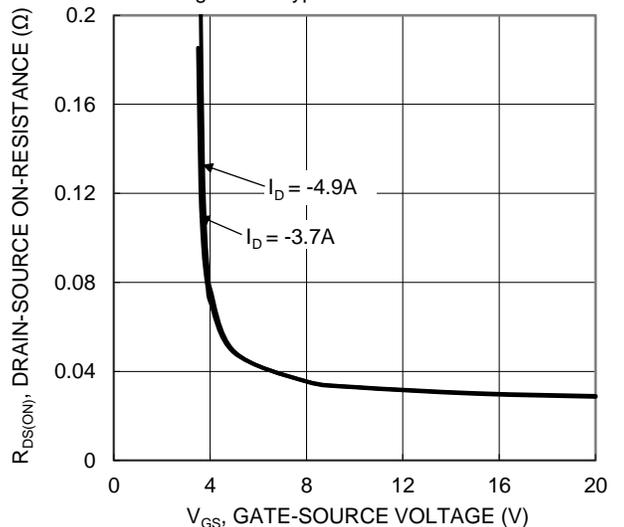


Figure 17. Typical Transfer Characteristic

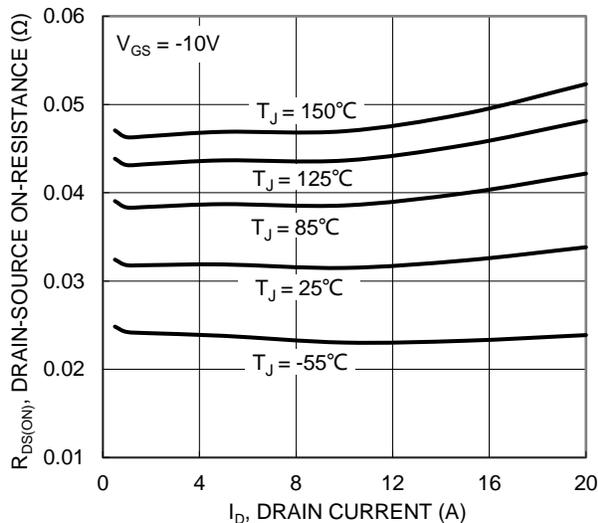


Figure 18. Typical On-Resistance vs. Drain Current and Junction Temperature

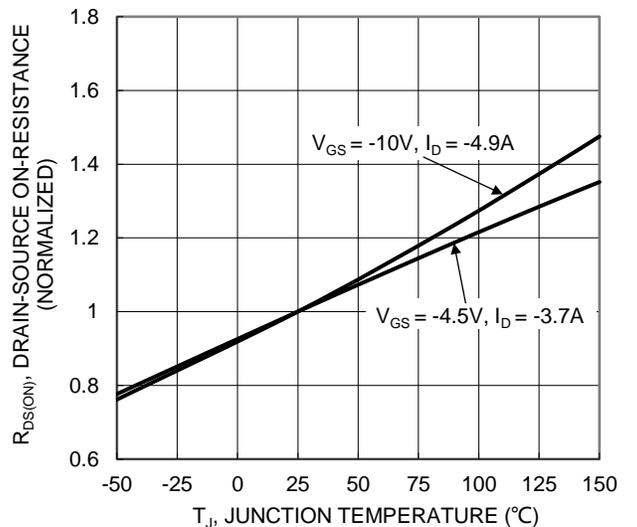


Figure 19. On-Resistance Variation with Junction Temperature

**Q2 – P-Channel** (continued)

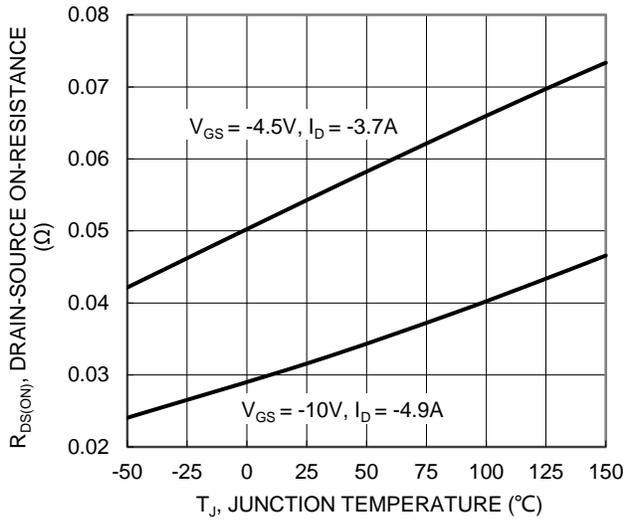


Figure 20. On-Resistance Variation with Junction Temperature

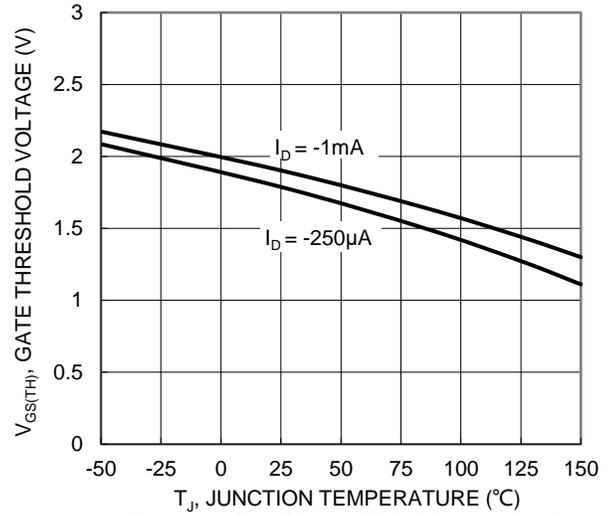


Figure 21. Gate Threshold Variation vs. Junction Temperature

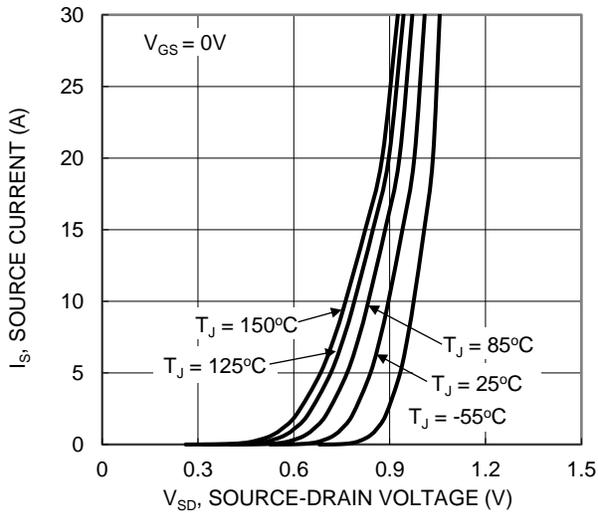


Figure 22. Diode Forward Voltage vs. Current

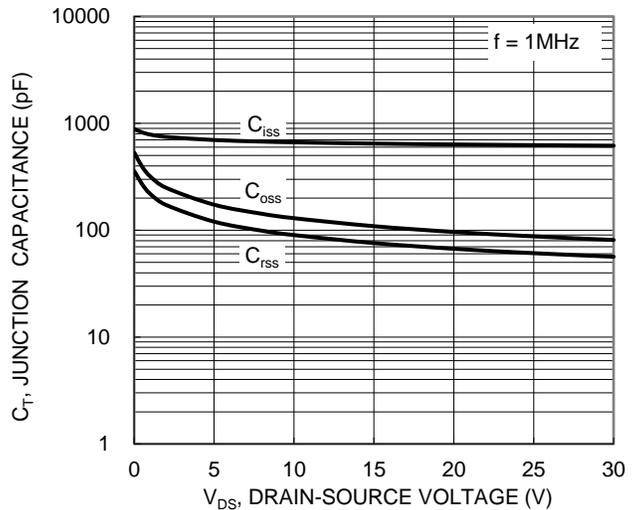


Figure 23. Typical Junction Capacitance

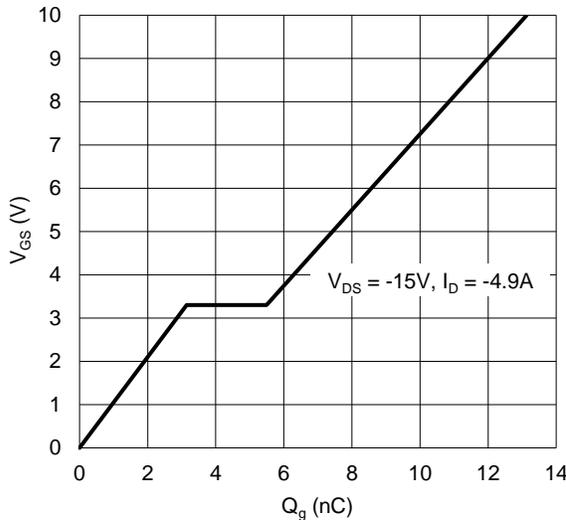


Figure 24. Gate Charge

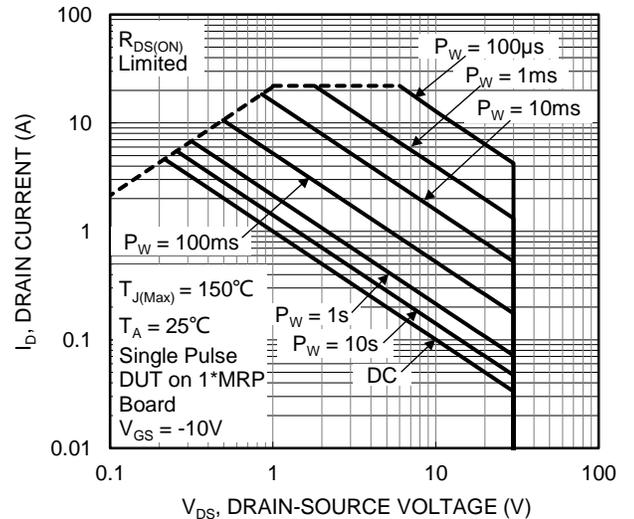


Figure 25. SOA, Safe Operation Area

**Q2 – P-Channel** (continued)

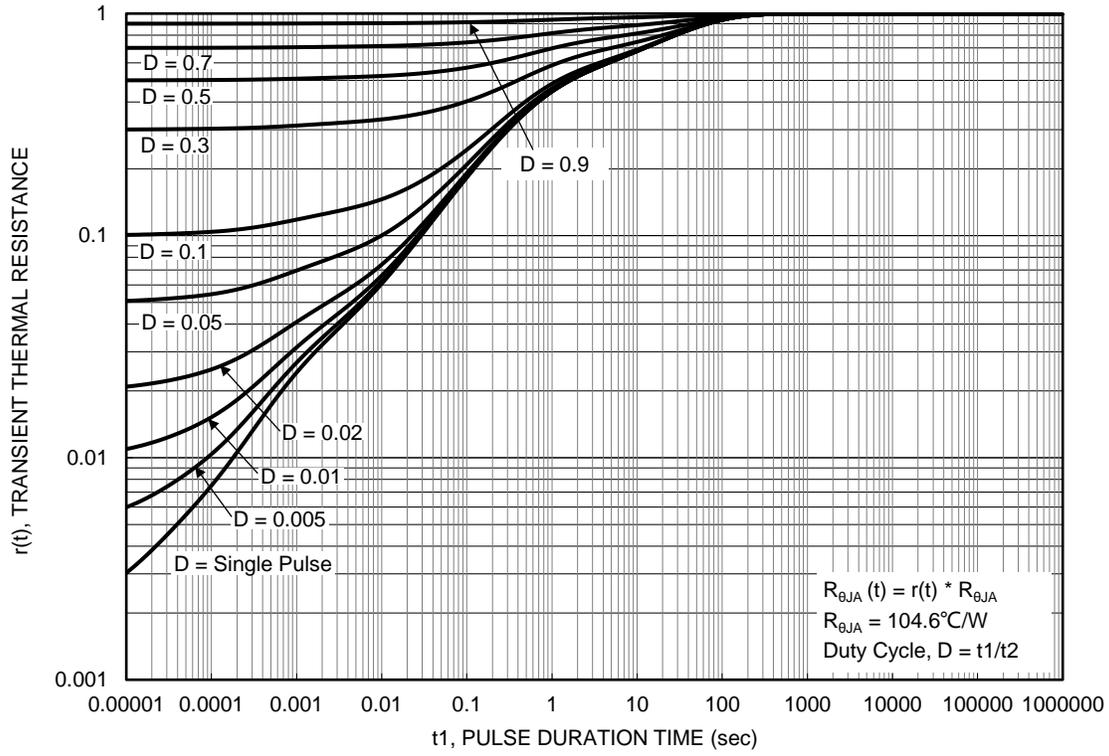
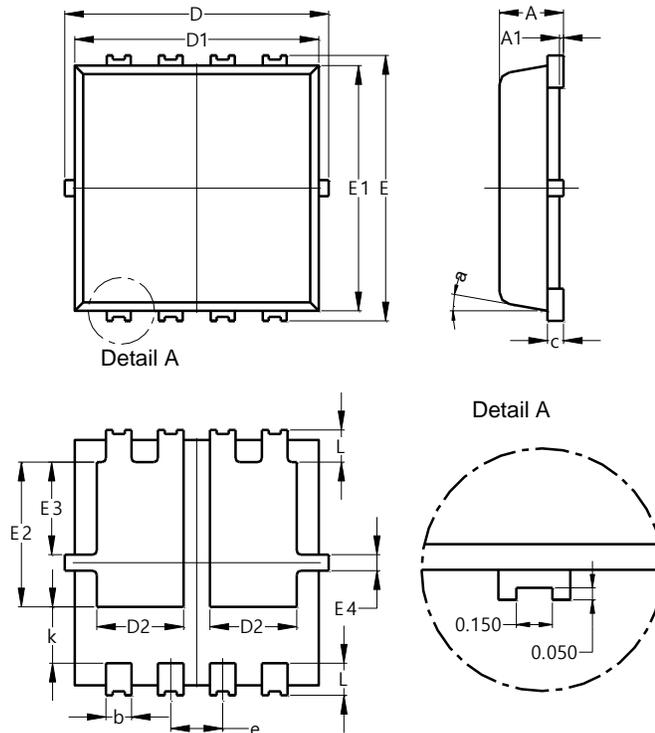


Figure 26. Transient Thermal Resistance

## Package Outline Dimensions

POWERDI®3333-8/SWP (Type UXD)

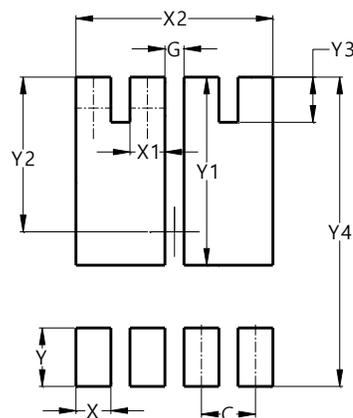


POWERDI®3333-8/SWP (Type UXD)			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	--
b	0.25	0.40	0.32
c	0.10	0.25	0.15
D	3.20	3.40	3.30
D1	2.95	3.15	3.05
D2	1.00	1.20	1.10
E	3.20	3.40	3.30
E1	2.95	3.15	3.05
E2	1.60	2.00	1.80
E3	0.95	1.35	1.15
E4	0.10	0.30	0.20
e	--	--	0.65
L	0.30	0.50	0.40
k	0.50	0.90	0.70
a	0°	12°	10°

All Dimensions in mm

## Suggested Pad Layout

POWERDI®3333-8/SWP (Type UXD)



Dimensions	Value (in mm)
C	0.650
G	0.230
X	0.420
X1	0.420
X2	2.370
Y	0.700
Y1	2.250
Y2	1.850
Y3	0.540
Y4	3.700