优尚

YOUSHANG SEMICONDUCTOR

# 设计研发新型功率器件

## 各类小信号开关

## 中低压及高压大电流等场效应管

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企业微信二维码　企业QQ二维码

## Product Summary

| Device | $V_{(BR)DSS}$ | $R_{DS(on)}$ Max | $I_D$ $T_A$ = +25°C |
|---|---|---|---|
| Q1 | 40V | 28mΩ @ $V_{GS}$= 10V | 7.2A |
| | | 49mΩ @ $V_{GS}$= 4.5V | 5.4A |
| Q2 | -40V | 50mΩ @ $V_{GS}$= -10V | -5.2A |
| | | 79mΩ @ $V_{GS}$= -4.5V | -4.7A |

## Description

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## Applications

- Motor Control
- Backlighting
- DC-DC Converters
- Power Management Functions

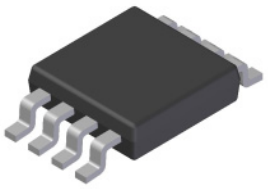
## Features and Benefits

- Low On-Resistance
- Fast Switching Speed

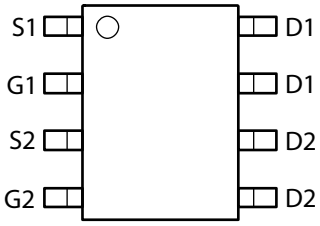
## Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (approximate)

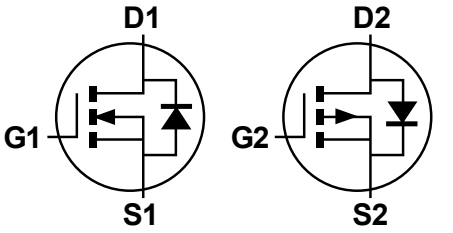
SO-8



Top View




Top View




Equivalent Circuit

## Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

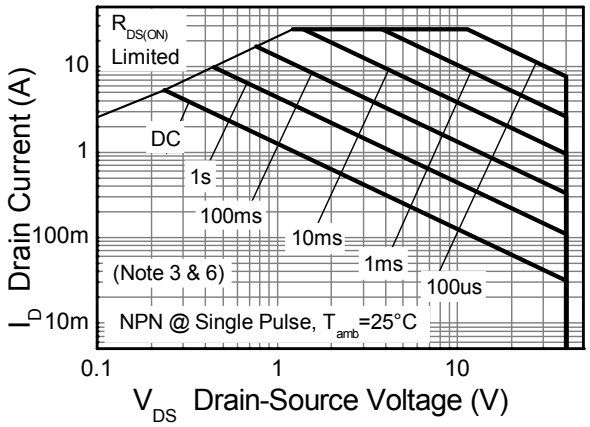
| Characteristic | | | Symbol | N-Channel - Q1 | P-Channel - Q2 | Units |
|---|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DSS}$ | 40 | -40 | V |
| Gate-Source Voltage | | (Note 5) | $V_{GSS}$ | ±20 | ±20 | V |
| Continuous Drain Current | $V_{GS}$ = 10V | (Notes 7 & 9) | $I_D$ | 7.2 | 5.2 | A |
| | | $T_A$ = 70°C (Notes 7 & 9) | | 5.5 | 4.2 | |
| | | (Notes 6 & 9) | | 5.4 | 4 | |
| | | (Notes 6 & 10) | | 6.5 | 4.8 | |
| Pulsed Drain Current | $V_{GS}$ = 10V | (Notes 7 & 9) | $I_{DM}$ | 27.3 | 20.4 | A |
| Continuous Source Current (Body diode) | | (Notes 7 & 9) | $I_S$ | 3.35 | 3.15 | A |
| Pulsed Source Current (Body diode) | | (Notes 8 & 9) | $I_{SM}$ | 27.3 | 20.4 | A |

## Thermal Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

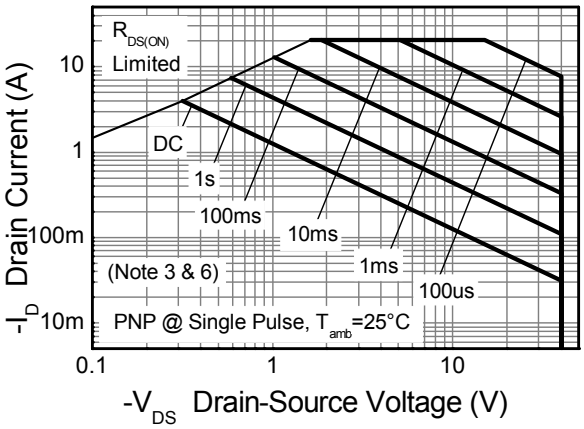
| Characteristic | | Symbol | N-Channel - Q1 | P-Channel - Q2 | Unit |
|---|---|---|---|---|---|
| Power Dissipation<br>Linear Derating Factor | (Notes 6 & 9) | $P_D$ | 1.25<br>10 | | W<br>mW/°C |
| | (Notes 6 & 10) | | 1.8<br>14.3 | | |
| | (Notes 7 & 9) | | 2.16<br>17.2 | | |
| Thermal Resistance, Junction to Ambient | (Notes 6 & 9) | $R_{\theta JA}$ | 100 | | °C/W |
| | (Notes 6 & 10) | | 70 | | |
| | (Notes 7 & 9) | | 58 | | |
| Thermal Resistance, Junction to Lead | (Notes 9 & 11) | $R_{\theta JL}$ | 53 | 53 | |
| Operating and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +150 | | °C |

Notes:
5. AEC-Q101 $V_{GS}$ maximum is ±16V.
6. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
7. Same as note (5), except the device is measured at t ≤ 10 sec.
8. Same as note (5), except the device is pulsed with D= 0.02 and pulse width 300 μs. The pulse current is limited by the maximum junction temperature.
9. For a dual device with one active die.
10. For a device with two active die running at equal power.
11. Thermal resistance from junction to solder-point (at the end of the drain lead).

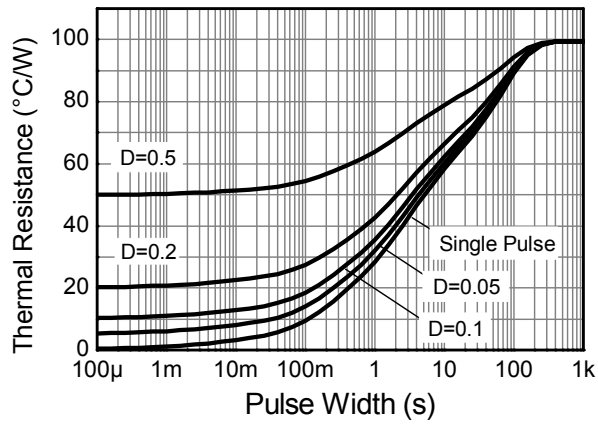
## Thermal Characteristics



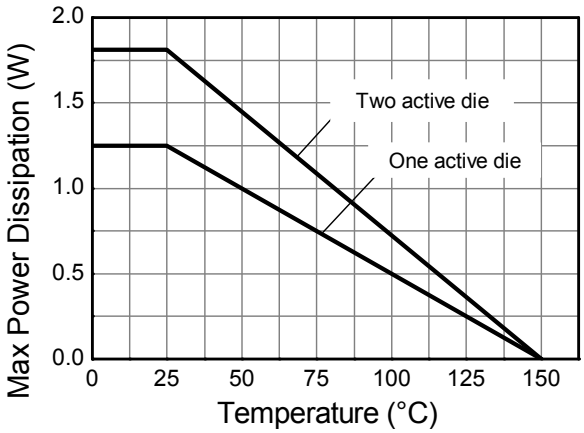

**N-channel Safe Operating Area**



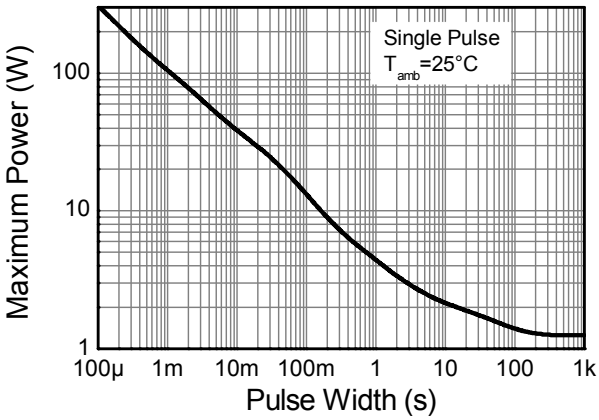

**P-channel Safe Operating Area**




**Transient Thermal Impedance**




**Derating Curve**



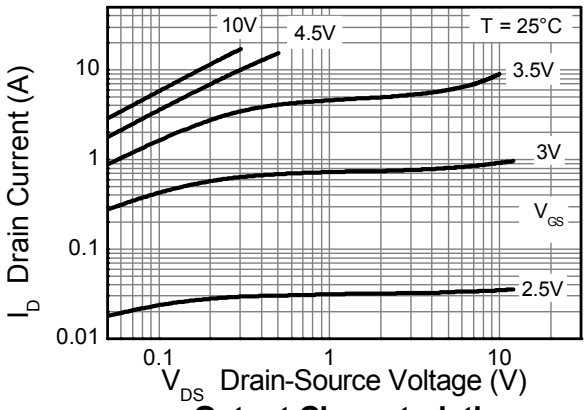

**Pulse Power Dissipation**

## Electrical Characteristics – Q1 N-Channel (@$T_A$ = +25°C, unless otherwise specified.)

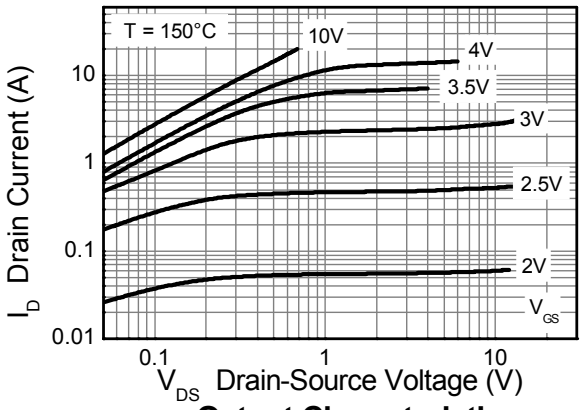
| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 40 | — | — | V | $I_D$ = 250μA, $V_{GS}$ = 0V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | 0.5 | μA | $V_{DS}$ = 40V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | — | 3.0 | V | $I_D$ = 250μA, $V_{DS}$ = $V_{GS}$ |
| Static Drain-Source On-Resistance (Note 12) | $R_{DS\ (ON)}$ | — | 0.018 | 0.028 | Ω | $V_{GS}$ = 10V, $I_D$ = 6A |
| | | | 0.033 | 0.049 | | $V_{GS}$ = 4.5V, $I_D$ = 5A |
| Forward Transconductance (Notes 12 & 13) | $g_{fs}$ | — | 22.8 | — | S | $V_{DS}$ = 15V, $I_D$ = 6A |
| Diode Forward Voltage (Note 12) | $V_{SD}$ | — | 0.845 | 1.1 | V | $I_S$ = 6A, $V_{GS}$ = 0V |
| Reverse recovery time (Note 13) | $t_{rr}$ | | 135 | — | ns | $I_S$ = 6A, di/dt = 100A/μs |
| Reverse recovery charge (Note 13) | $Q_{rr}$ | — | 799 | — | nC | |
| **DYNAMIC CHARACTERISTICS (Note 13)** | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 604 | — | pF | $V_{DS}$ = 20V, $V_{GS}$ = 0V<br>f = 1MHz |
| Output Capacitance | $C_{oss}$ | — | 106 | — | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 59.6 | — | pF | |
| Total Gate Charge (Note 14) | $Q_g$ | — | 6.5 | — | nC | $V_{GS}$ = 4.5V; $V_{DS}$ = 20V, $I_D$ = 6A |
| Total Gate Charge (Note 14) | $Q_g$ | — | 12.9 | — | nC | $V_{GS}$ = 10V; $V_{DS}$ = 20V, $I_D$ = 6A |
| Gate-Source Charge (Note 14) | $Q_{gs}$ | — | 2.3 | — | nC | $V_{GS}$ = 10V; $V_{DS}$ = 20V, $I_D$ = 6A |
| Gate-Drain Charge (Note 14) | $Q_{gd}$ | — | 3.6 | — | nC | $V_{GS}$ = 10V; $V_{DS}$ = 20V, $I_D$ = 6A |
| Turn-On Delay Time (Note 14) | $t_{D(on)}$ | — | 4.2 | — | ns | $V_{DD}$ = 20V, $V_{GS}$ = 10V<br>$I_D$ = 6A, $R_G \cong$ 6.0Ω |
| Turn-On Rise Time (Note 14) | $t_r$ | — | 12.4 | — | ns | |
| Turn-Off Delay Time (Note 14) | $t_{D(off)}$ | — | 13.8 | — | ns | |
| Turn-Off Fall Time (Note 14) | $t_f$ | — | 10.7 | — | ns | |

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
13. For design aid only, not subject to production testing.
14. Switching characteristics are independent of operating junction temperatures.

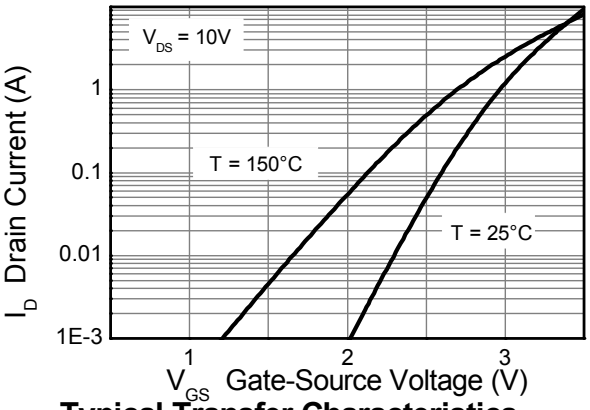
## Typical Characteristics – Q1 N-Channel



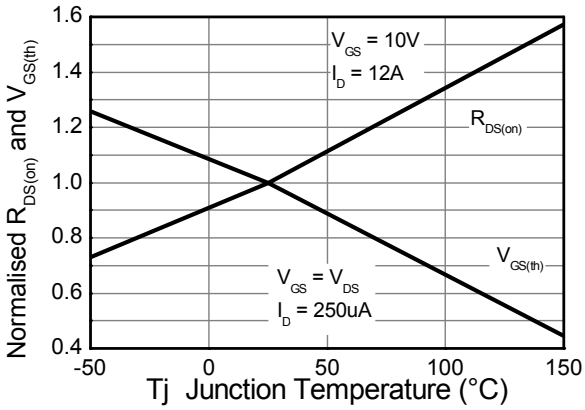

**Output Characteristics**



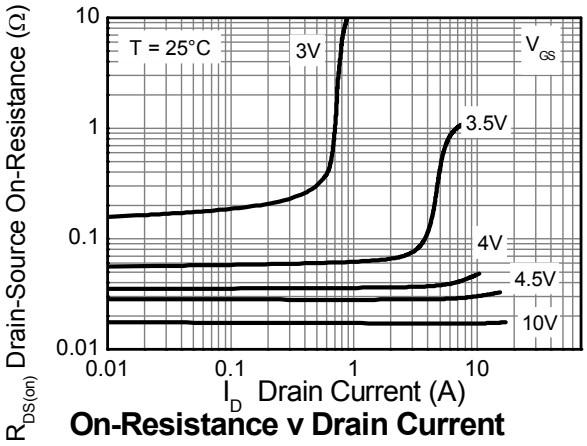

**Output Characteristics**



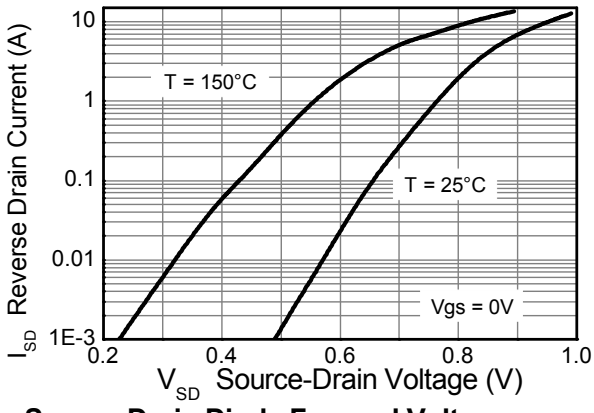

**Typical Transfer Characteristics**




**Normalised Curves v Temperature**

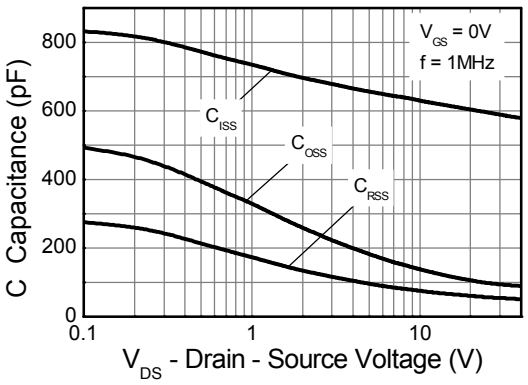



**On-Resistance v Drain Current**

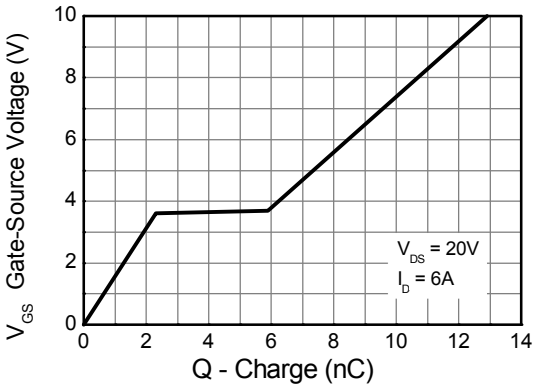



**Source-Drain Diode Forward Voltage**

## Typical Characteristics – Q1 N-Channel - (cont.)

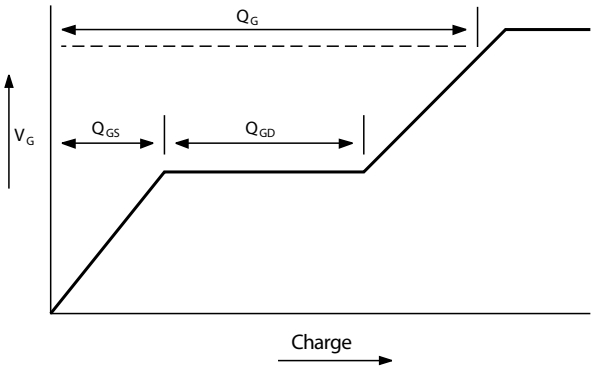



**Capacitance v Drain-Source Voltage**

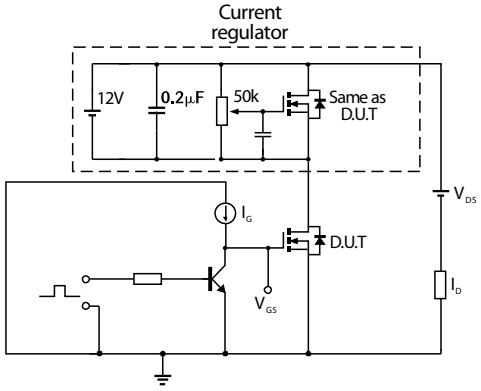



**Gate-Source Voltage v Gate Charge**

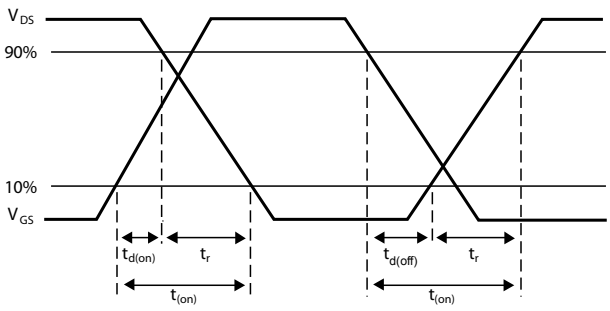
## Test Circuits – Q1 N-Channel



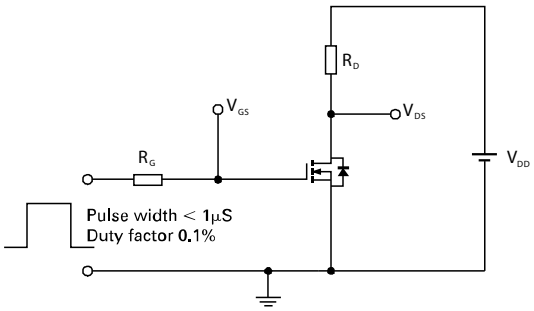

**Basic gate charge waveform**




**Gate charge test circuit**




**Switching time waveforms**



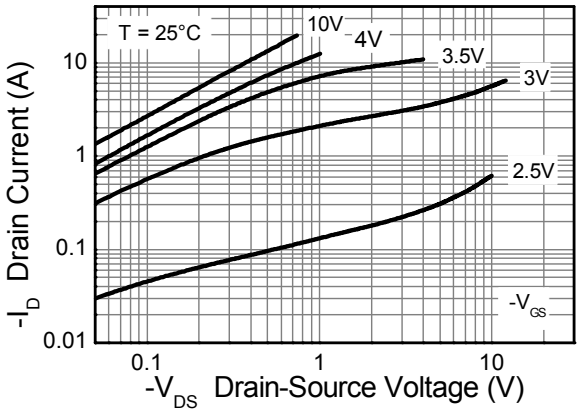

**Switching time test circuit**

## Electrical Characteristics – Q2 P-Channel (@$T_A$ = +25°C, unless otherwise specified.)

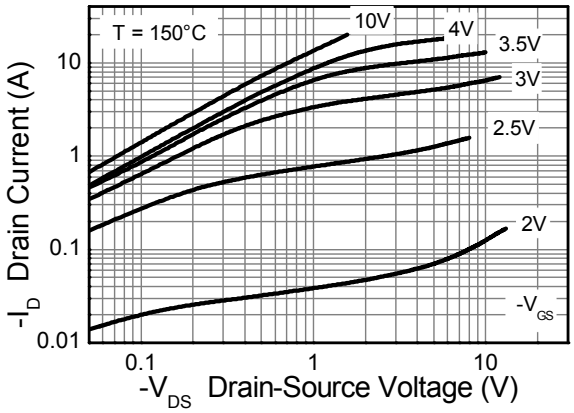
| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | -40 | — | — | V | $I_D$ = -250 μA, $V_{GS}$ = 0V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | -0.5 | μA | $V_{DS}$ = -40V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -1.0 | – | -3.0 | V | $I_D$ = -250 μA, $V_{DS}$ = $V_{GS}$ |
| Static Drain-Source On-Resistance (Note 12) | $R_{DS(ON)}$ | — | 0.039 | 0.050 | Ω | $V_{GS}$ = -10V, $I_D$ = -6A |
| | | | 0.060 | 0.079 | | $V_{GS}$ = -4.5V, $I_D$ = -5A |
| Forward Transconductance (Notes 12 & 13) | $g_{fs}$ | — | 16.6 | — | S | $V_{DS}$ = -15V, $I_D$ = -6A |
| Diode Forward Voltage (Note 13) | $V_{SD}$ | — | -0.865 | -1.1 | V | $I_S$ = -6A, $V_{GS}$ = 0V |
| Reverse Recovery Time (Note 13) | $t_{rr}$ | — | 138 | — | ns | $I_S$ = -6A, di/dt = 100A/μs |
| Reverse Recovery Charge (Note 13) | $Q_{rr}$ | — | 841 | — | nC | |
| **DYNAMIC CHARACTERISTICS (Note 13)** | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 674 | — | pF | $V_{DS}$ = -20V, $V_{GS}$ = 0V<br>f = 1MHz |
| Output Capacitance | $C_{oss}$ | — | 115 | — | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 67.7 | — | pF | |
| Total Gate Charge (Note 14) | $Q_g$ | — | 7.0 | — | nC | $V_{GS}$ = -4.5V; $V_{DS}$ = -20V, $I_D$ = -6A |
| Total Gate Charge (Note 14) | $Q_g$ | — | 14 | — | nC | $V_{GS}$ = -10V; $V_{DS}$ = -20V, $I_D$ = -6A |
| Gate-Source Charge (Note 14) | $Q_{gs}$ | — | 2.2 | — | nC | $V_{GS}$ = -10V; $V_{DS}$ = -20V, $I_D$ = -6A |
| Gate-Drain Charge (Note 14) | $Q_{gd}$ | — | 3.7 | — | nC | $V_{GS}$ = -10V; $V_{DS}$ = -20V, $I_D$ = -6A |
| Turn-On Delay Time (Note 14) | $t_{D(on)}$ | — | 2.3 | — | ns | $V_{DD}$ = -20V, $V_{GS}$ = -10V<br>$I_D$ = -6A, $R_G \cong$ 6.0Ω |
| Turn-On Rise Time (Note 14) | $t_r$ | — | 14.1 | — | ns | |
| Turn-Off Delay Time (Note 14) | $t_{D(off)}$ | — | 25.1 | — | ns | |
| Turn-Off Fall Time (Note 14) | $t_f$ | — | 14.3 | — | ns | |

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
13. For design aid only, not subject to production testing.
14. Switching characteristics are independent of operating junction temperatures.

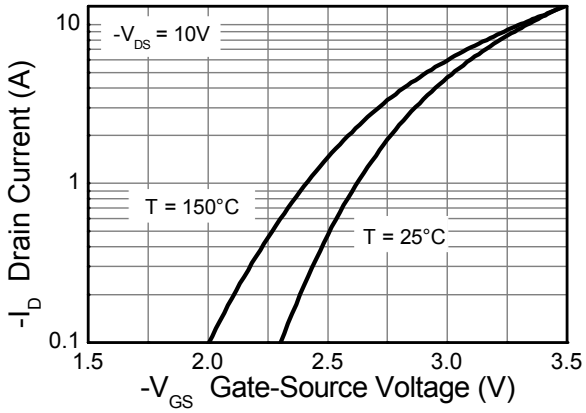
## Typical Characteristics – Q2 P-Channel



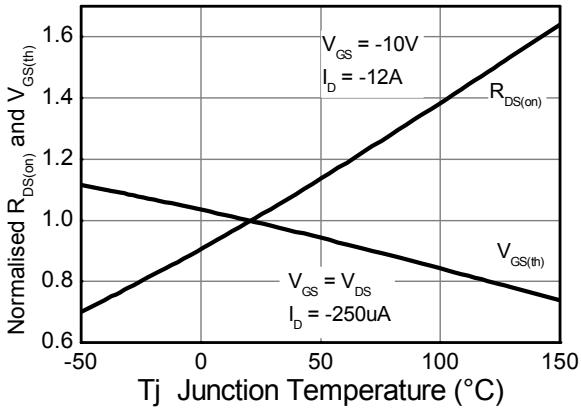

**Output Characteristics**



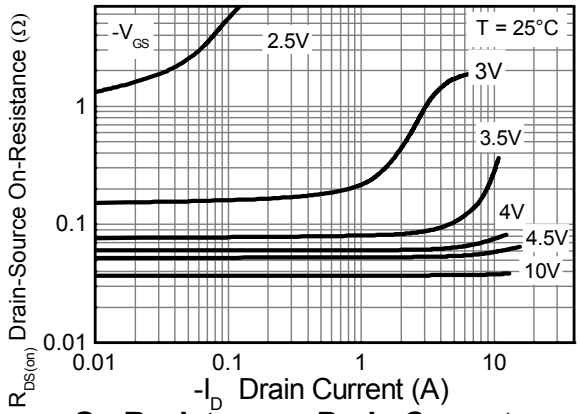

**Output Characteristics**



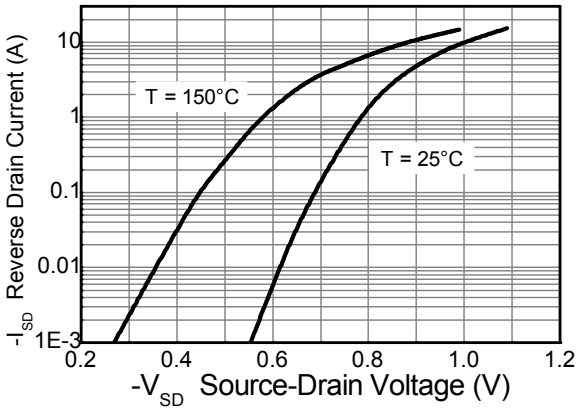

**Typical Transfer Characteristics**




**Normalised Curves v Temperature**

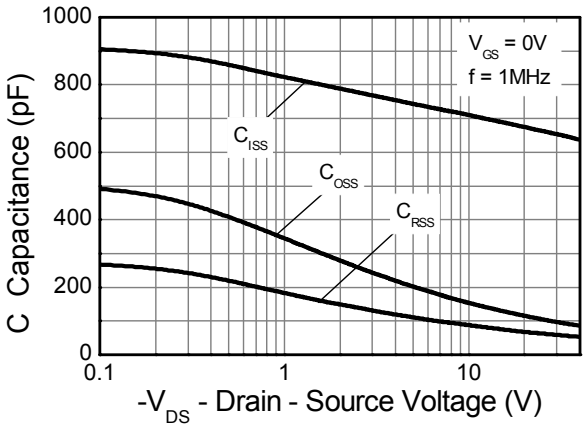



**On-Resistance v Drain Current**

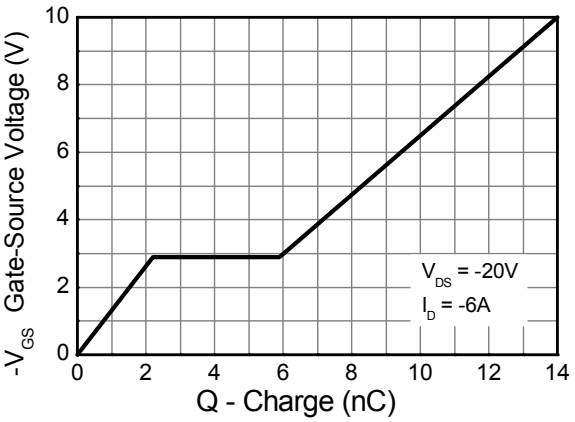



**Source-Drain Diode Forward Voltage**

## Typical Characteristics – Q2 P-Channel – (cont.)

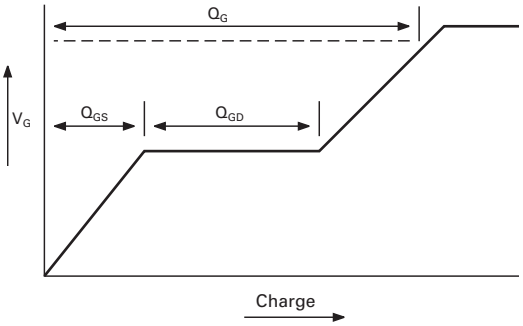



**Capacitance v Drain-Source Voltage**

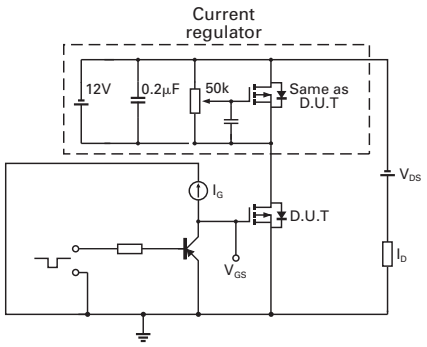



**Gate-Source Voltage v Gate Charge**

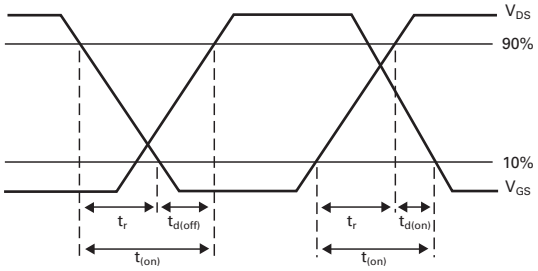
## Test Circuits – Q2 P-Channel



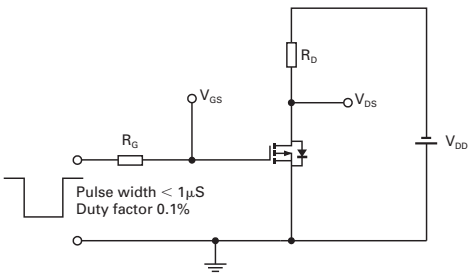

**Basic gate charge waveform**




**Gate charge test circuit**

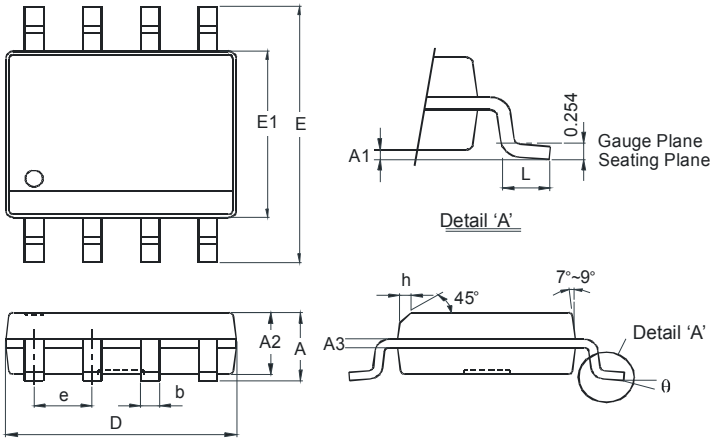



**Switching time waveforms**



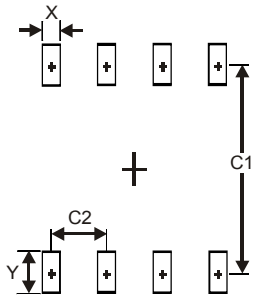

**Switching time test circuit**

## Package Outline Dimensions




| SO-8 | | |
|---|---|---|
| **Dim** | **Min** | **Max** |
| **A** | - | 1.75 |
| **A1** | 0.10 | 0.20 |
| **A2** | 1.30 | 1.50 |
| **A3** | 0.15 | 0.25 |
| **b** | 0.3 | 0.5 |
| **D** | 4.85 | 4.95 |
| **E** | 5.90 | 6.10 |
| **E1** | 3.85 | 3.95 |
| **e** | 1.27 Typ | |
| **h** | - | 0.35 |
| **L** | 0.62 | 0.82 |
| **θ** | 0° | 8° |
| All Dimensions in mm | | |

## Suggested Pad Layout




| Dimensions | Value (in mm) |
|---|---|
| **X** | 0.60 |
| **Y** | 1.55 |
| **C1** | 5.4 |
| **C2** | 1.27 |