



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



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Product Summary

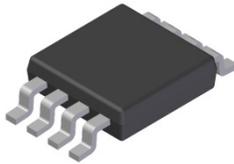
Device	$V_{(BR)DSS}$	$R_{DS(on) \max}$	I_D $T_A = +25^\circ\text{C}$
Q2	40V	$24\text{m}\Omega @ V_{GS} = 10\text{V}$	9.0A
		$32\text{m}\Omega @ V_{GS} = 4.5\text{V}$	7.8A
Q1	-40V	$45\text{m}\Omega @ V_{GS} = -10\text{V}$	-6.5A
		$55\text{m}\Omega @ V_{GS} = -4.5\text{V}$	-5.9A

Description

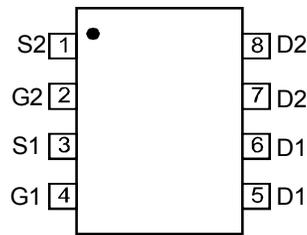
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Backlighting



Top View



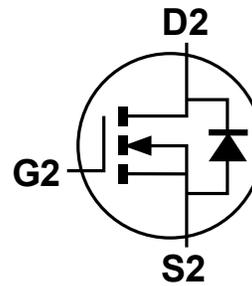
TOP VIEW
Internal Schematic

Features and Benefits

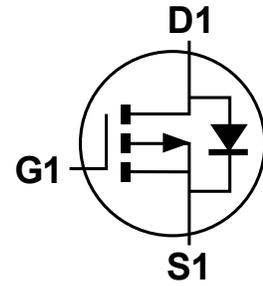
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 [Ⓔ]3
- Weight: 0.074 grams (approximate)



N-Channel MOSFET



P-Channel MOSFET

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value Q2	Value Q1	Units
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	± 20	± 20	V
Continuous Drain Current (Note 7) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	7.0 5.6	-5.1 -4.1	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$		9.0 7.2	-6.5 -5.2	
Maximum Body Diode Forward Current (Note 7)			I_S	2.5	-2.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	70	-40	A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.3	W
	$T_A = +70^\circ\text{C}$		0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	98	$^\circ\text{C/W}$
	$t < 10\text{s}$		59	
Total Power Dissipation (Note 7)	$T_A = +25^\circ\text{C}$	P_D	1.8	W
	$T_A = +70^\circ\text{C}$		1.1	
Thermal Resistance, Junction to Ambient (Note 7)	Steady state	$R_{\theta JA}$	71	$^\circ\text{C/W}$
	$t < 10\text{s}$		43	
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	11.8	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

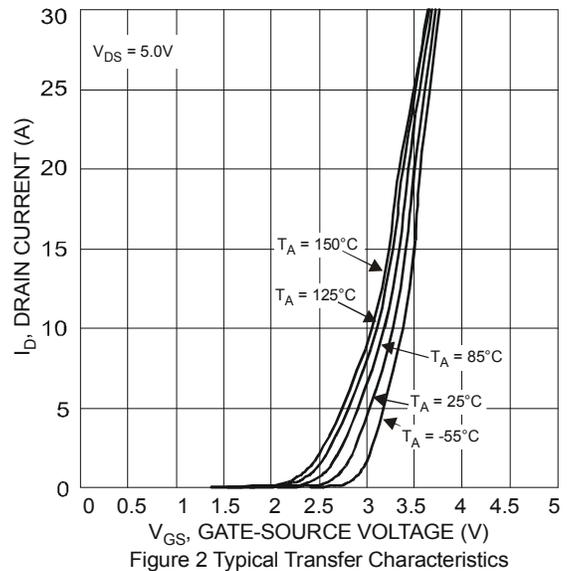
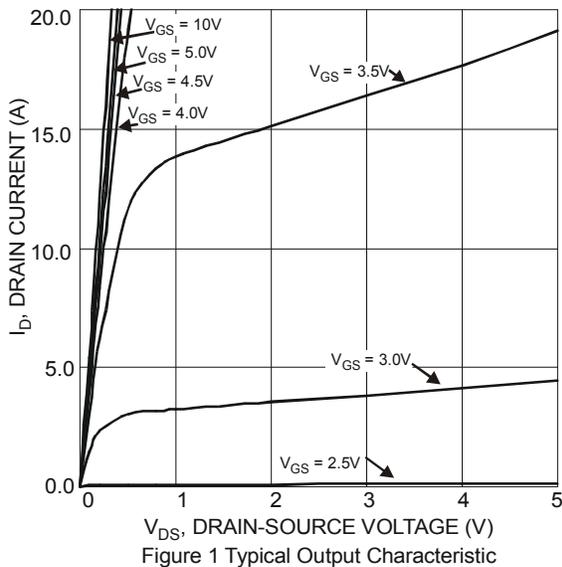
Electrical Characteristics N-Channel Q2 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	15	24	m Ω	$V_{GS} = 10\text{V}, I_D = 6\text{A}$
		—	20	32		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.0	V	$V_{GS} = 0\text{V}, I_S = 1.0\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1060	—	pF	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	84	—		
Reverse Transfer Capacitance	C_{rss}	—	58	—		
Gate Resistance	R_G	—	1.6	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	8.8	—	nC	$V_{DS} = 20\text{V}, I_D = 8\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	19.1	—		
Gate-Source Charge	Q_{gs}	—	3.0	—		
Gate-Drain Charge	Q_{gd}	—	2.5	—		
Turn-On Delay Time	$t_{D(on)}$	—	5.3	—	nS	$V_{DD} = 25\text{V}, R_L = 2.5\Omega, V_{GS} = 10\text{V}, R_G = 3\Omega$
Turn-On Rise Time	t_r	—	7.1	—		
Turn-Off Delay Time	$t_{D(off)}$	—	15.1	—		
Turn-Off Fall Time	t_f	—	4.8	—		
Body Diode Reverse Recovery Time	t_{rr}	—	10.5	—	nS	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	4.15	—	nC	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$

Electrical Characteristics P-Channel Q1 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -40V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-3.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	33	45	m Ω	$V_{GS} = -10V, I_D = -5A$
		—	40	55		$V_{GS} = -4.5V, I_D = -4A$
Diode Forward Voltage	V_{SD}	—	-0.7	-1.0	V	$V_{GS} = 0V, I_S = -1.0A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1154	—	pF	$V_{DS} = -20V, V_{GS} = 0V$ $f = 1.0MHz$
Output Capacitance	C_{oss}	—	84	—		
Reverse Transfer Capacitance	C_{rss}	—	66	—		
Gate Resistance	R_G	—	12.6	—	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge ($V_{GS} = -4.5V$)	Q_g	—	10.6	—	nC	$V_{DS} = -20V, I_D = -4.9A$
Total Gate Charge ($V_{GS} = -10V$)	Q_g	—	21.5	—		
Gate-Source Charge	Q_{gs}	—	2.2	—		
Gate-Drain Charge	Q_{gd}	—	3.3	—		
Turn-On Delay Time	$t_{D(on)}$	—	8.7	—	nS	$V_{DS} = -20V, I_D = -3.9A$ $V_{GS} = -4.5V, R_G = 1\Omega$
Turn-On Rise Time	t_r	—	19.6	—		
Turn-Off Delay Time	$t_{D(off)}$	—	34.9	—		
Turn-Off Fall Time	t_f	—	25.5	—		
Body Diode Reverse Recovery Time	t_{rr}	—	9.61	—	nS	$I_S = -3.9A, di/dt = 100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	—	3.3	—	nC	$I_S = -3.9A, di/dt = 100A/\mu s$

- Notes:
6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 7. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.

N-Channel Q2


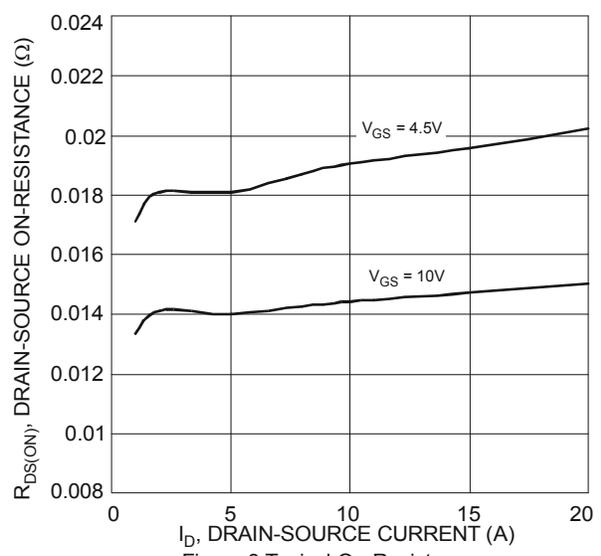


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

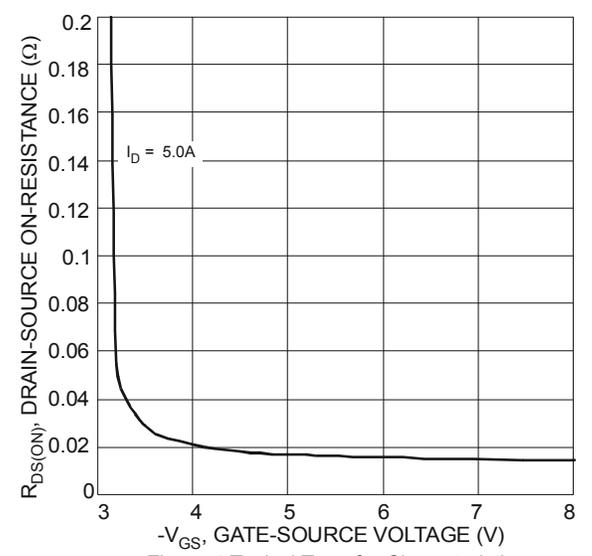


Figure 4 Typical Transfer Characteristic

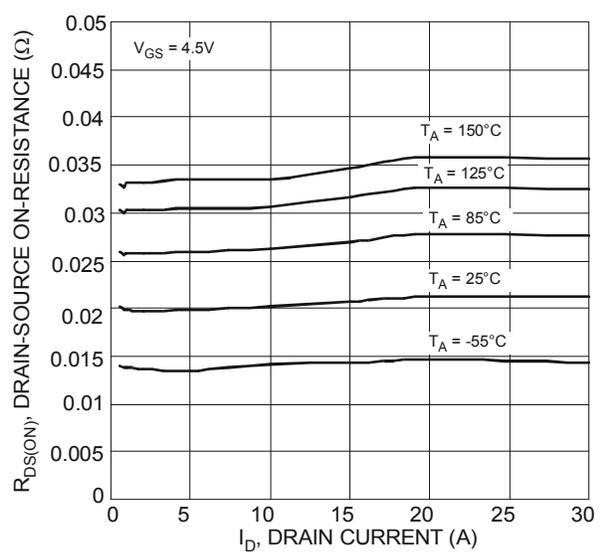


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

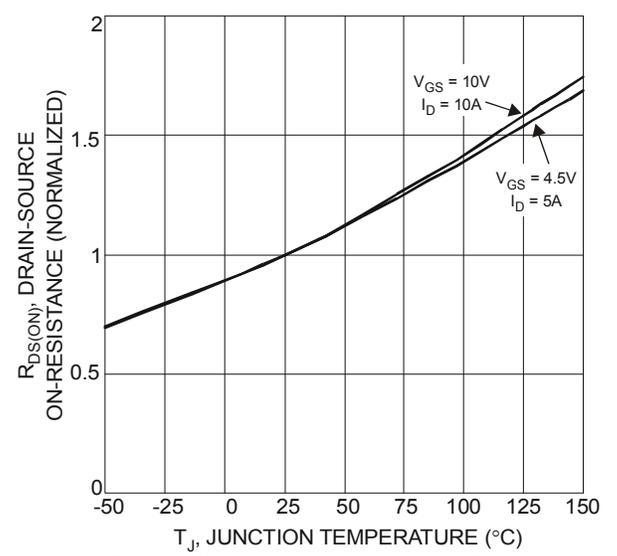


Figure 6 On-Resistance Variation with Temperature

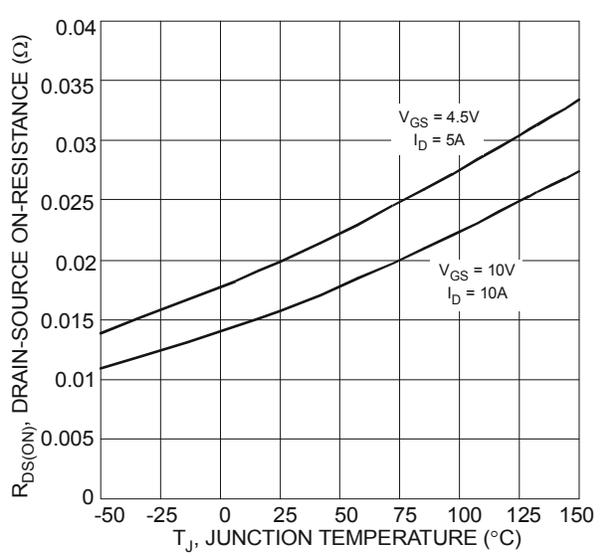


Figure 7 On-Resistance Variation with Temperature

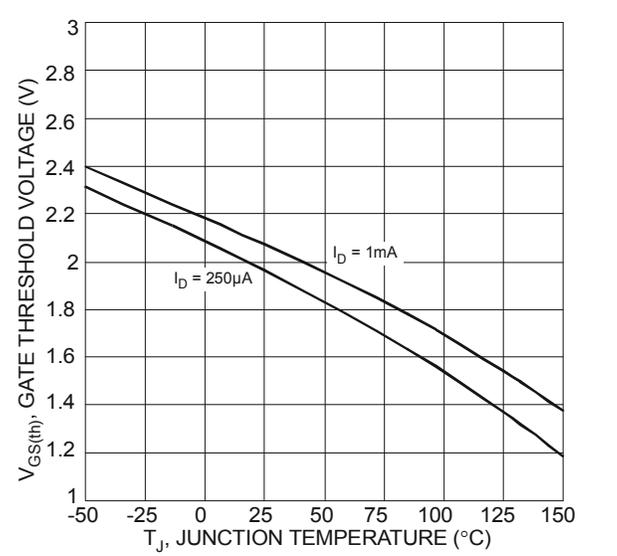


Figure 8 Gate Threshold Variation vs. Ambient Temperature

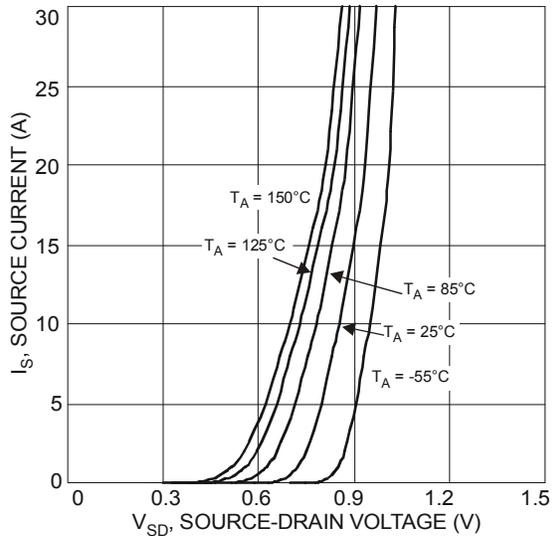


Figure 9 Diode Forward Voltage vs. Current

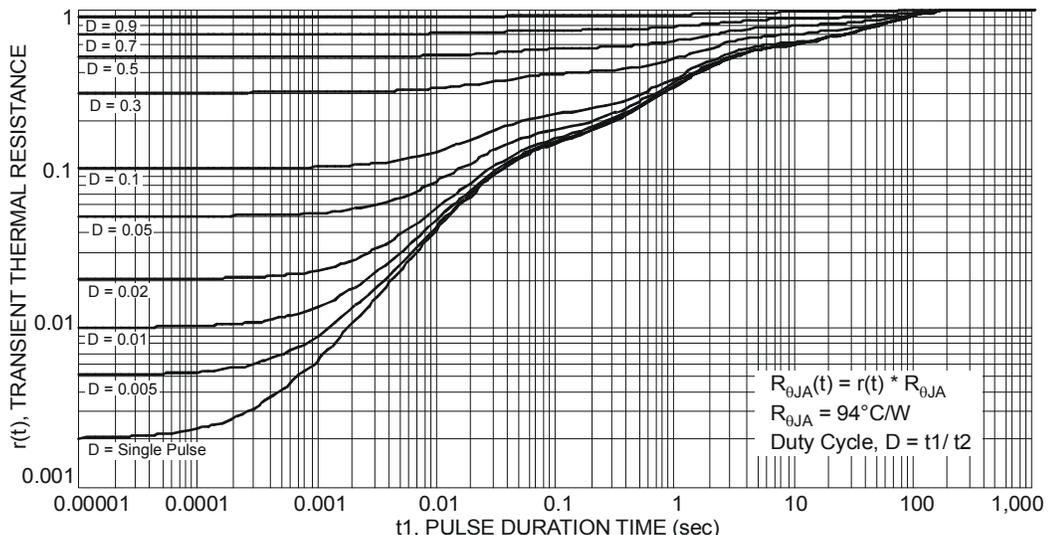


Figure 10 Transient Thermal Resistance

P-Channel Q1

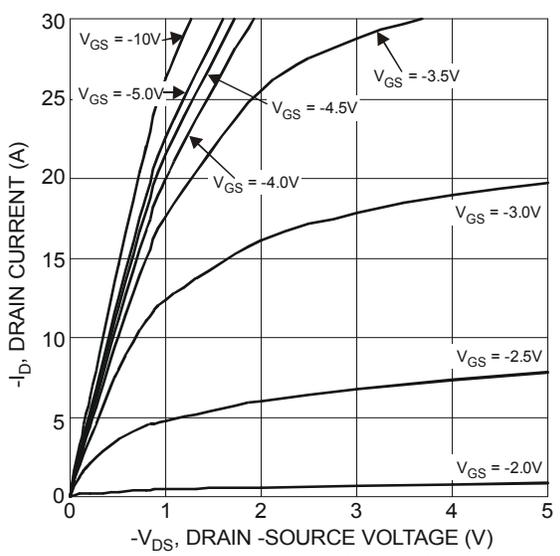


Figure 1 Typical Output Characteristics

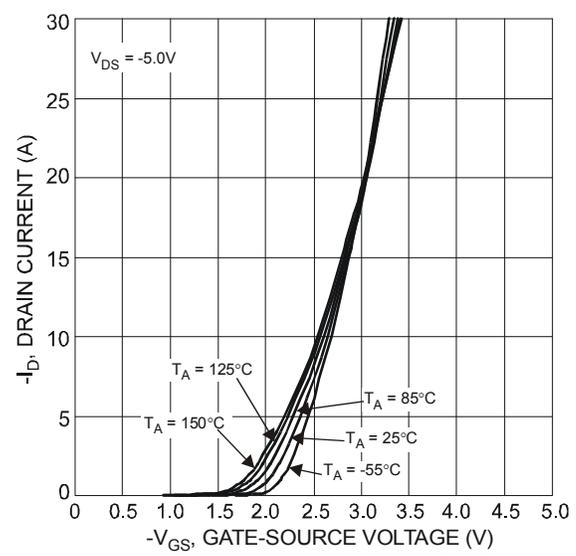
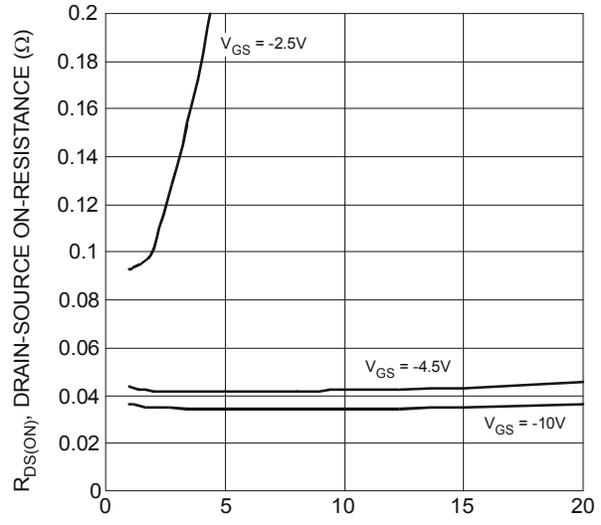
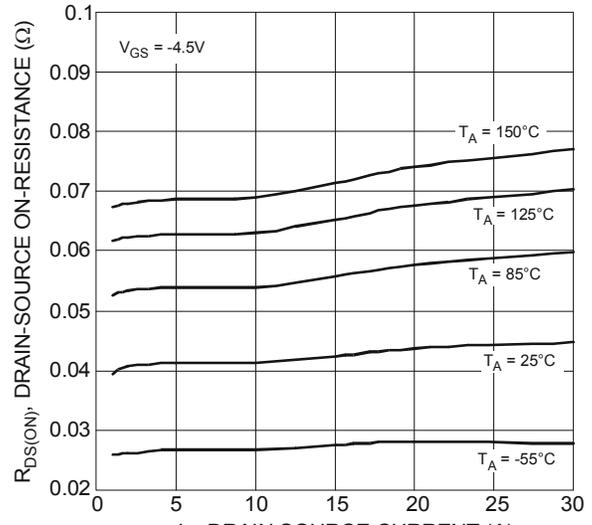


Figure 2 Typical Transfer Characteristics



-I_D, DRAIN SOURCE CURRENT (A)
Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage



-I_D, DRAIN SOURCE CURRENT (A)
Figure 4 Typical On-Resistance vs. Drain Current and Temperature

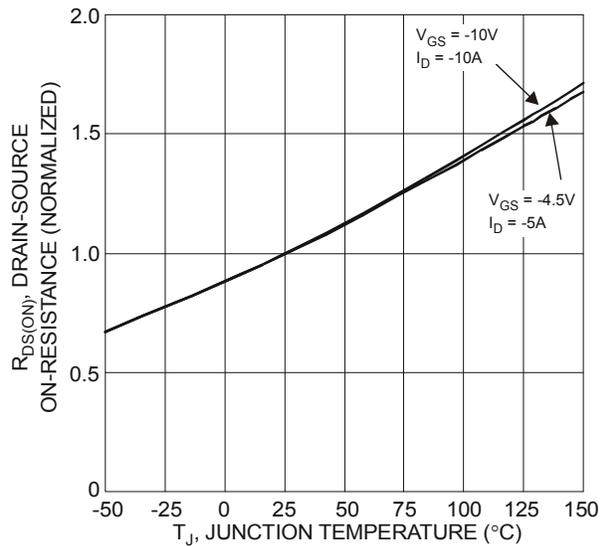


Figure 5 On-Resistance Variation with Temperature

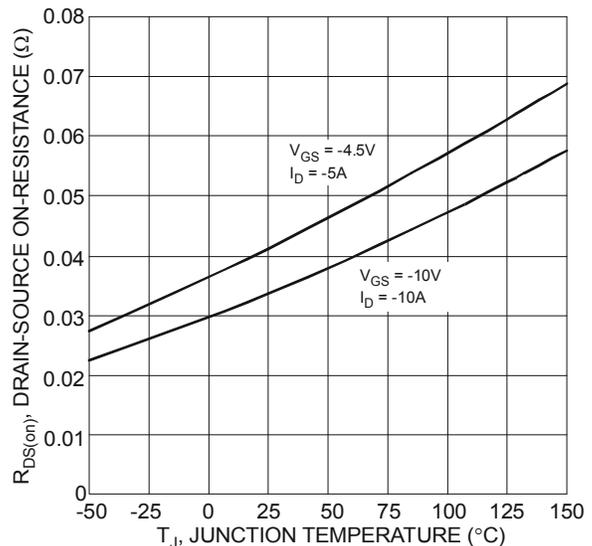


Figure 6 On-Resistance Variation with Temperature

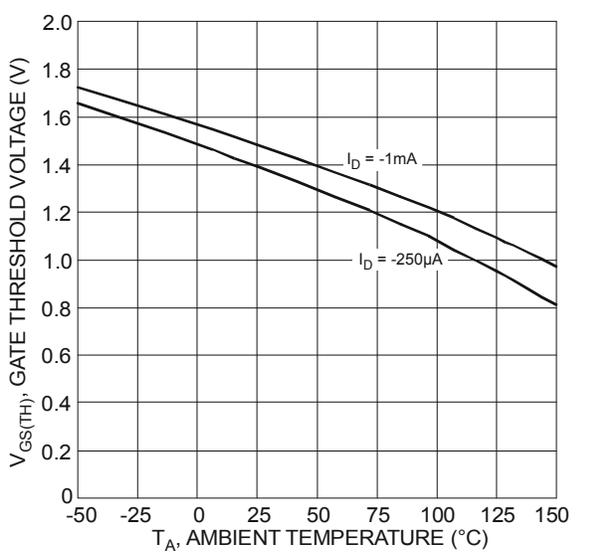


Figure 7 Gate Threshold Variation vs. Ambient Temperature

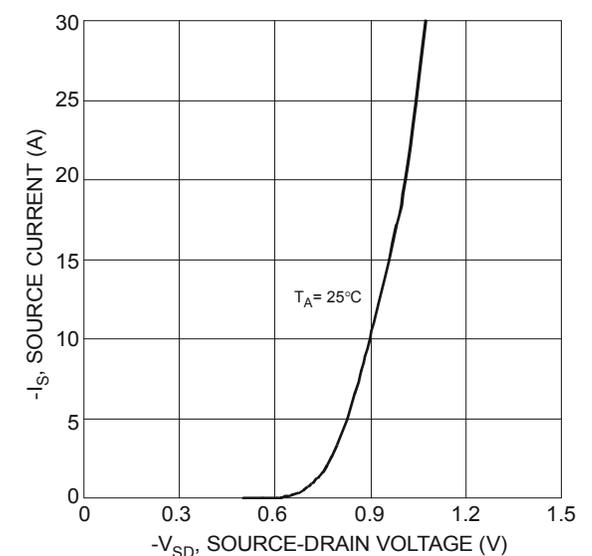
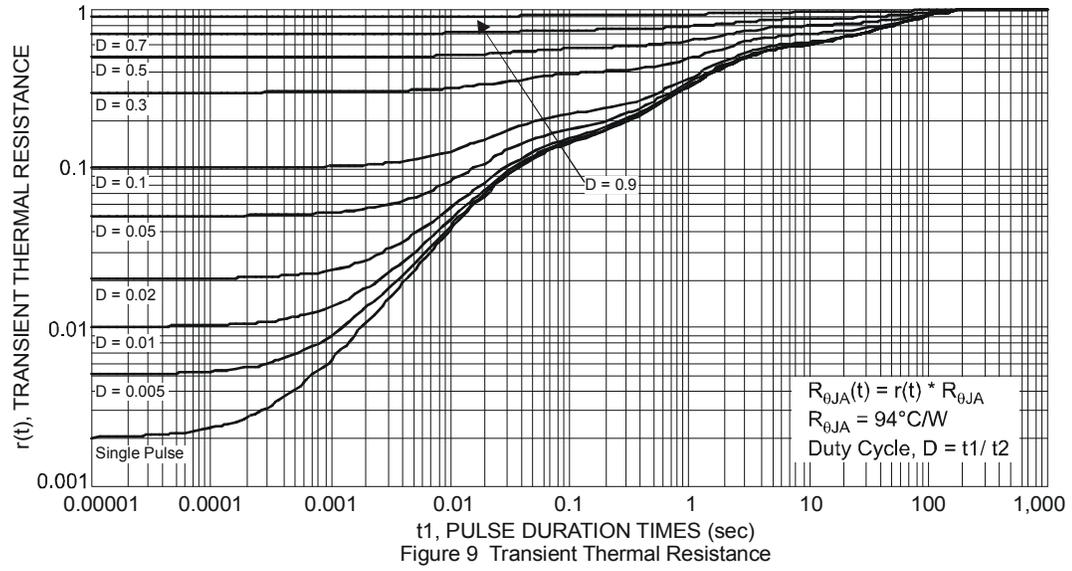
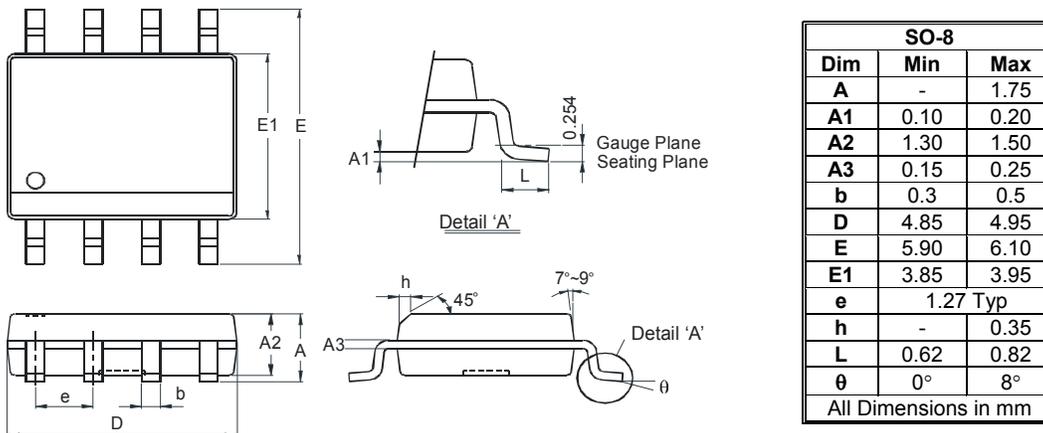


Figure 8 Diode Forward Voltage vs. Current



Package Outline Dimensions



Suggested Pad Layout

