优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
-20V	160mΩ @ V_{GS} = -4.5V	-2.4A
	210mΩ @ V_{GS} = -2.5V	-2.1A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Backlighting
- Power management functions
- DC-DC converters
- Motor controls

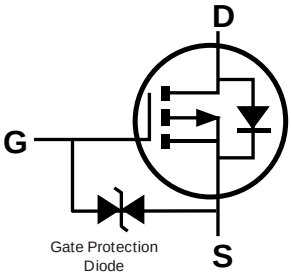
Mechanical Data

- Package: SOT23
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminals Connections: See Diagram Below
- Weight: 0.009 grams (Approximate)

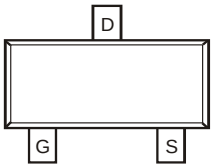
ESD Protected Gate

SOT23 (Standard)

Top View



Internal Schematic



Top View

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-2.4 -1.9	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	-1.12	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-8	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)		P_D	0.84	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	150	°C/W
Total Power Dissipation (Note 5)		P_D	1.40	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	91	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on 1” x 1” FR-4 PCB with high coverage 2oz. copper, single sided.
6. Device mounted on FR-4 PCB, with minimum recommended pad layout.

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current (T_J = +25°C)	I_{DSS}	—	—	-10	μA	V_{DS} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±10V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.3	-0.6	-1.0	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	136	160	mΩ	V_{GS} = -4.5V, I_D = -1.0A
			183	210		V_{GS} = -2.5V, I_D = -1.0A
			229	298		V_{GS} = -1.8V, I_D = -0.2A
Diode Forward Voltage	V_{SD}	—	-0.8	-1.2	V	V_{GS} = 0V, I_S = -1.0A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	156	—	pF	V_{DS} = -6V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	36	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	28	—	pF	
Gate Resistance	R_g	—	41	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	1.6	—	nC	V_{DS} = -6V I_D = -2.2A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	3.4	—	nC	
Gate-Source Charge	Q_{gs}	—	0.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.4	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.2	—	ns	V_{DS} = -6V, V_{GS} = -4.5V R_{GEN} = 6Ω, I_D = -1A
Turn-On Rise Time	t_R	—	7.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	11.0	—	ns	
Turn-Off Fall Time	t_F	—	10.5	—	ns	
Reverse Recovery Time	t_{RR}	—	6.5	—	ns	I_F = -1.0A, dI/dt = 100A/μs
Reverse Recovery Charge	Q_{RR}	—	0.8	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

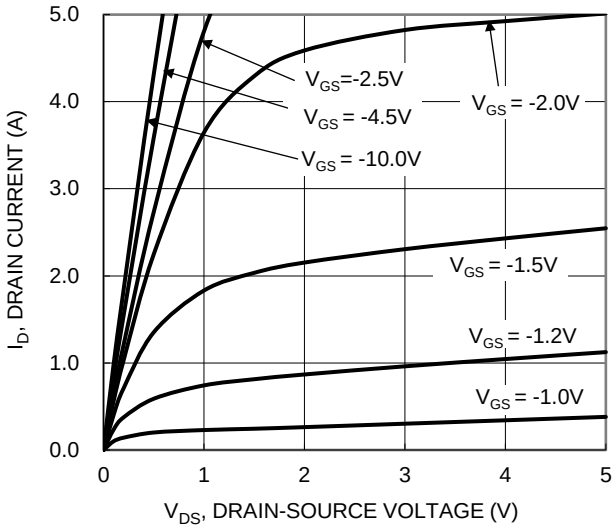


Figure 1. Typical Output Characteristic

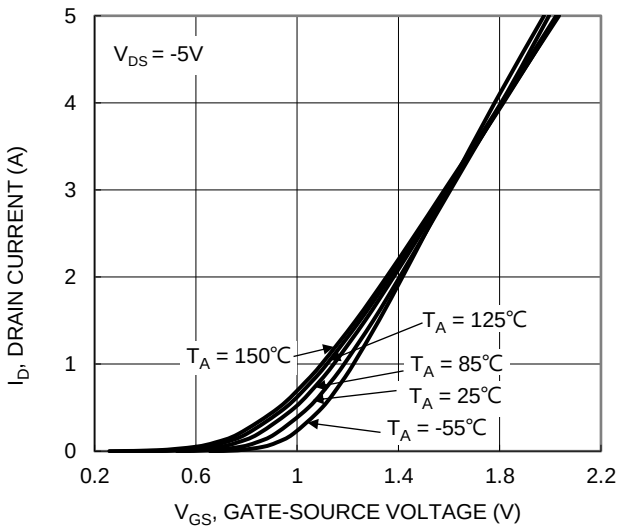


Figure 2. Typical Transfer Characteristic

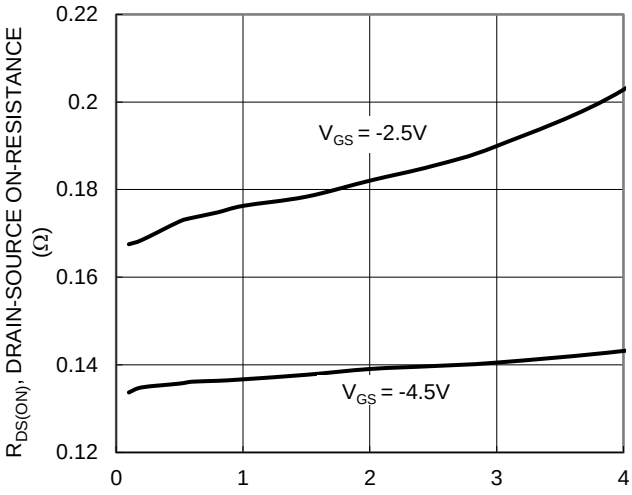


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

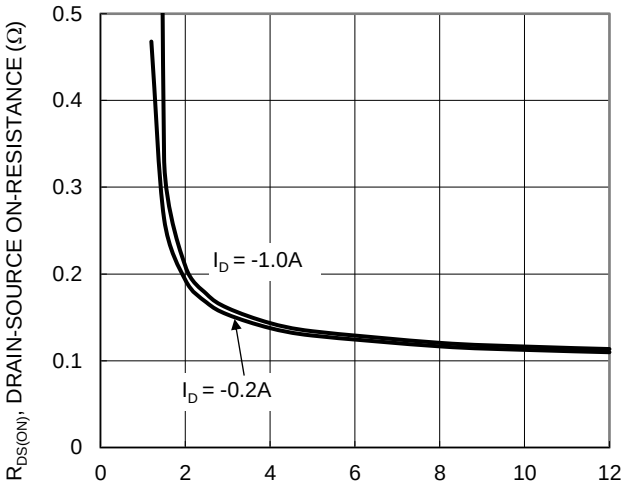


Figure 4. Typical Transfer Characteristic

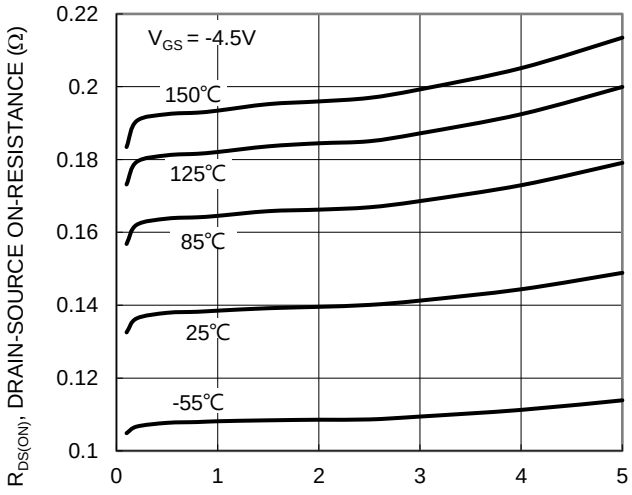


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

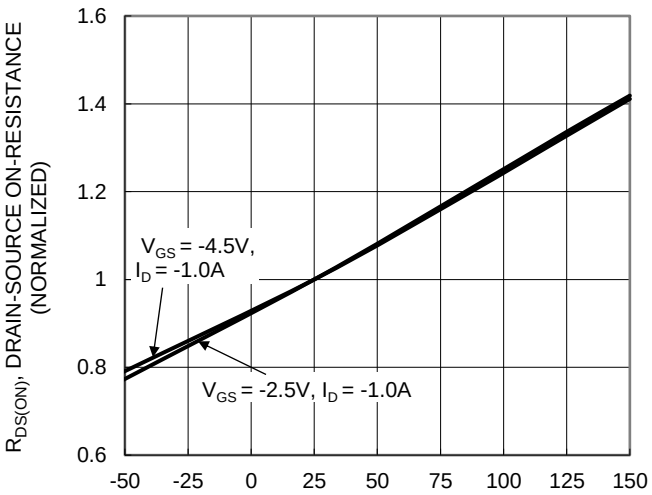


Figure 6. On-Resistance Variation with Junction Temperature

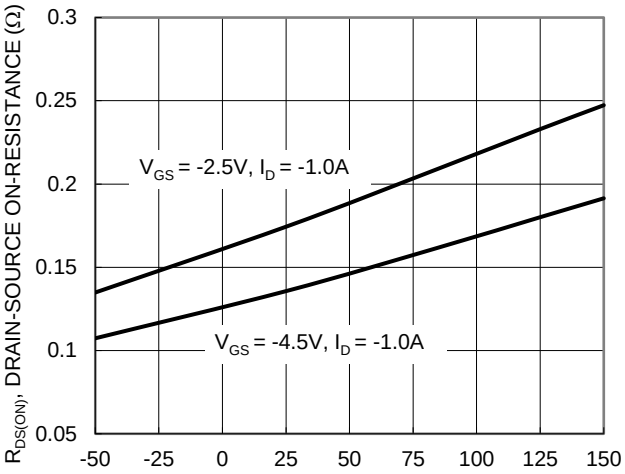


Figure 7. On-Resistance Variation with Junction Temperature

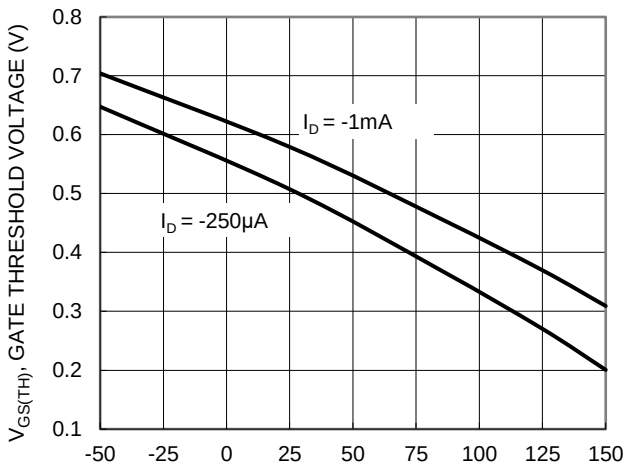


Figure 8. Gate Threshold Variation vs. Junction Temperature

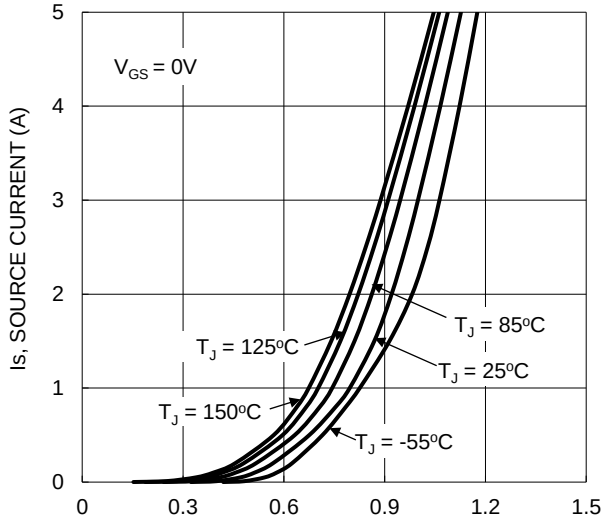


Figure 9. Diode Forward Voltage vs. Current

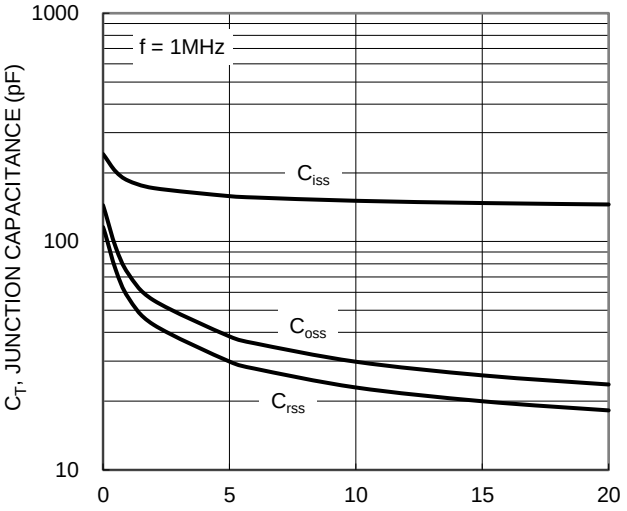


Figure 10. Typical Junction Capacitance

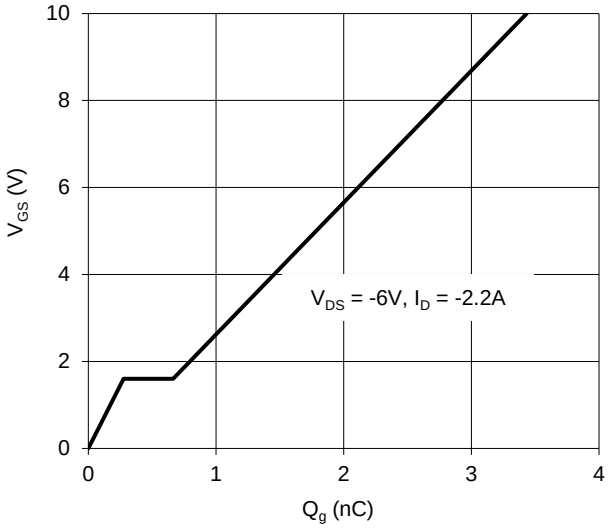


Figure 11. Gate Charge

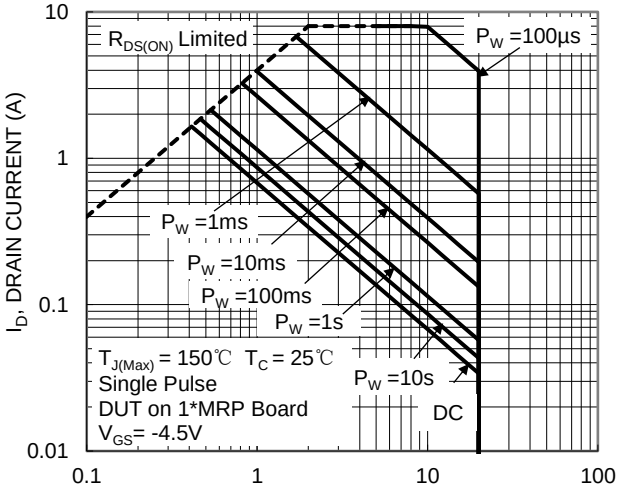


Figure 12. SOA, Safe Operation Area

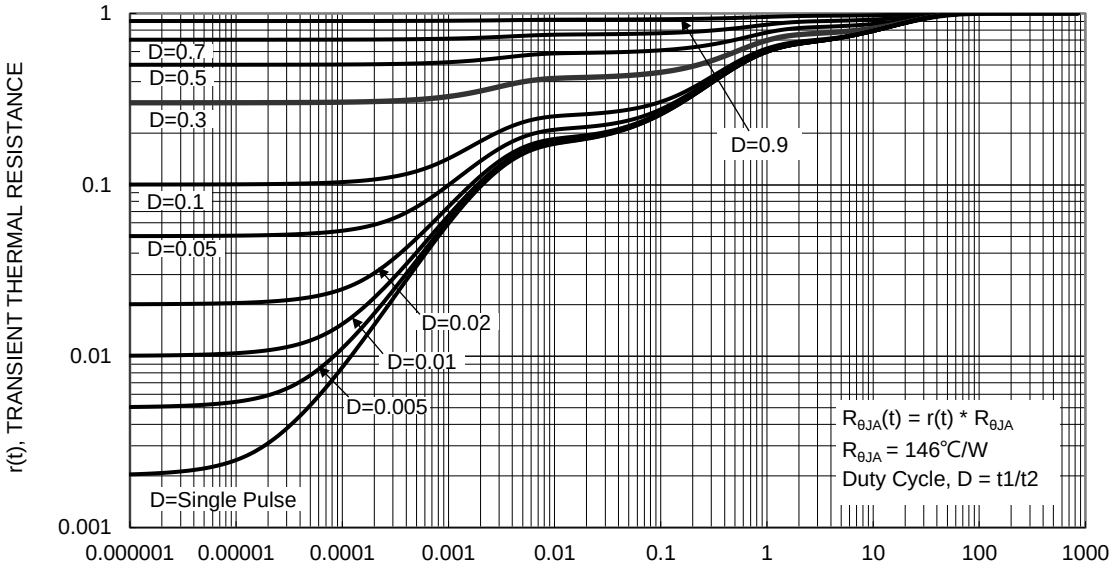
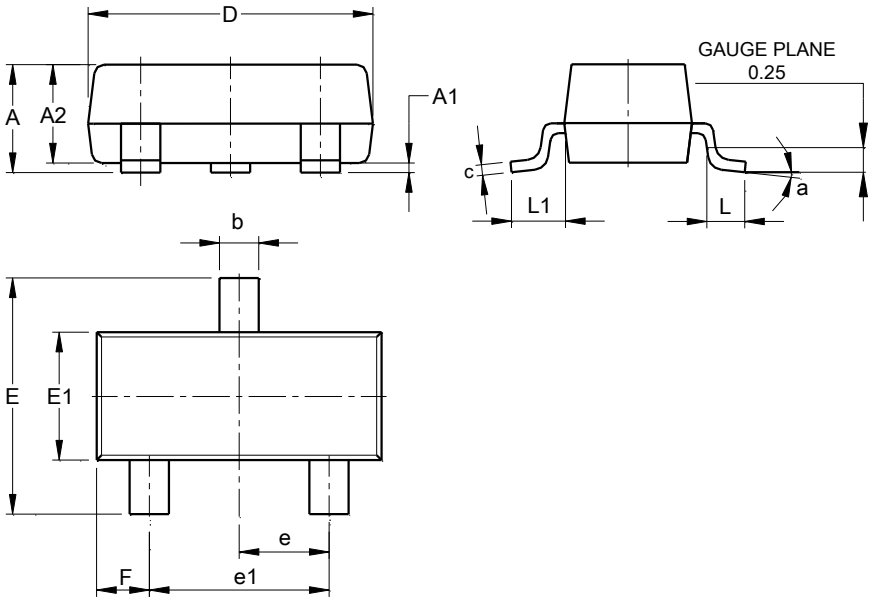


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

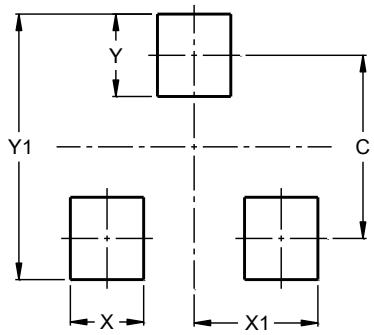
SOT23 (Standard)



SOT23 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.15	1.025
A1	0.00	0.10	0.05
A2	0.85	1.10	0.975
b	0.30	0.51	0.40
c	0.080	0.202	0.11
D	2.80	3.00	2.90
E	2.25	2.55	2.40
E1	1.20	1.40	1.30
e	0.89	1.03	0.915
e1	1.78	2.05	1.83
F	0.40	0.60	0.535
L1	0.45	0.61	0.55
L	0.25	0.55	0.40
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23 (Standard)



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9