优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
20V	90mΩ @ V_{GS} = 4.5V	2.8A
	120mΩ @ V_{GS} = 2.5V	2.4A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed

Description and Applications

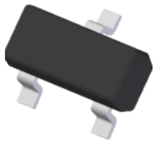
This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP, and is ideal for use in:

- Backlighting
- Power Management Functions
- DC-DC Converters
- Motor Control

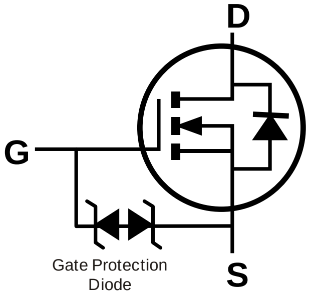
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminals Connections: See Diagram Below
- Weight: 0.009 grams (Approximate)

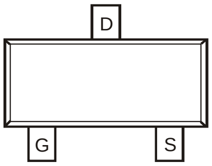
ESD Protected Gate



Top View



Internal Schematic



Top View

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 7) V_{GS} = 4.5V	Steady State	T_A = +25°C	I_D	2.8	A
		T_A = +70°C		2.2	
Maximum Continuous Body Diode Forward Current (Note 7)			I_S	1.1	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	12	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)		P_D	0.66	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	192	°C/W
Total Power Dissipation (Note 7)		P_D	1.1	W
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	115	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	10	µA	V_{DS} = 16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±10V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.3	0.6	1.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	61	90	mΩ	V_{GS} = 4.5V, I_D = 3.6A
			80	120		V_{GS} = 2.5V, I_D = 3.1A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1.0A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	130	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	26	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	18	—	pF	
Gate Resistance	R_g	—	2.7	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	1.4	—	nC	V_{DS} = 10V, I_D = 3.6A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	2.8	—	nC	
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.5	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	0.6	—	ns	V_{DS} = 10V, V_{GS} = 4.5V, R_g = 1Ω, R_L = 2.78Ω
Turn-On Rise Time	t_R	—	2.7	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	4.2	—	ns	
Turn-Off Fall Time	t_F	—	1.7	—	ns	
Reverse Recovery Time	t_{RR}	—	5.3	—	ns	I_F = 3.6A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	0.5	—	nC	I_F = 3.6A, di/dt = 100A/µs

Notes:
6. Device mounted on FR-4 PCB with minimum recommended pad layout.
7. Device mounted on 1” × 1” FR-4 PCB with high-coverage 2oz copper, single sided.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

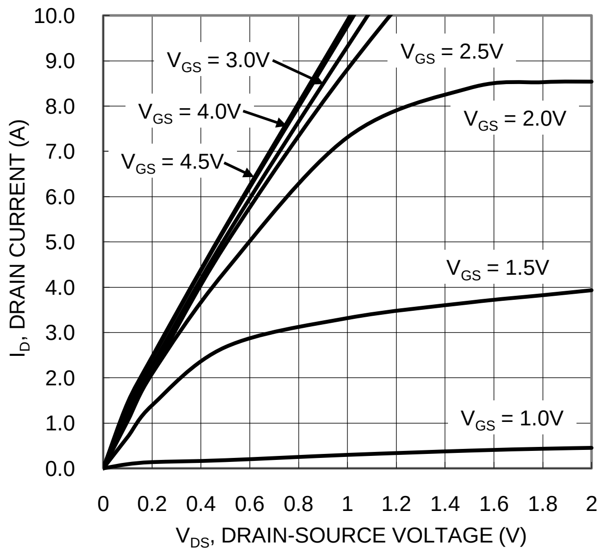


Figure 1. Typical Output Characteristic

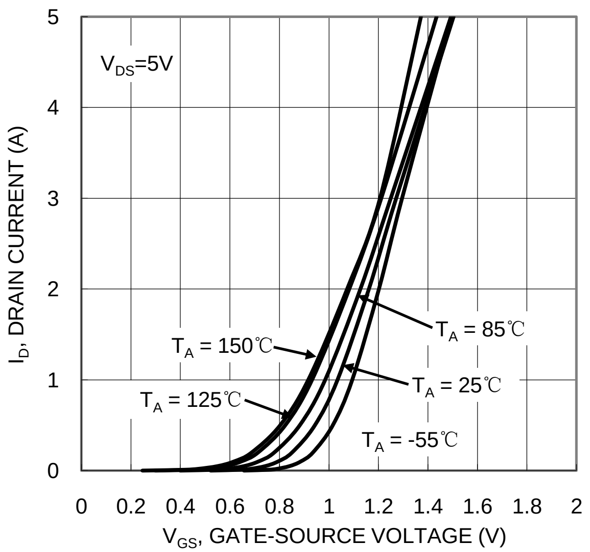


Figure 2. Typical Transfer Characteristic

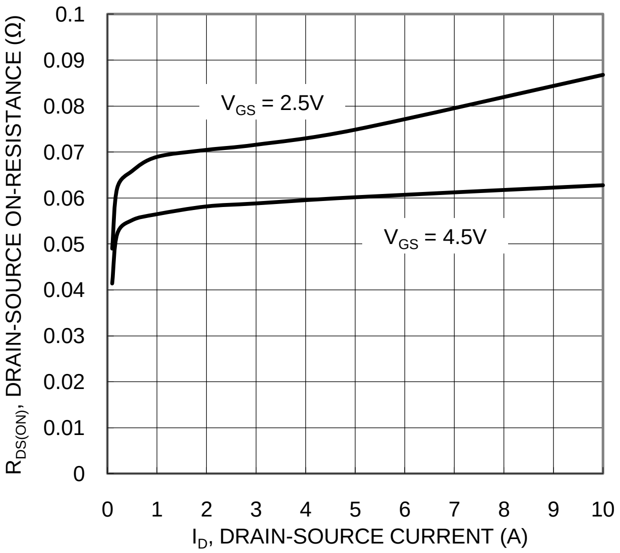


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

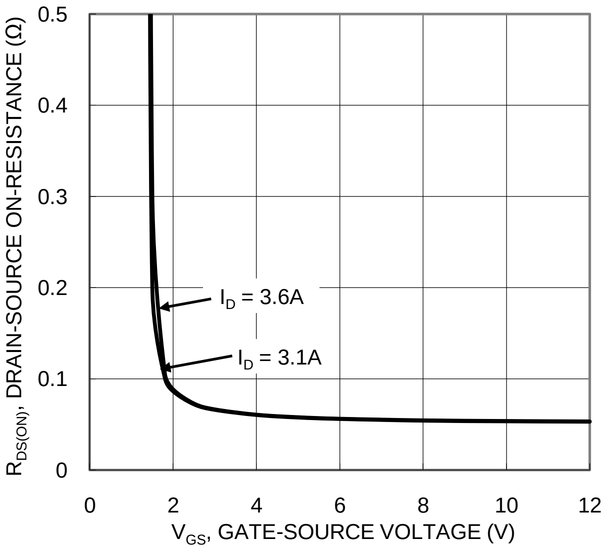


Figure 4. Typical Transfer Characteristic

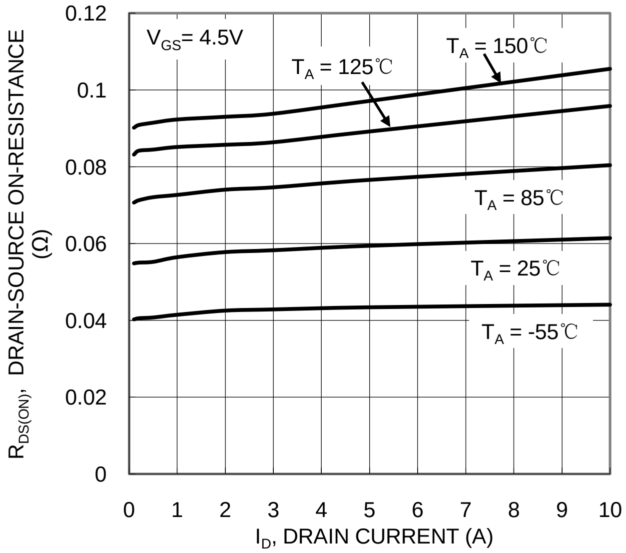


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

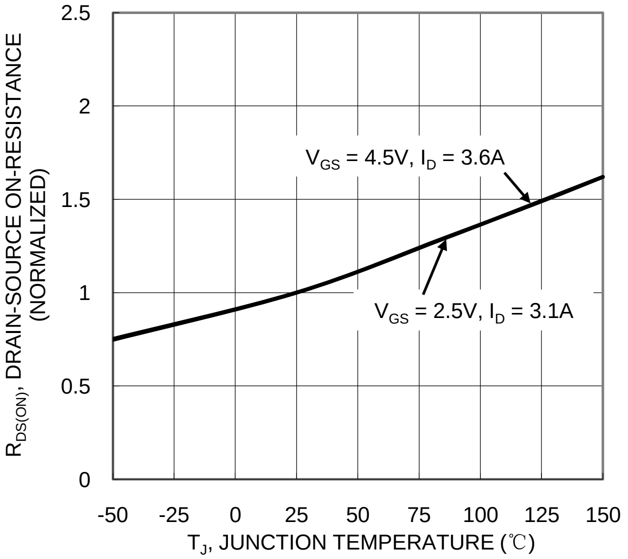


Figure 6. On-Resistance Variation with Junction Temperature

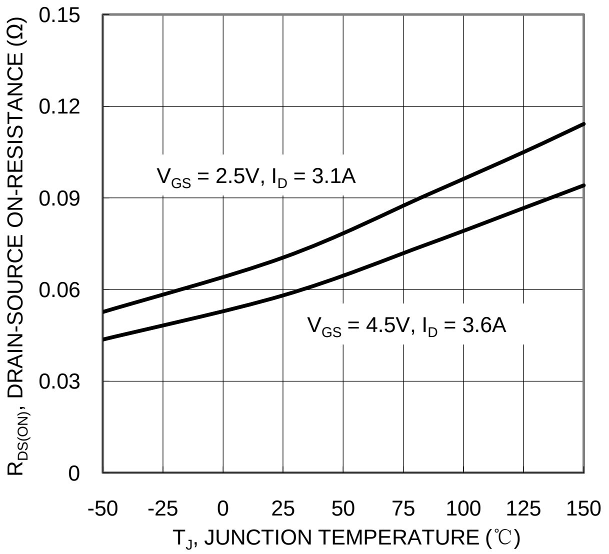


Figure 7. On-Resistance Variation with Junction Temperature

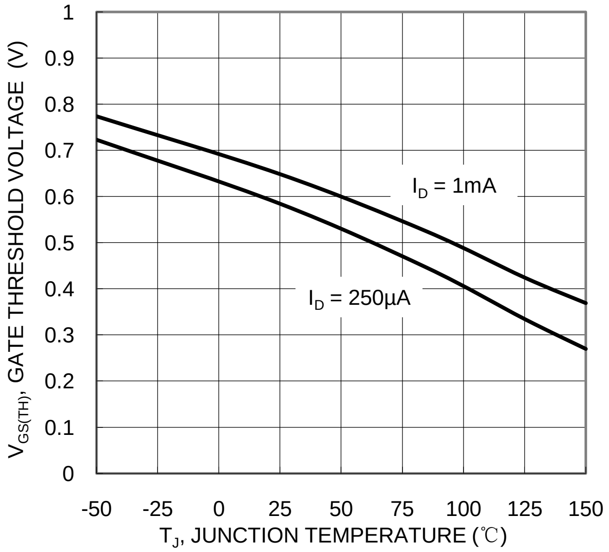


Figure 8. Gate Threshold Variation vs. Junction Temperature

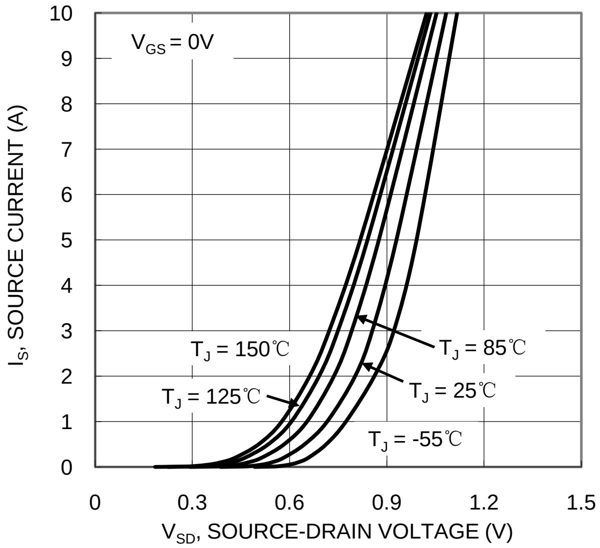


Figure 9. Diode Forward Voltage vs. Current

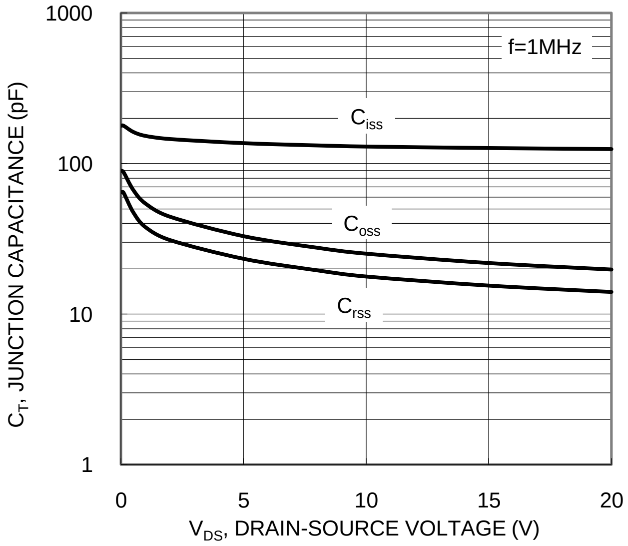


Figure 10. Typical Junction Capacitance

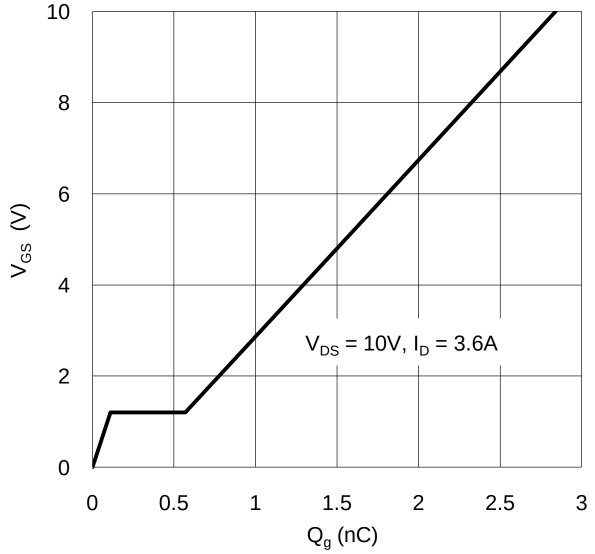


Figure 11. Gate Charge

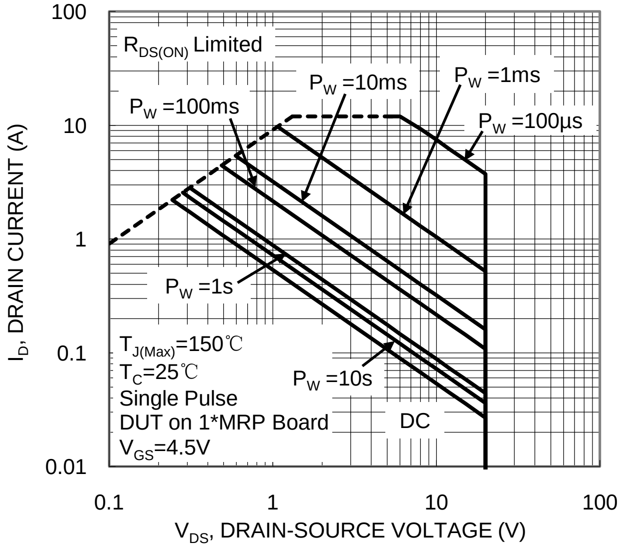


Figure 12. SOA, Safe Operation Area

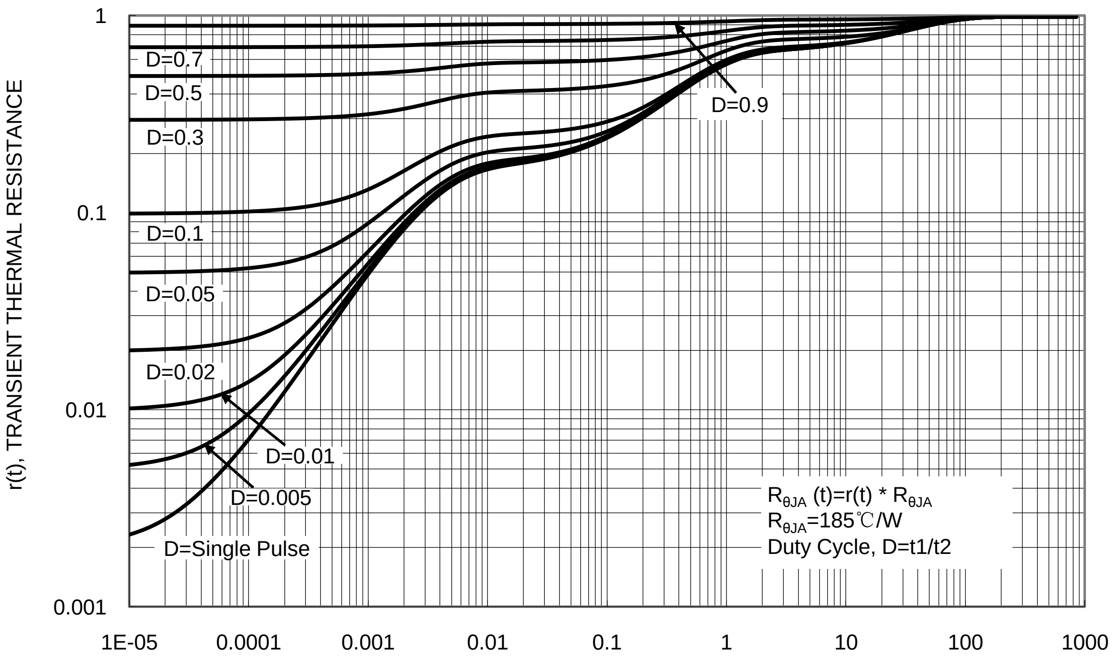
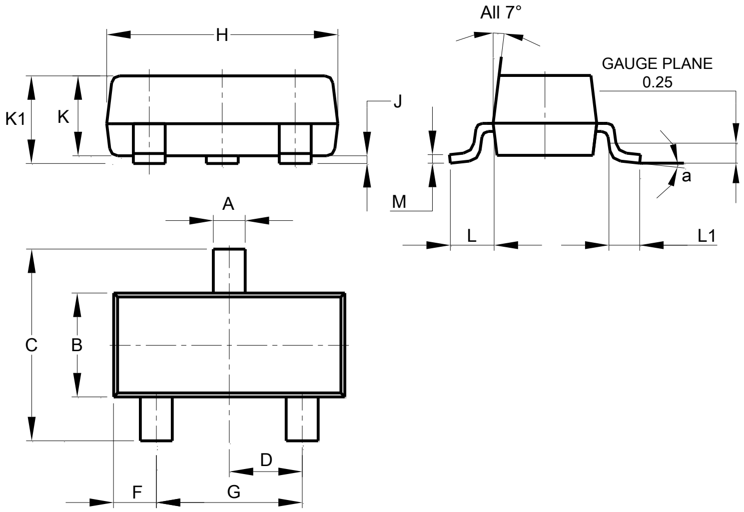


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

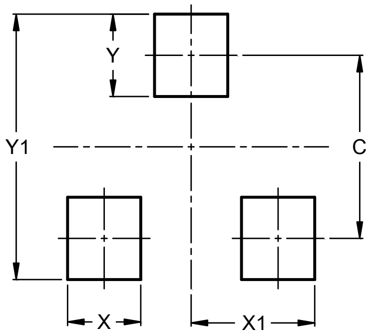
SOT23



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9