优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = +25°C
-25V	10Ω @ V_{GS} = -4.5V	-0.17A
	13Ω @ V_{GS} = -2.7V	-0.15A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions

Features

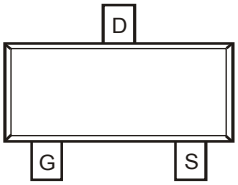
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surfaced Mount Package
- ESD Protected Gate (>6kV Human Body Model)

Mechanical Data

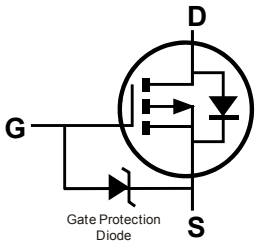
- Case: SOT23
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Solderable per MIL-STD-202, Method 208 e3
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

ESD HBM >6kV

Top View



Top View
Pin Configuration



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-25	V
Gate-Source Voltage			V_{GSS}	-8	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-0.17 -0.14	A
Continuous Drain Current (Note 6) V_{GS} = -2.7V	Steady State	T_A = +25°C T_A = +70°C	I_D	-0.15 -0.12	A
Pulsed Drain Current $T_P \le 300\mu s$, Duty Cycle = 2%)			I_{DM}	-0.5	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 5)	P_D	0.33	W
	(Note 6)		0.45	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	376	°C/W
	(Note 6)		275	
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	81	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-25	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = -8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.65	-0.96	-1.5	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	2.5	10	Ω	V_{GS} = -4.5V, I_D = -0.2A
		—	3	13		V_{GS} = -2.7V, I_D = -0.05A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	189	—	ms	V_{DS} = -5V, I_D = -0.2A
Diode Forward Voltage (Note 7)	V_{SD}	—	—	-1.5	V	V_{GS} = 0V, I_S = -0.2A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	27.2	—	pF	V_{DS} = -10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	6.1	—		
Reverse Transfer Capacitance	C_{rss}	—	1.7	—		
Total Gate Charge	Q_g	—	0.35	—	nC	V_{DS} = -5V, I_D = -0.2A, V_{GS} = -4.5V,
Gate-Source Charge	Q_{gs}	—	0.08	—		
Gate-Drain Charge	Q_{gd}	—	0.06	—		
Turn-On Delay Time	$t_{d(on)}$	—	4.5	—	ns	V_{GS} = -4.5V, V_{DD} = -6V I_D = -0.2A, R_G = 50Ω
Rise Time	t_r	—	2.3	—		
Turn-Off Delay Time	$t_{d(off)}$	—	24.1	—		
Fall Time	t_f	—	11.0	—		

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

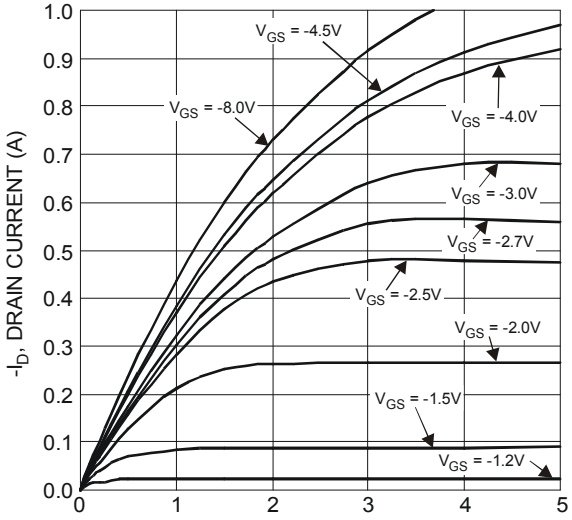


Figure 1 Typical Output Characteristics

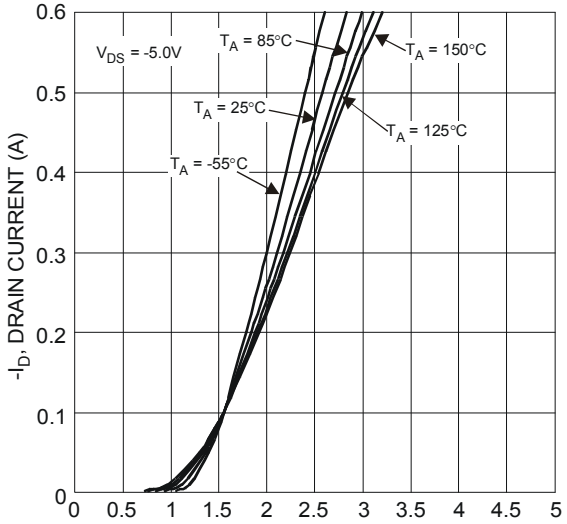


Figure 2 Typical Transfer Characteristics

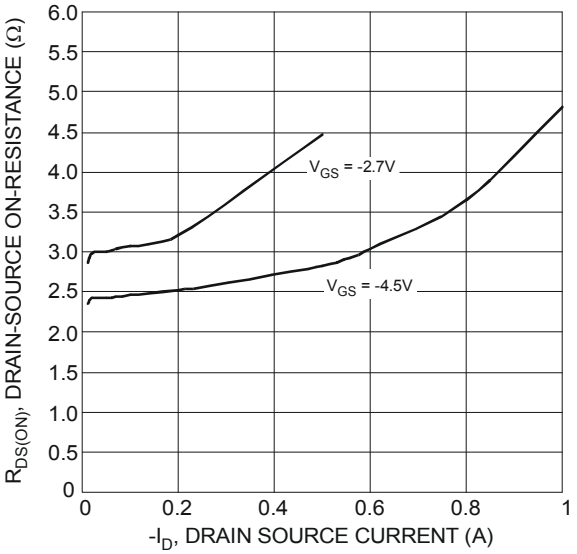


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

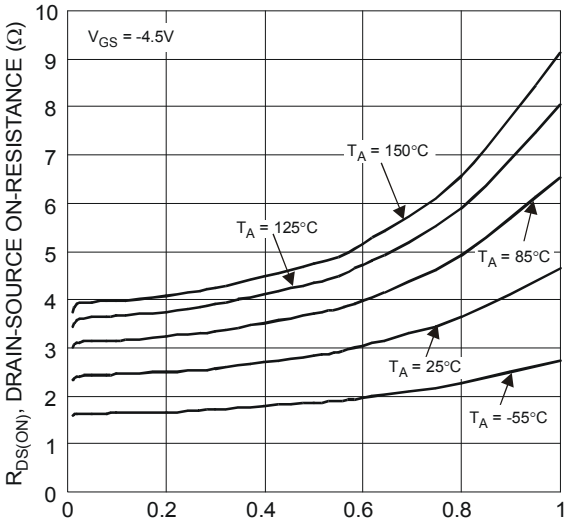


Figure 4 Typical On-Resistance vs.
Drain Current and Temperature

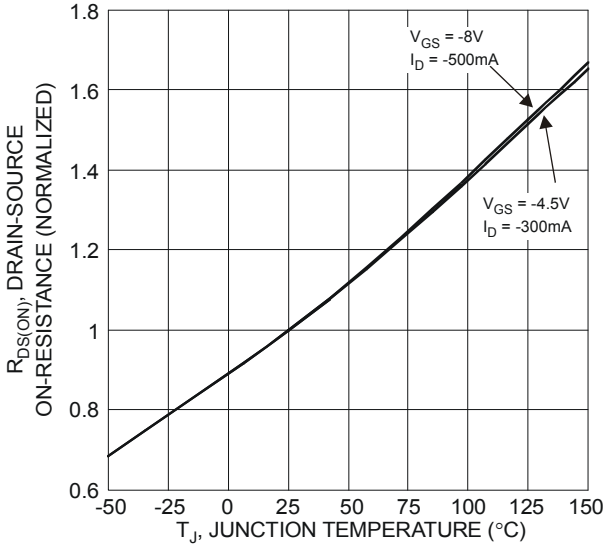


Figure 5 On-Resistance Variation with Temperature

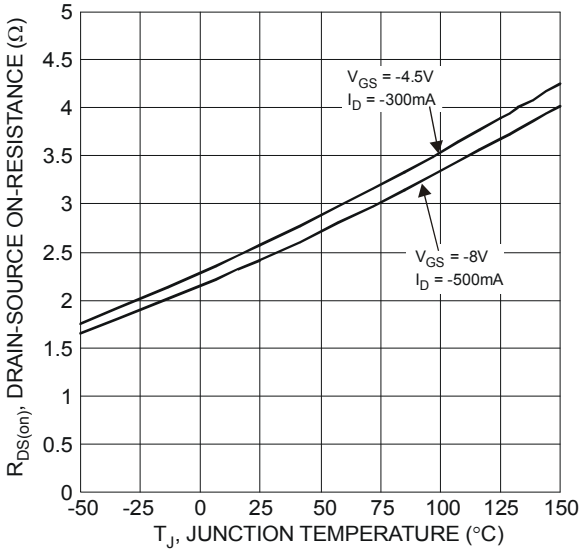


Figure 6 On-Resistance Variation with Temperature

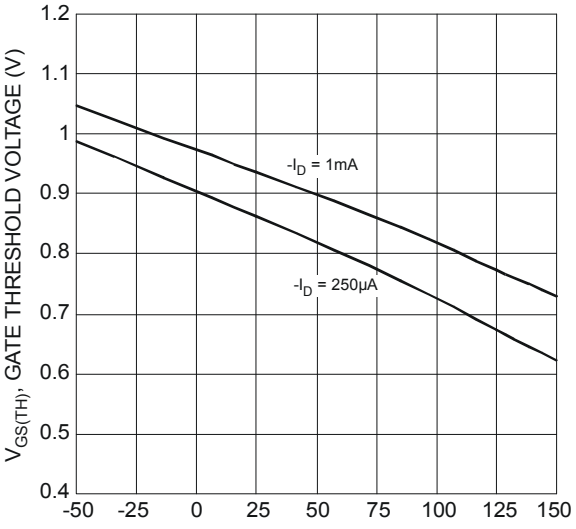


Figure 7 Gate Threshold Variation vs. Ambient Temperature

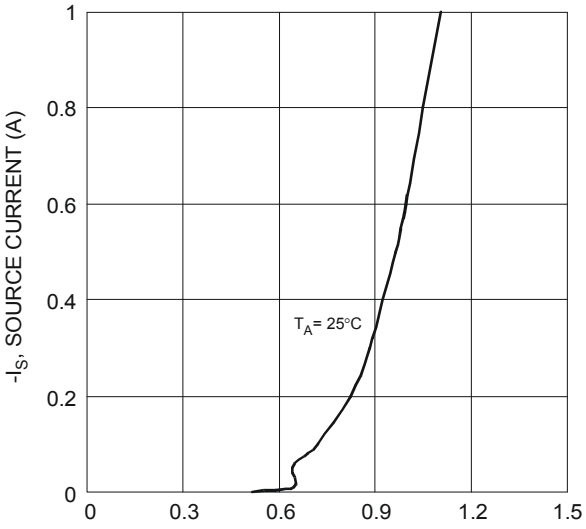


Figure 8 Diode Forward Voltage vs. Current

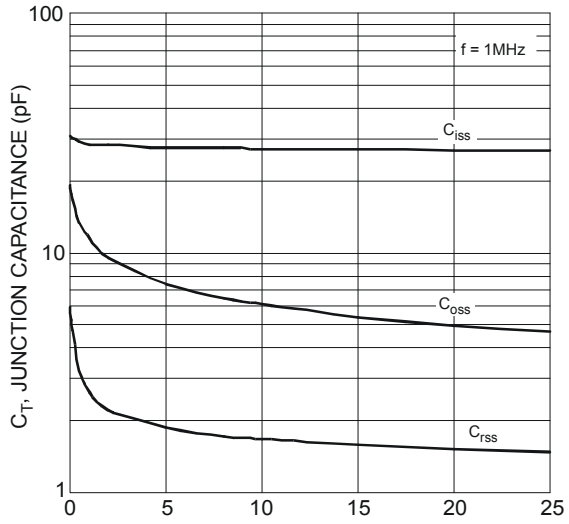


Figure 9 Typical Junction Capacitance

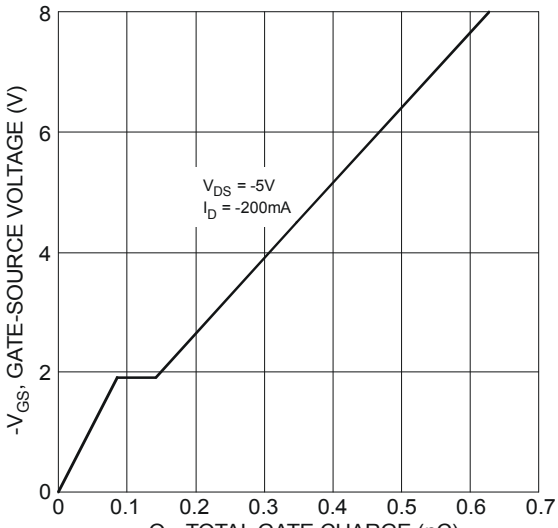


Figure 10 Gate-Charge Characteristics

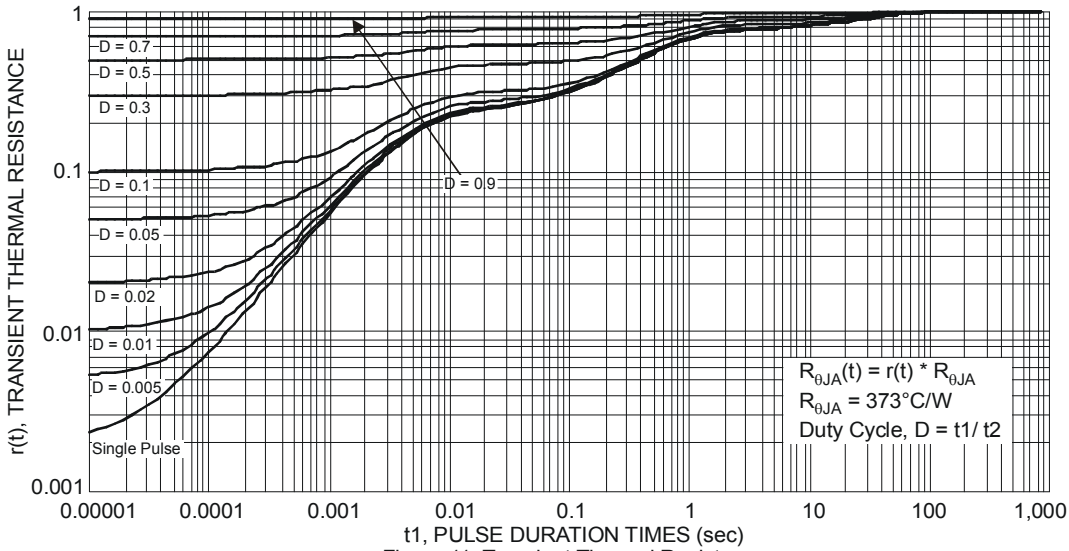
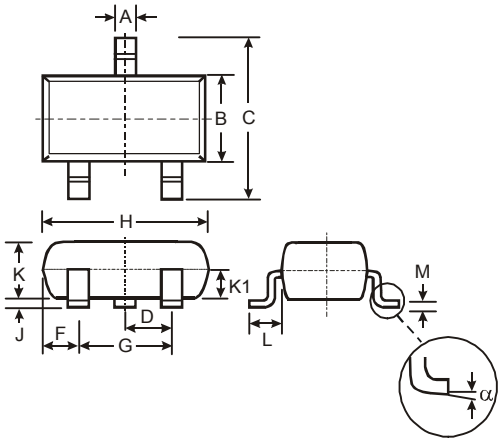


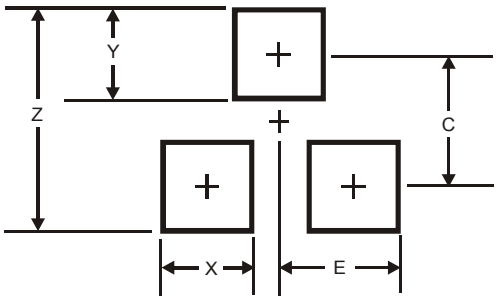
Figure 11 Transient Thermal Resistance

Package Outline Dimensions



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35