优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
20V	16mΩ @ V_{GS} = 4.5V	9.8A
	23mΩ @ V_{GS} = 2.5V	8.7A

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP, and is ideal for use in:

- Backlighting
- Power management functions
- DC-DC converters

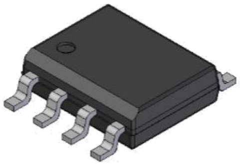
Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected up to 2kV
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application

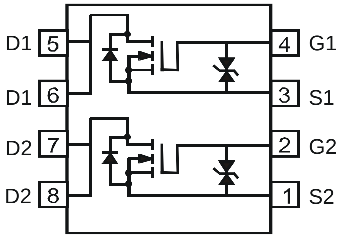
Mechanical Data

- Package: SO-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish- Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram Below
- Weight: 0.072 grams (Approximate)

ESD PROTECTED TO 2kV



Top View



Top View
Internal Schematic

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 5)	Steady State	T_A = +25°C T_A = +85°C	I_D	9.5 7.1	A
Pulsed Drain Current (Note 6)			I_{DM}	30	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	1.28	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{\theta JA}$	99.3	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = +25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	μA	V_{DS} = 20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	1.0	1.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	11 17	16 23	mΩ	V_{GS} = 4.5V, I_D = 9.4A V_{GS} = 2.5V, I_D = 8.3A
Forward Transfer Admittance	$\lvert Y_{fs}\rvert$	—	17	—	S	V_{DS} = 5V, I_D = 9.4A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1.3A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1149	—	pF	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	157	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	142	—	pF	
Gate Resistance	R_g	—	1.51	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	11.6	—	nC	V_{DS} = 10V, I_D = 9.4A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	26	—	nC	
Gate-Source Charge	Q_{gs}	—	2.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.4	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	11.67	—	ns	V_{DD} = 10V, V_{GS} = 4.5V, R_{GEN} = 6Ω, I_D = 1A
Turn-On Rise Time	t_r	—	12.49	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	35.89	—	ns	
Turn-Off Fall Time	t_f	—	12.33	—	ns	

Notes:
5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Repetitive rating, pulse width limited by junction temperature.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

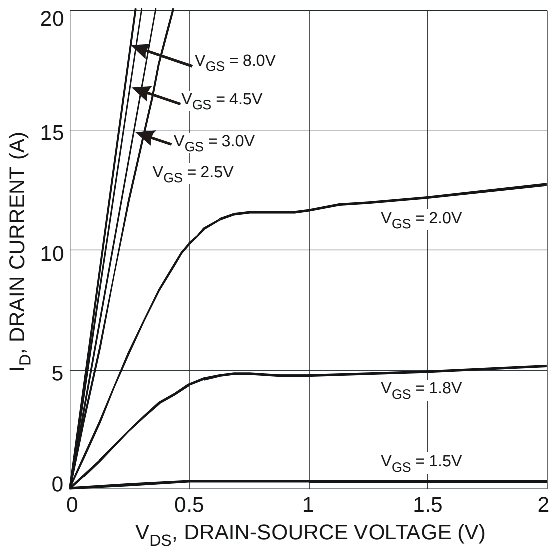


Fig. 1 Typical Output Characteristic

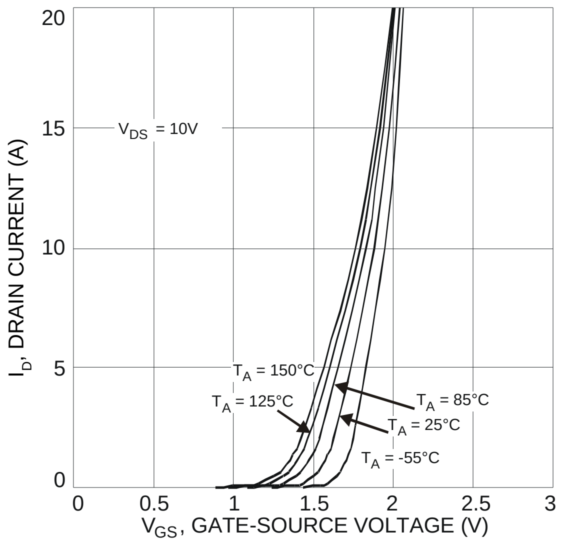


Fig. 2 Typical Transfer Characteristic

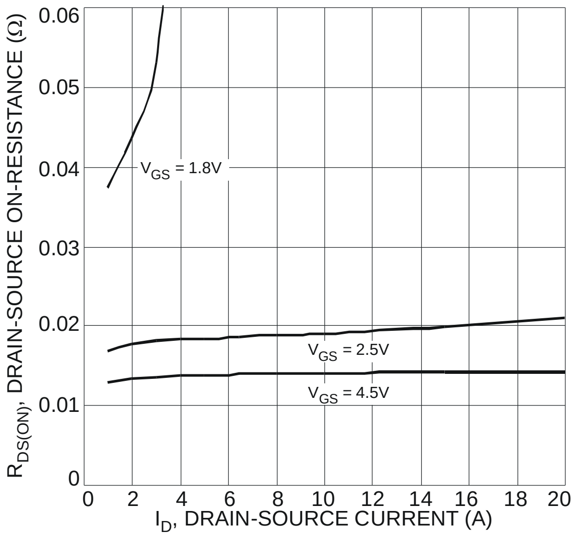


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

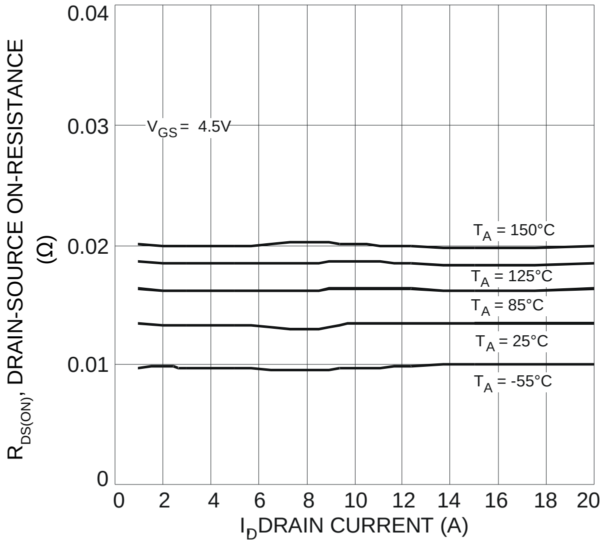


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

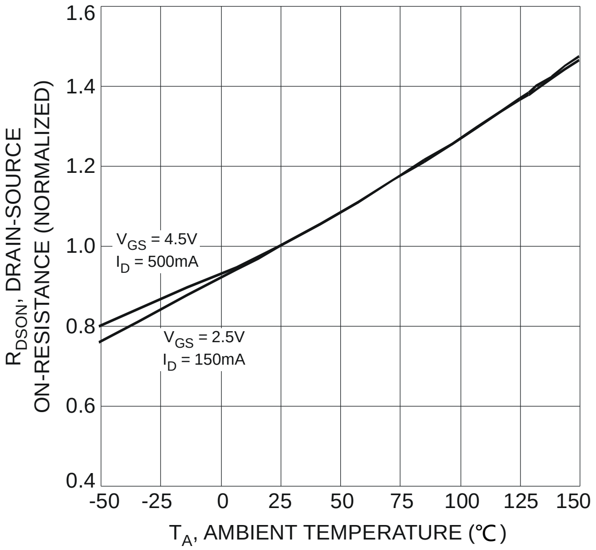


Fig. 5 On-Resistance Variation with Temperature

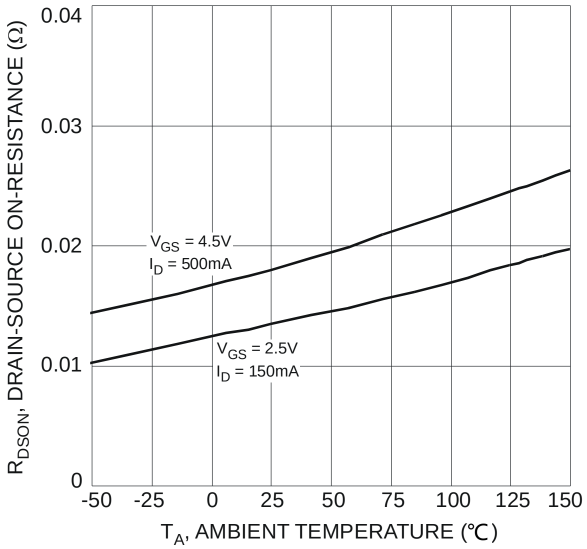


Fig. 6 On-Resistance Variation with Temperature

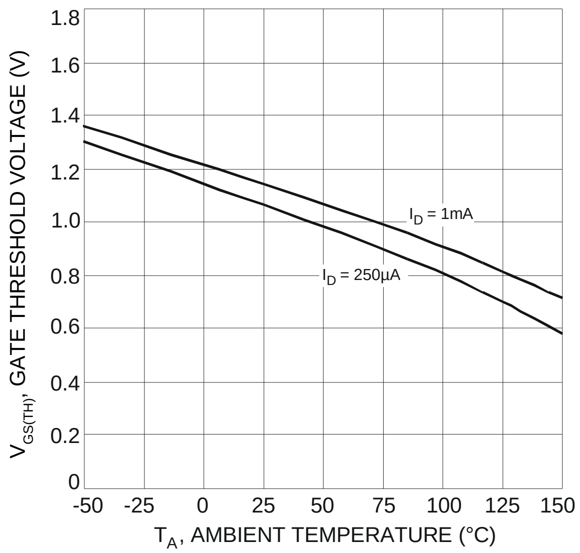


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

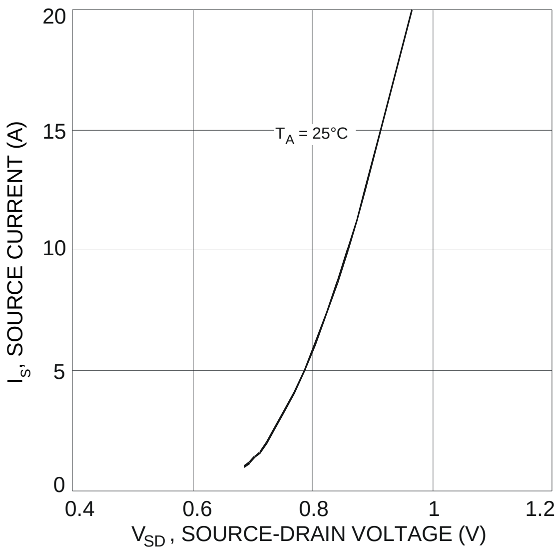


Fig. 8 Diode Forward Voltage vs. Current

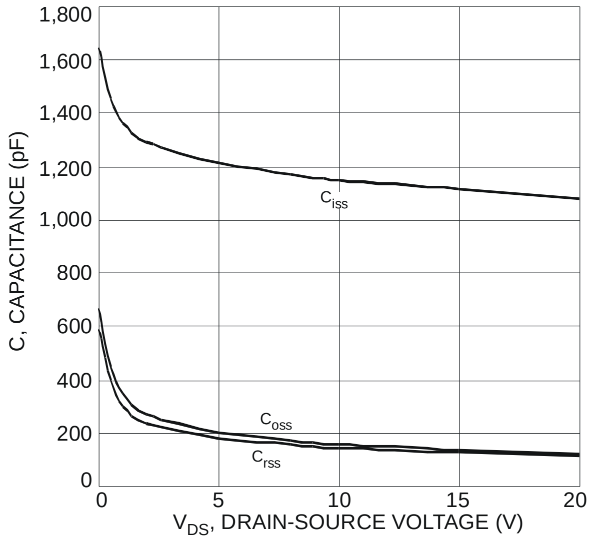


Fig. 9 Typical Total Capacitance

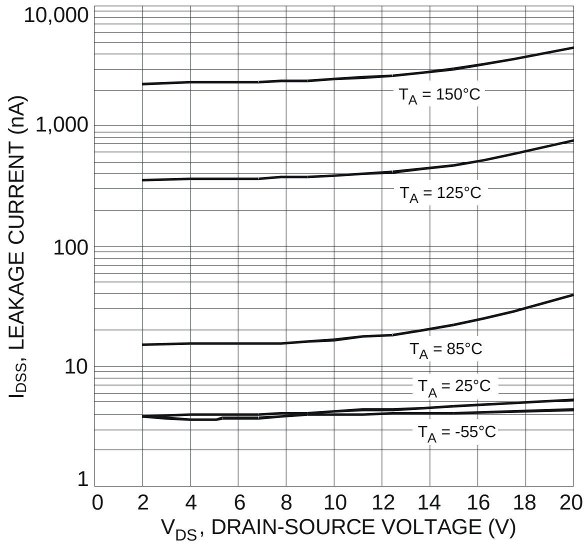


Fig. 10 Typical Leakage Current
vs. Drain-Source Voltage

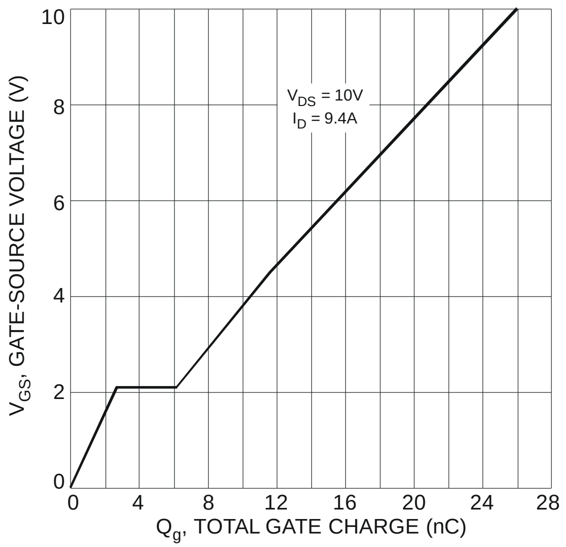


Fig. 11 Gate-Source Voltage vs. Total Gate Charge

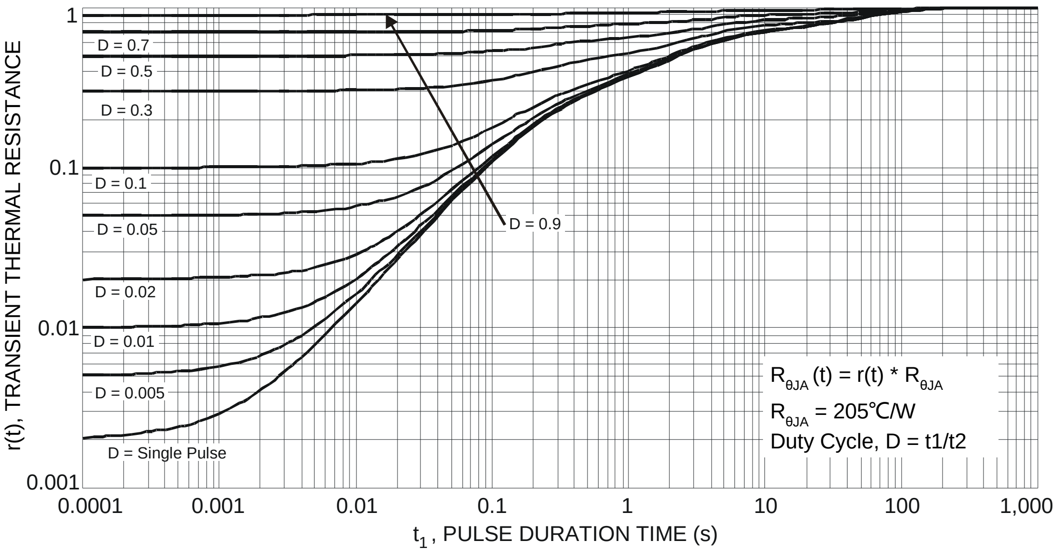
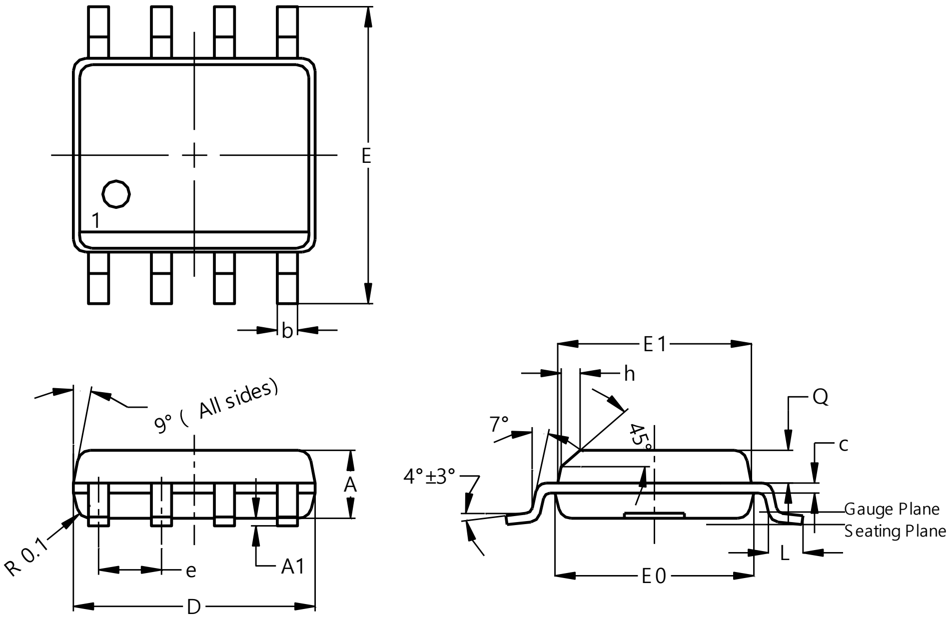


Fig. 12 Transient Thermal Response

Package Outline Dimensions

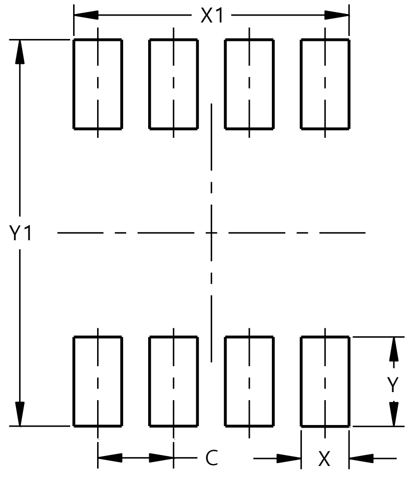
SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50