



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



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Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
-20V	75mΩ @ V _{GS} = -4.5V	-4.6A
	110mΩ @ V _{GS} = -2.5V	-2.9A

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description

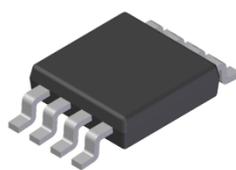
This MOSFET has been designed to minimize the on-state resistance yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

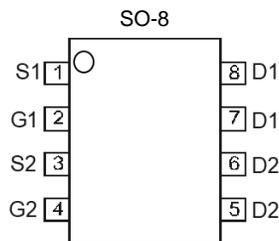
- Backlighting
- Power-management functions
- DC-DC converters

Mechanical Data

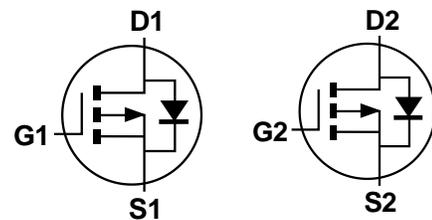
- Package: SO-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.072 grams (Approximate)



Top View



Top View



P-Channel MOSFET

P-Channel MOSFET

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	± 12	V
Continuous Drain Current (Note 5) $V_{GS} = -4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	-4.6	A
		$T_A = +85^\circ\text{C}$		-3	
Pulsed Drain Current (Note 6)			I_{DM}	-20	A

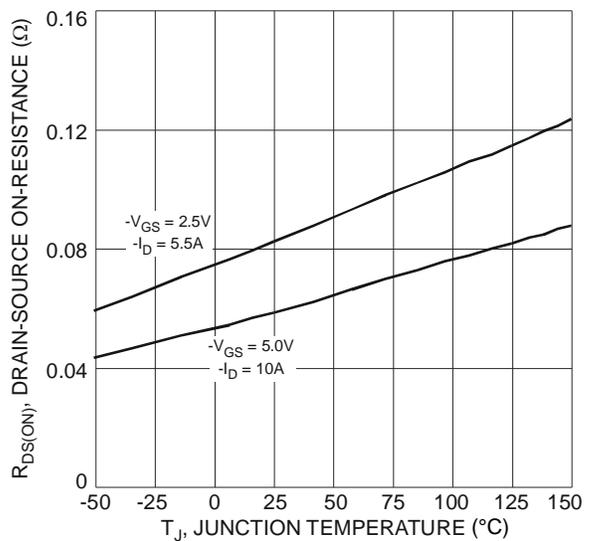
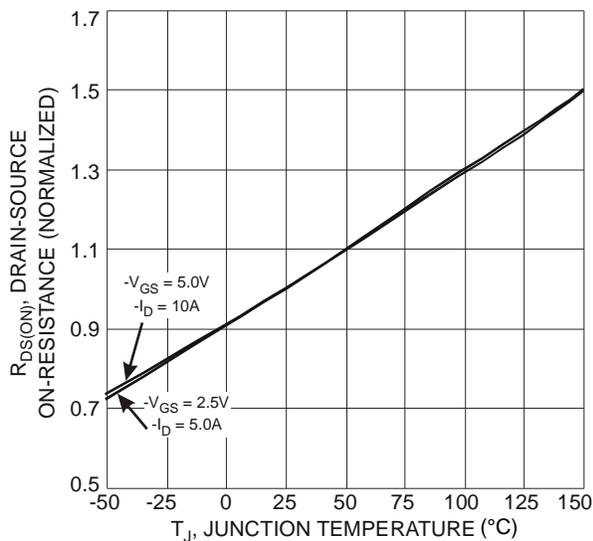
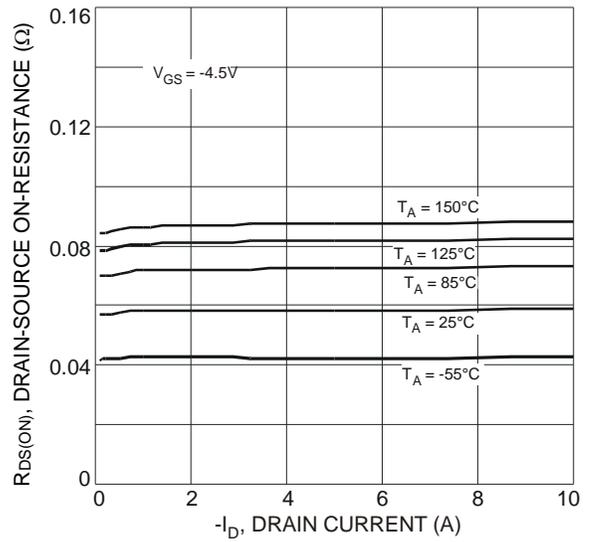
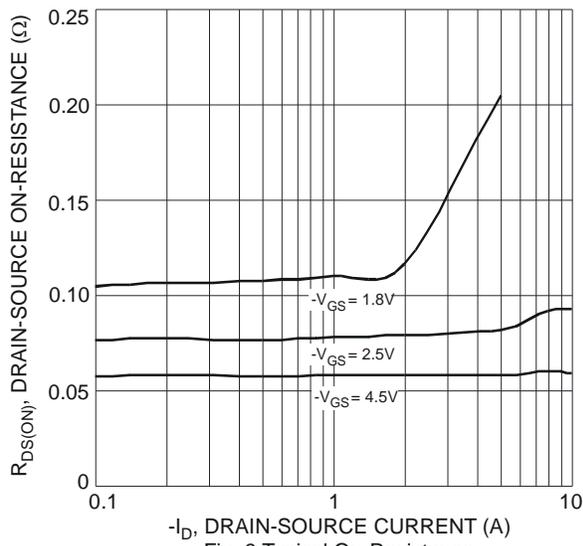
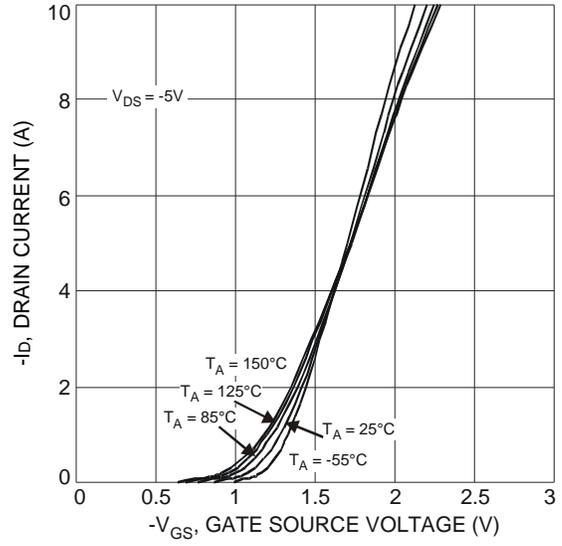
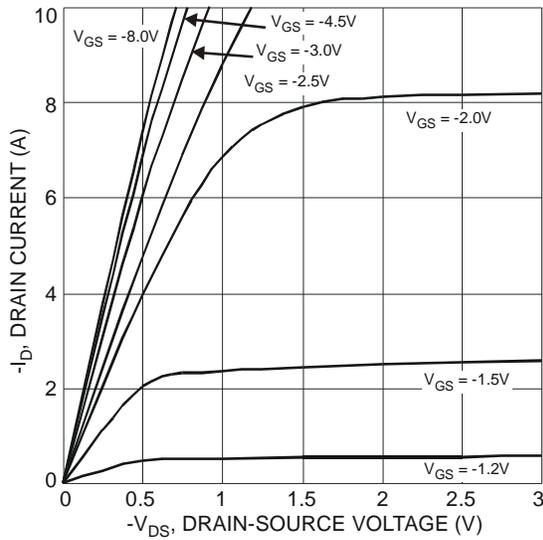
Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	1.15	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	109	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	-1	μA	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.45	—	-1.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	55	75	m Ω	$V_{GS} = -4.5\text{V}, I_D = -4.8\text{A}$
		—	76	110		$V_{GS} = -2.5\text{V}, I_D = -1\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	10	—	S	$V_{DS} = -9\text{V}, I_D = -3.4\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.8	-1.2	V	$V_{GS} = 0\text{V}, I_S = -2\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	608.4	—	pF	$V_{DS} = -6\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	81.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	72.4	—	pF	
Gate Resistance	R_g	—	44.91	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_g	—	6.5	—	nC	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $I_D = -3.2\text{A}$
Gate-Source Charge	Q_{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.5	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	12.45	—	ns	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $R_L = 10\Omega, R_G = 1\Omega, I_D = -1\text{A}$
Turn-On Rise Time	t_r	—	10.29	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	46.52	—	ns	
Turn-Off Fall Time	t_f	—	22.19	—	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
 - Repetitive rating, pulse width limited by junction temperature.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.



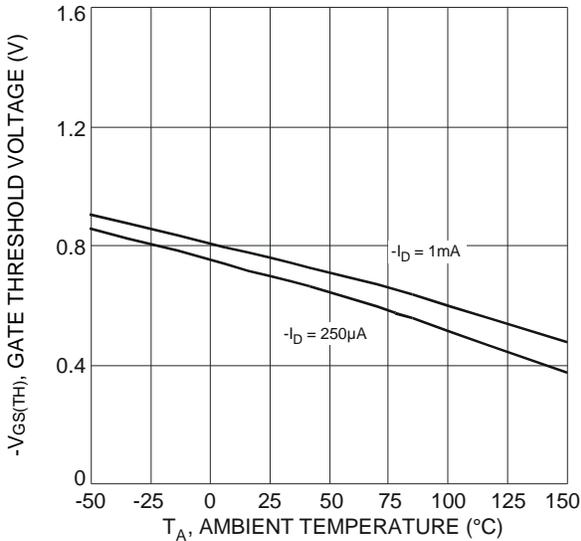


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

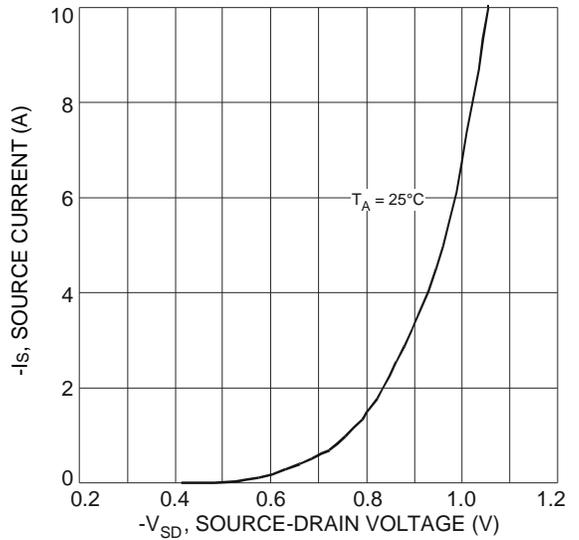


Fig. 8 Diode Forward Voltage vs. Current

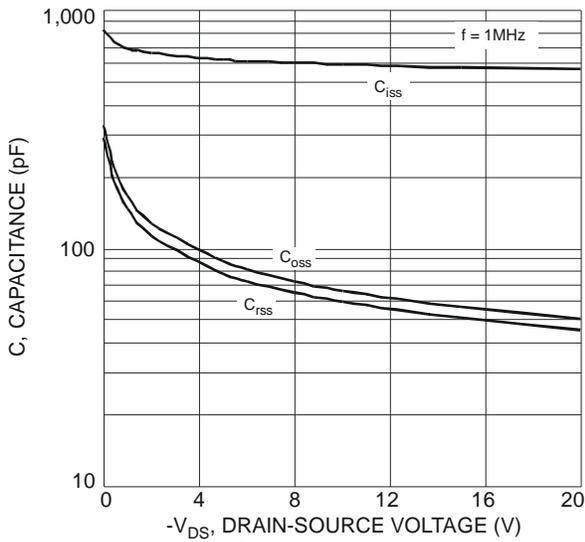


Fig. 9 Typical Total Capacitance

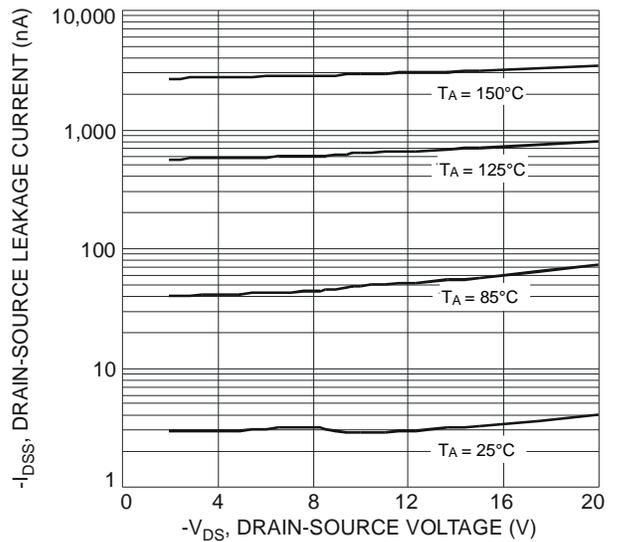


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

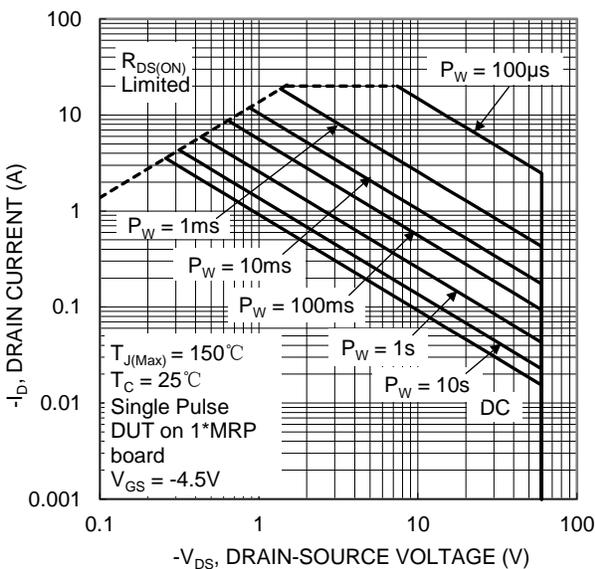


Fig. 11 SOA, Safe Operation Area

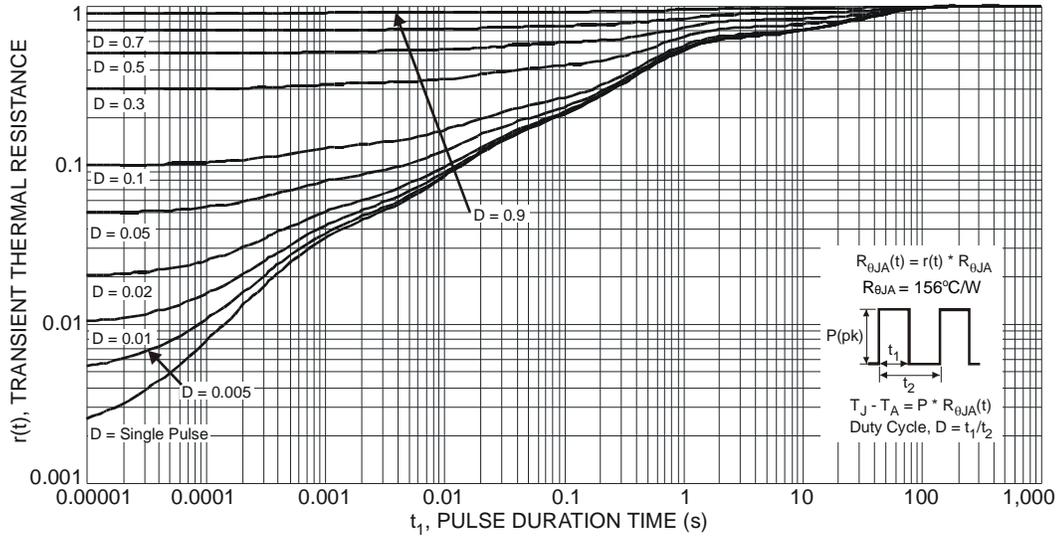
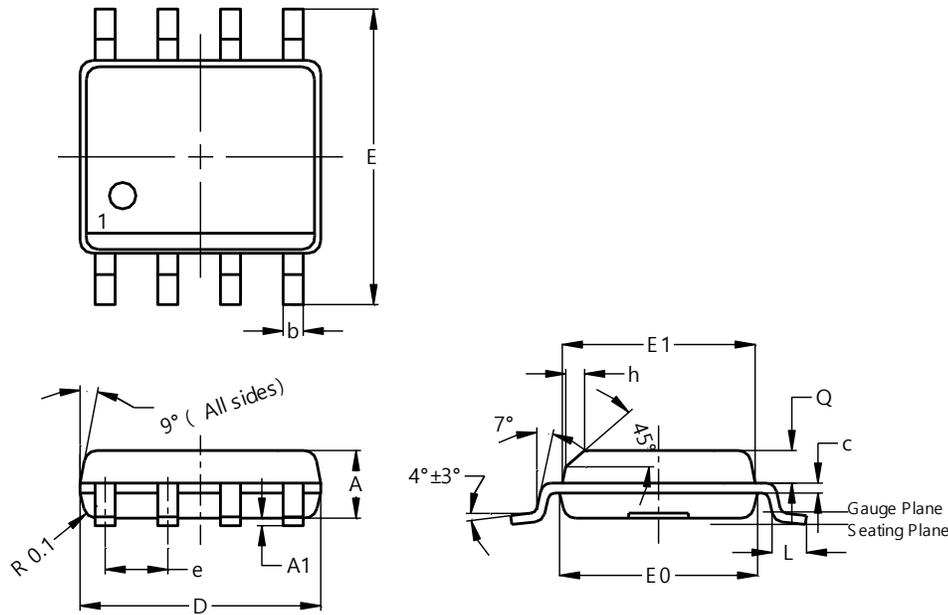


Fig. 12 Transient Thermal Resistance

Package Outline Dimensions

SO-8

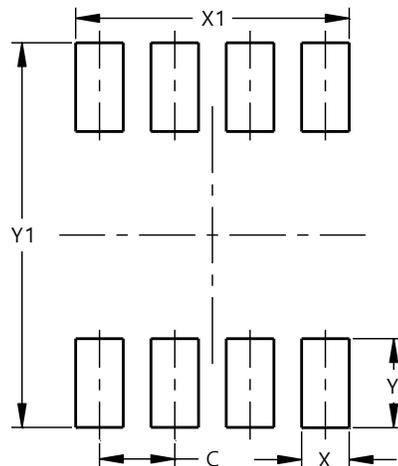


SO-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

Suggested Pad Layout

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50