优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

企业微信二维码

企业QQ二维码

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
30V	60mΩ @ V_{GS} = 10V	2.7A
	100mΩ @ V_{GS} = 4.5V	2.1A

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- DC-DC Converters
- Analog Switch

Features and Benefits

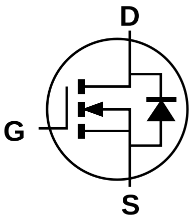
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed

Mechanical Data

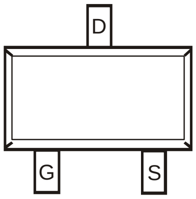
- Case: SOT323
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.027 grams (Approximate)

SOT323

Top View



Equivalent Circuit



Top View

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	2.7 2.2	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	22	A
Maximum Body Diode Forward Current (Note 5)			I_S	0.67	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.49	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	254	°C/W
Total Power Dissipation (Note 6)		P_D	0.65	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	191	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DSS}	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.8	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	41	60	mΩ	V_{GS} = 10V, I_D = 3.1A
		—	48	100		V_{GS} = 4.5V, I_D = 2A
		—	56	200		V_{GS} = 3.3V, I_D = 1.5A
Diode Forward Voltage	V_{SD}	—	0.7	1	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	278	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	44	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	29	—	pF	
Gate Resistance	R_g	—	4.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	3.5	—	nC	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 3A
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.3	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.7	—	ns	V_{GS} = 10V, V_{DS} = 15V, R_G = 3Ω, R_L = 1.7Ω
Turn-On Rise Time	t_R	—	97	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	12.6	—	ns	
Turn-Off Fall Time	t_F	—	51	—	ns	

Notes:
5. Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

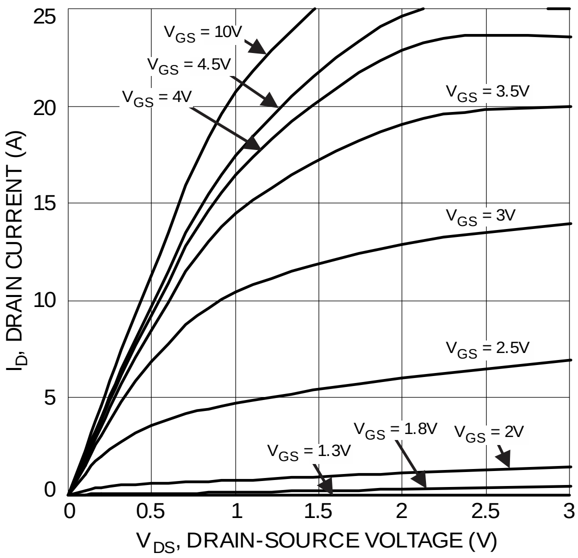


Figure 1 Typical Output Characteristic

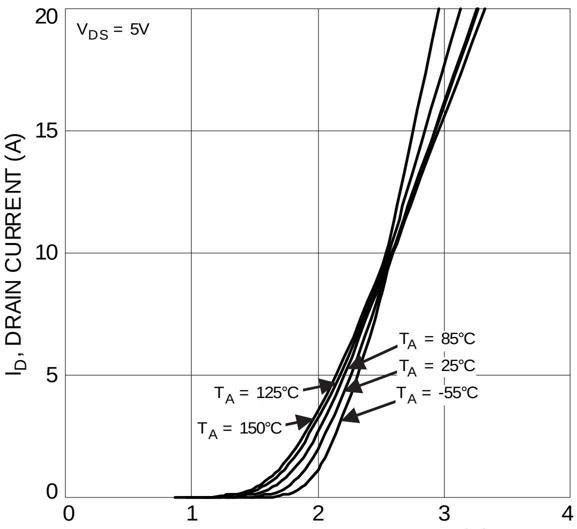


Figure 2 Typical Transfer Characteristics

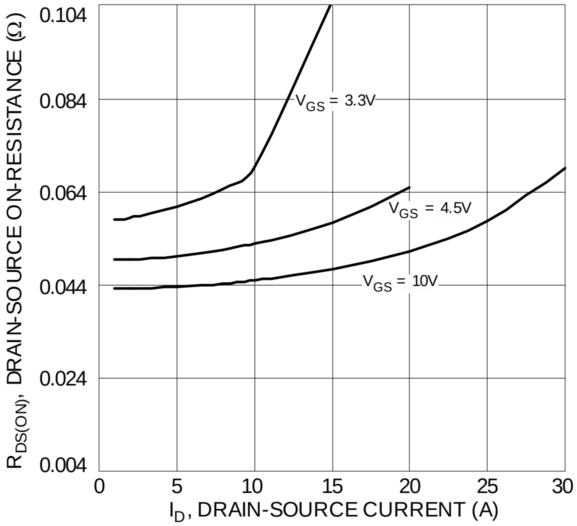


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

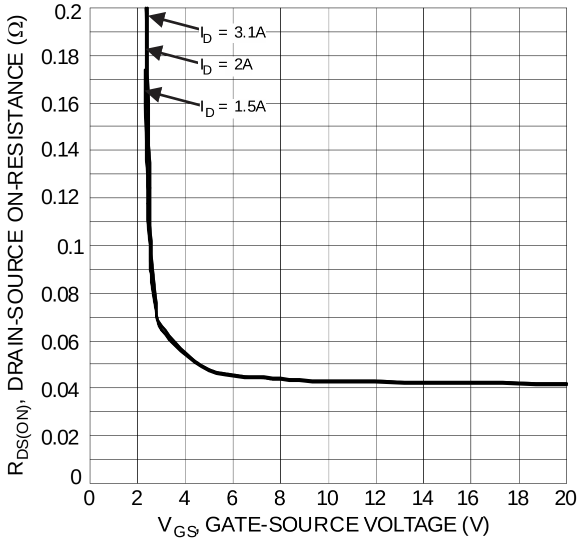


Figure 4 Typical Drain-Source On-Resistance
vs. Gate-Source Voltage

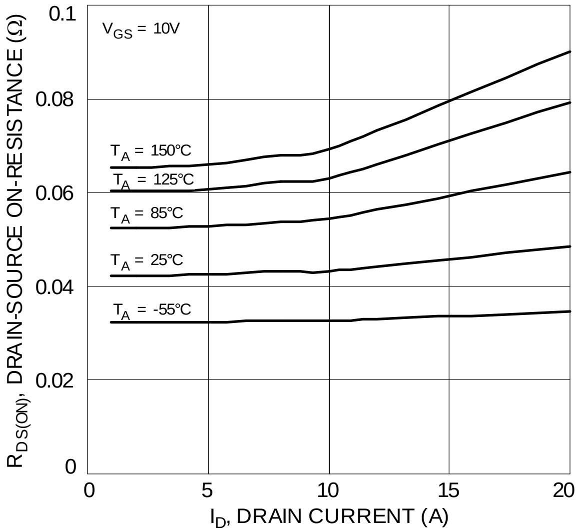


Figure 5 Typical On-Resistance vs.
Drain Current and Temperature

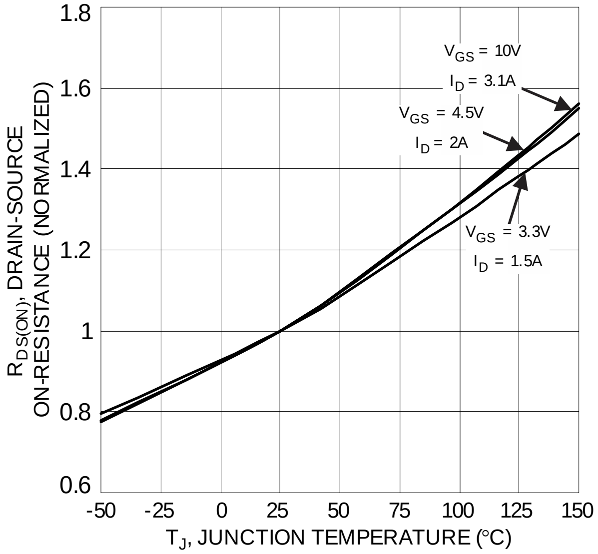


Figure 6 On-Resistance Variation with Temperature

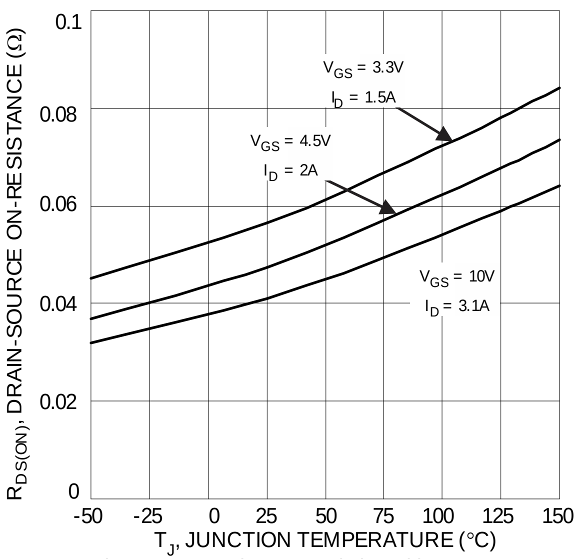


Figure 7 On-Resistance Variation with Temperature

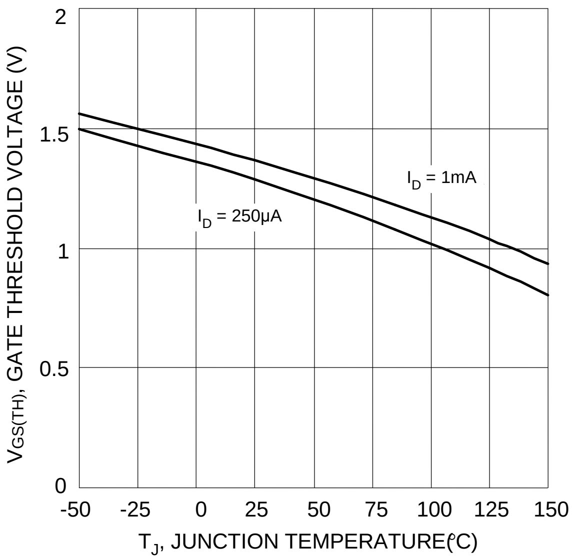


Figure 8 Gate Threshold Variation vs. Junction Temperature

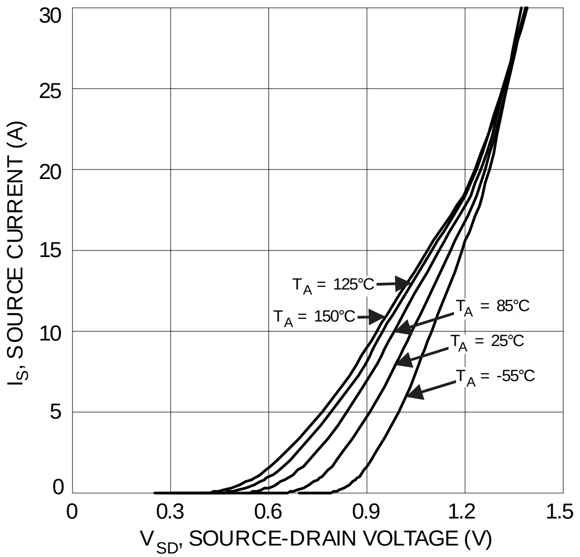


Figure 9 Diode Forward Voltage vs. Current

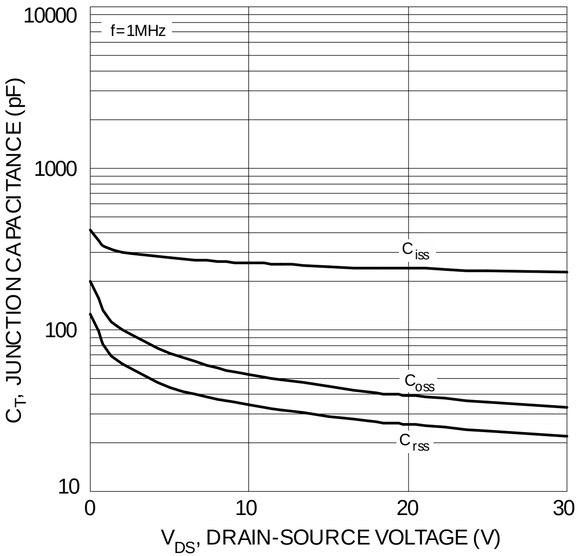


Figure 10 Typical Junction Capacitance

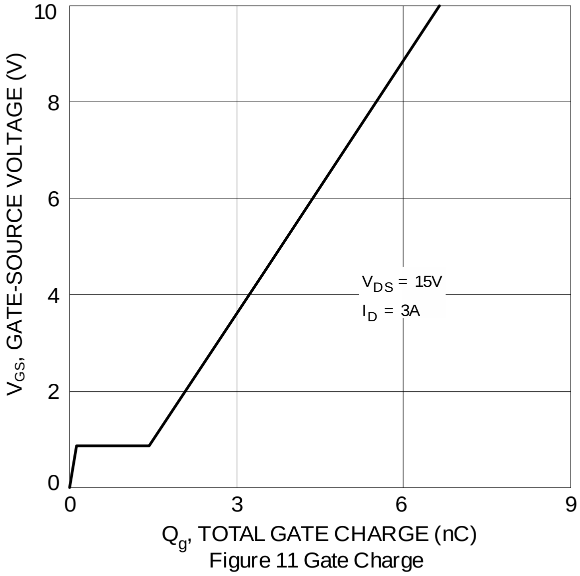


Figure 11 Gate Charge

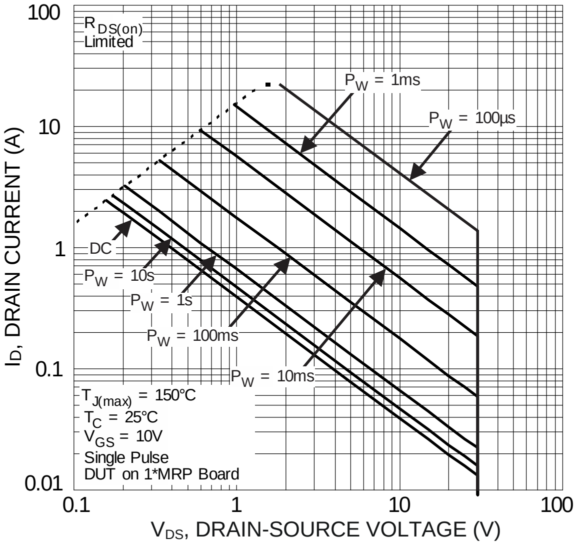


Figure 12 SOA, Safe Operation Area

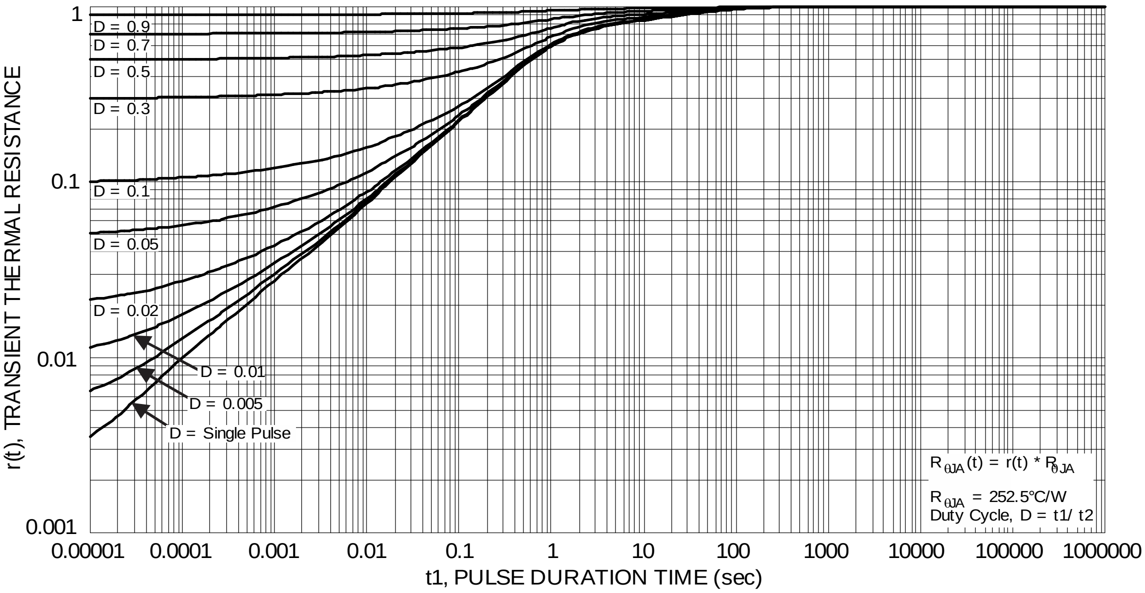
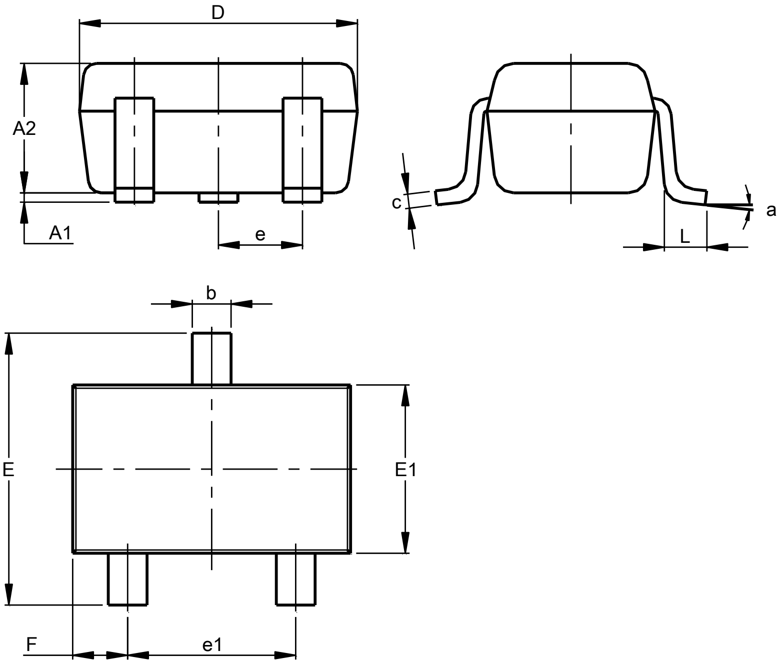


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

SOT323



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Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.25	0.40	0.30
c	0.10	0.18	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
e1	1.20	1.40	1.30
F	0.375	0.475	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

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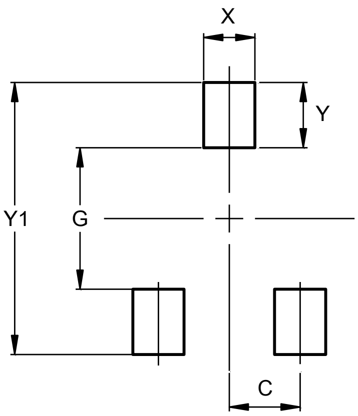

Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.470
Y	0.600
Y1	2.500