



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
30V	67mΩ @ V _{GS} = 4.5V	3.6A
	70mΩ @ V _{GS} = 4.0V	3.5A
	98mΩ @ V _{GS} = 2.5V	3.0A

Description

This new generation MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high efficiency power management applications.


Applications

- Load Switch

Features

- Low Gate Threshold Voltage
- Fast Switching Speed

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 
- Terminals Connections: See Diagram Below
- Weight: 0.008 grams (Approximate)

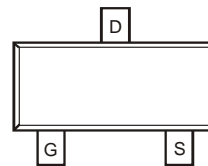


ESD Protected Gate

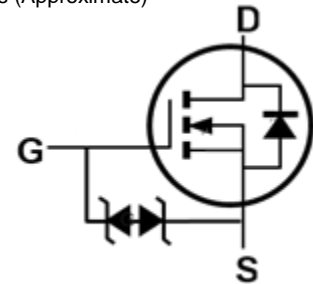
SOT23



Top View



Top View
Pin-Out



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate-Source Voltage	V _{GSS}	±12	V
Continuous Drain Current (Note 6) V _{GS} = 4.5V	I _D	3.6	A
Steady State T _A = +25°C T _A = +85°C		2.9	
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)	I _{DM}	21	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P _D	0.81	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	154	°C/W
Total Power Dissipation (Note 6)	P _D	1.33	W
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	94	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1.0	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.5	—	1.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	29	67	mΩ	V _{GS} = 4.5V, I _D = 2.5A
			31	70		V _{GS} = 4.0V, I _D = 2.5A
			43	98		V _{GS} = 2.5V, I _D = 2.5A
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 0.6A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	353	—	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	60	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	42	—	pF	
Gate Resistance	R _g	—	4.7	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	4.1	—	nC	V _{GS} = 4.5V, V _{DS} = 15V, I _D = 2.5A
Gate-Source Charge	Q _{gs}	—	0.6	—	nC	
Gate-Drain Charge	Q _{gd}	—	1.2	—	nC	
Turn-On Delay Time	t _{d(ON)}	—	5.7	—	ns	V _{DD} = 15V, I _D = 1.25A, V _{GEN} = 4.5V, R _{GEN} = 10Ω
Turn-On Rise Time	t _r	—	19	—	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	22	—	ns	
Turn-Off Fall Time	t _f	—	11	—	ns	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing

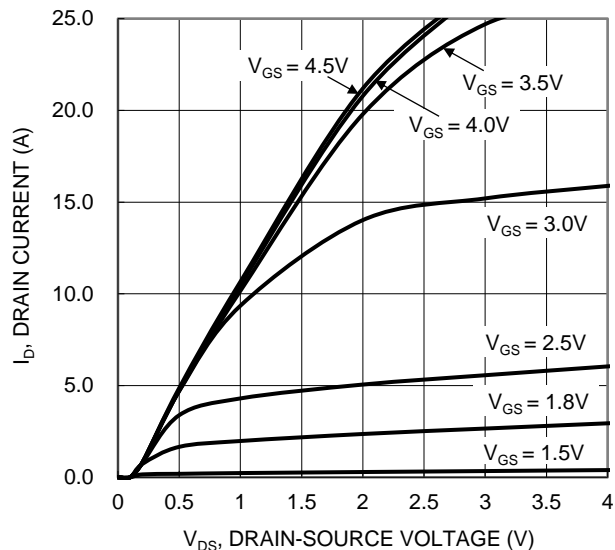


Figure 1. Typical Output Characteristic

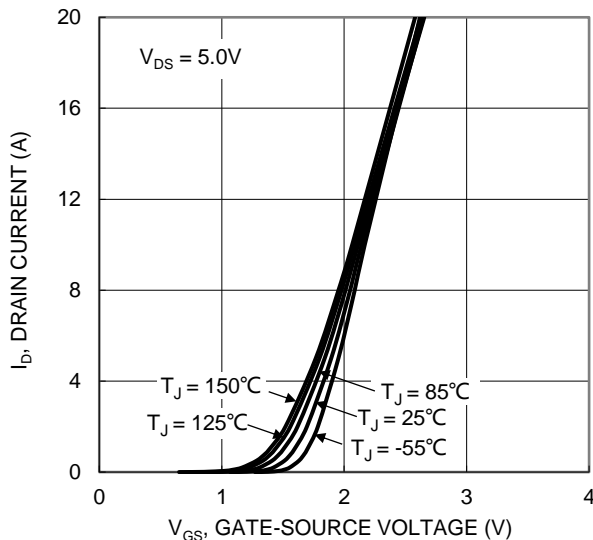


Figure 2. Typical Transfer Characteristic

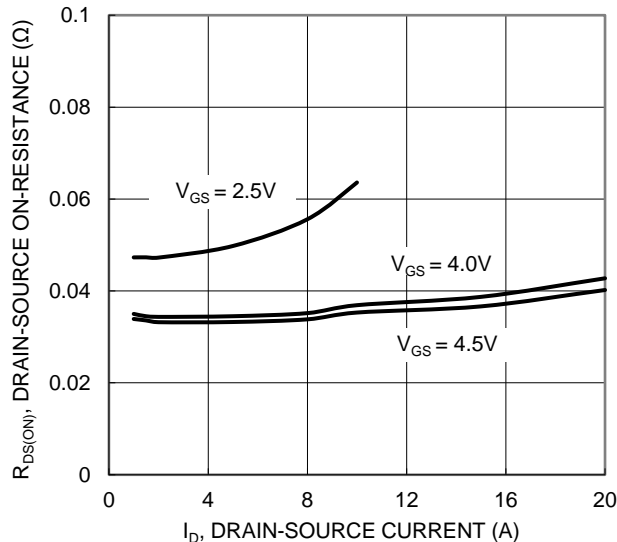


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

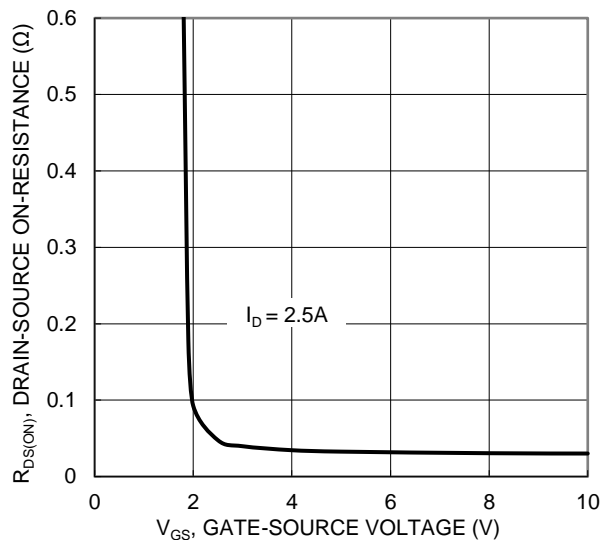


Figure 4. Typical Transfer Characteristic

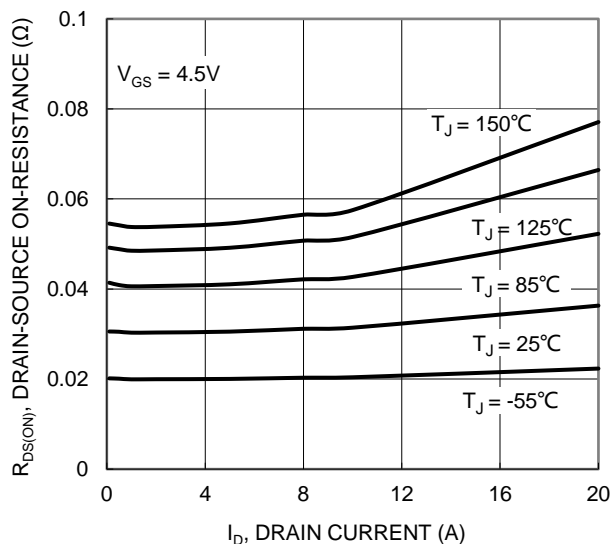


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

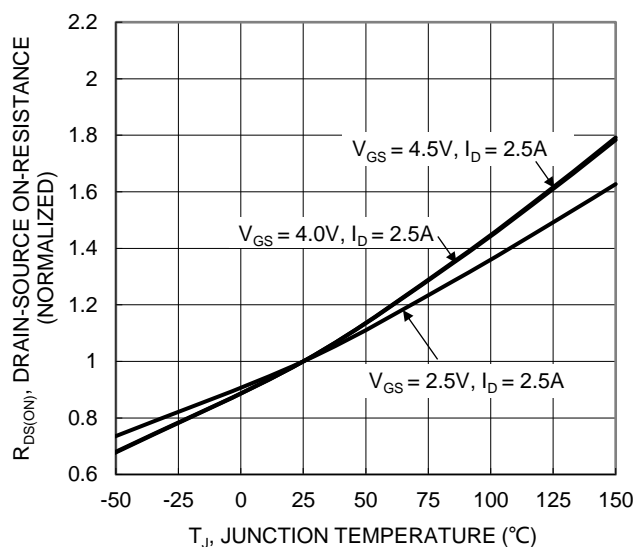


Figure 6. On-Resistance Variation with Temperature

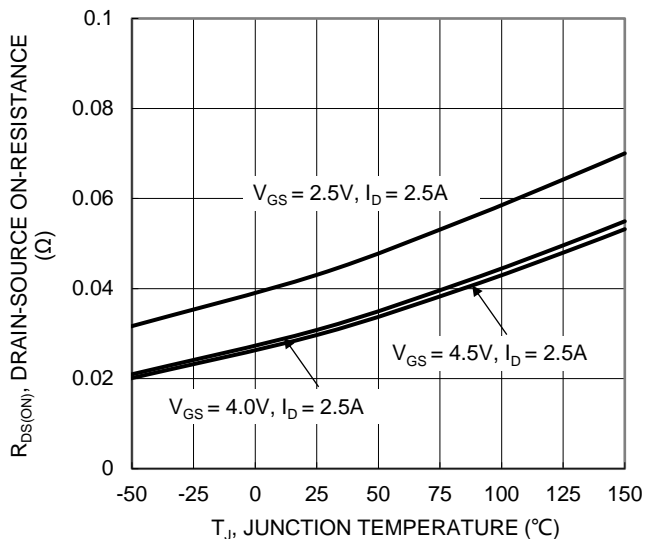


Figure 7. On-Resistance Variation with Temperature

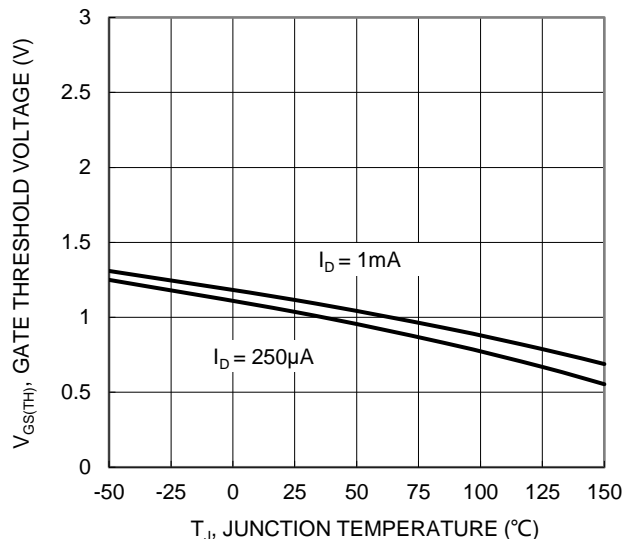


Figure 8. Gate Threshold Variation vs. Temperature

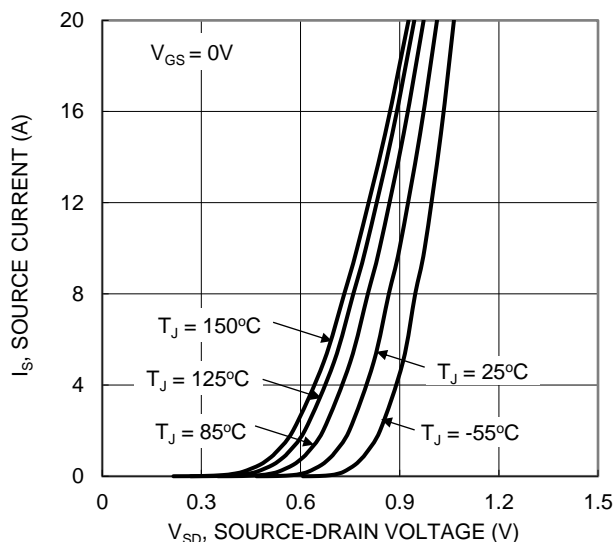


Figure 9. Diode Forward Voltage vs. Current

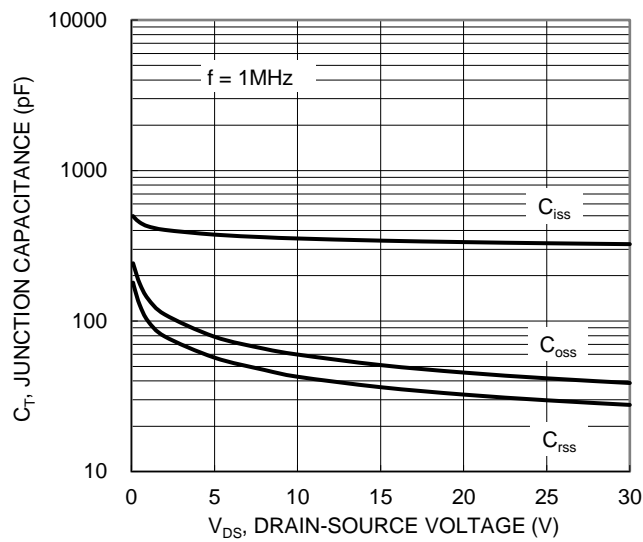


Figure 10. Typical Junction Capacitance

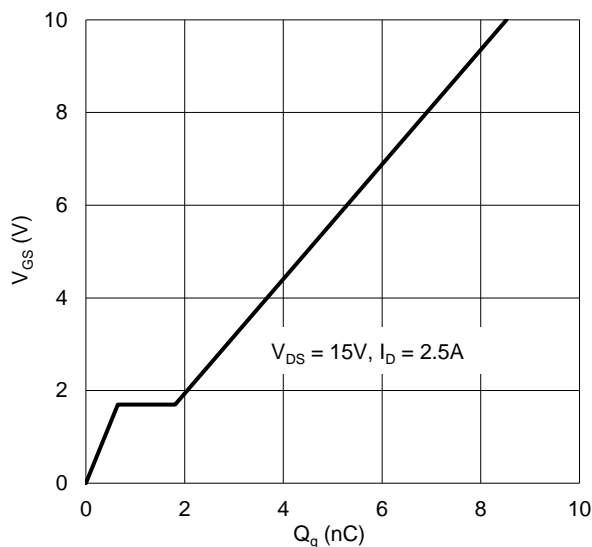


Figure 11. Gate Charge

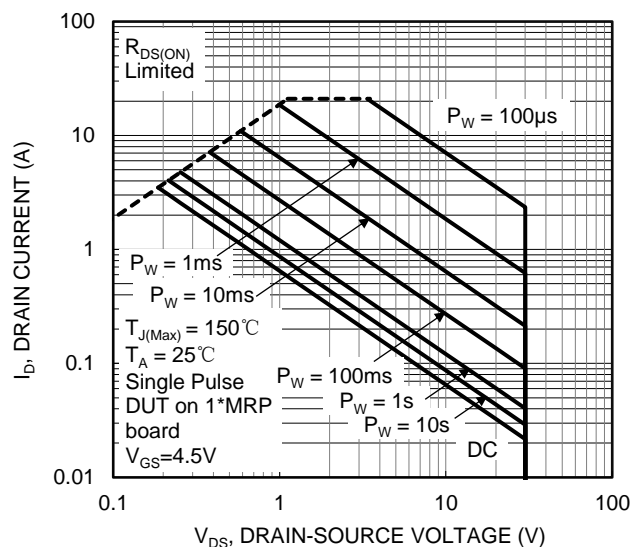


Figure 12. SOA, Safe Operation Area

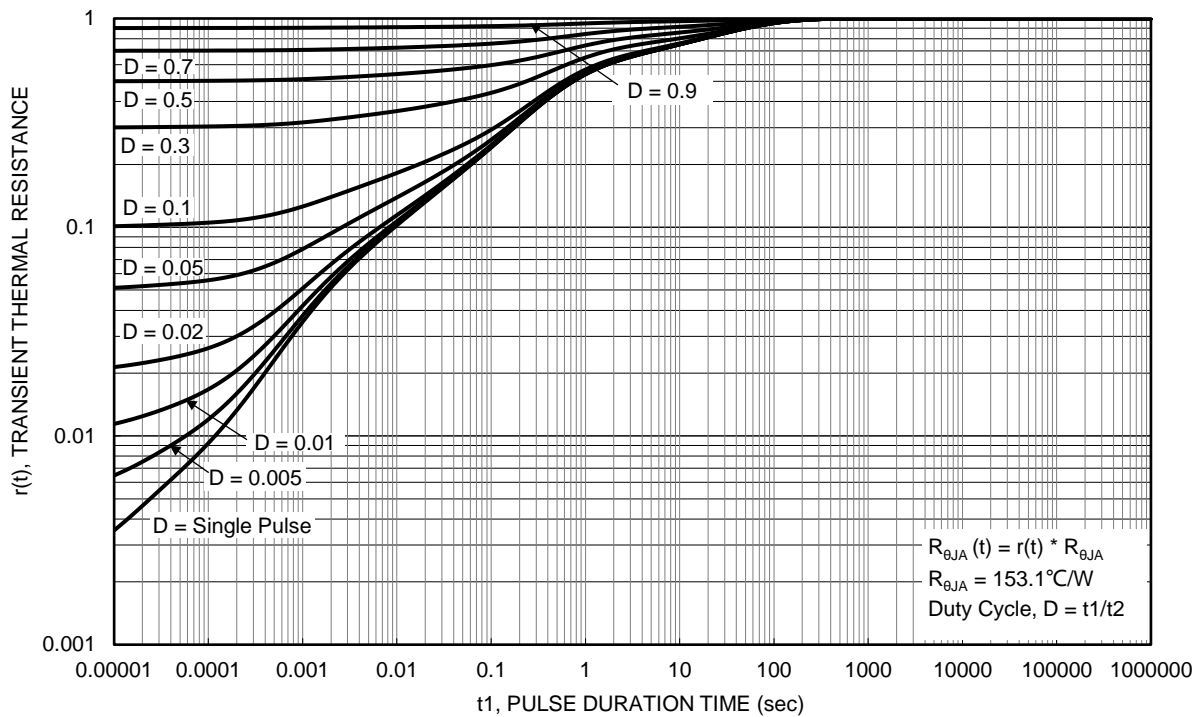
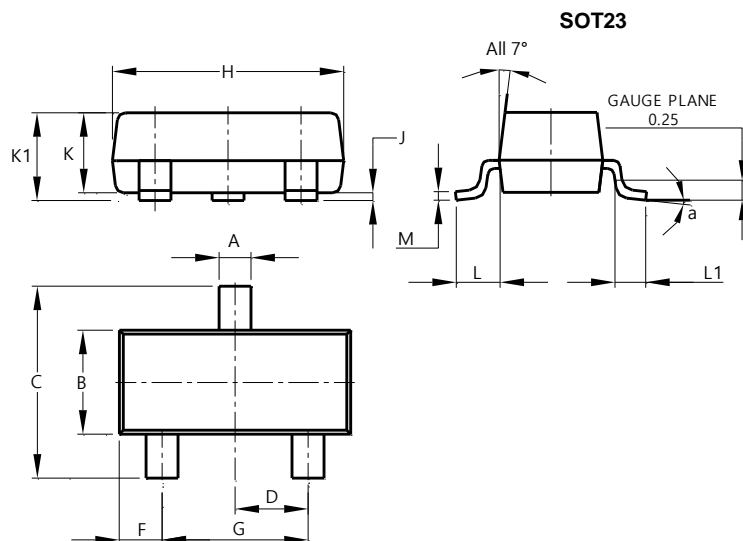


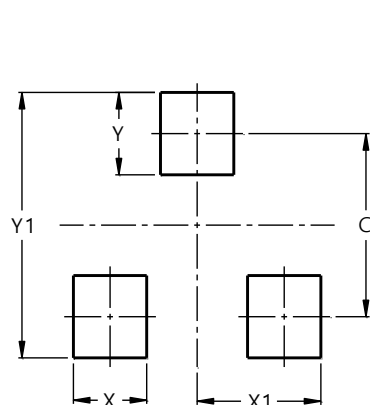
Figure 13. Transient Thermal Resistance

Package Outline Dimensions



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9