优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV$_{DSS}$	**R$_{DS(ON)}$**	**I$_D$** **T$_A$ = +25°C**
50V	2.0Ω @ V$_{GS}$ = 10V	360mA
	3.0Ω @ V$_{GS}$ = 5V	250mA

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance (R$_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- DC-DC converters
- Power-management functions
- Battery operated systems and solid-state relays
- Drivers: relays, solenoids, lamps, hammers, displays, memories, transistors, etc.

Features and Benefits

- N-Channel MOSFET
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate

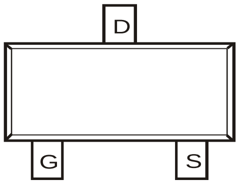
Mechanical Data

- Package: SOT323
- Package Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)

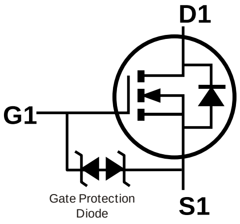
ESD PROTECTED

SOT323 (Standard)

Top View



Top View
Pin Configuration



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	50	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	360 250	mA
Continuous Drain Current (Note 6) V_{GS} = 5V	Steady State	T_A = +25°C T_A = +70°C	I_D	250 200	mA
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	700	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation	(Note 5)	P_D	320	mW
	(Note 6)		420	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	395	°C/W
	(Note 6)		301	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	50	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	µA	V_{DS} = 50V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.8	—	1.5	V	V_{DS} = V_{GS}, I_D = 100µA
Gate Threshold Voltage Temperature Coefficient (Note 8)	$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	—	-3.4	—	mV/°C	—
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.73	2.0	Ω	V_{GS} = 10V, I_D = 270mA
		—	0.77	3.0		V_{GS} = 5V, I_D = 200mA
Forward Transconductance	g_{FS}	80	—	—	mS	V_{DS} = 10V, I_D = 200mA
Diode Forward Voltage	V_{SD}	—	0.75	1.2	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	45.8	—	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	5.3	—		
Reverse Transfer Capacitance	C_{rss}	—	3.9	—		
Total Gate Charge V_{GS} = 10V	Q_g	—	1.2	—	nC	V_{GS} = 10V, V_{DS} = 10V, I_D = 250mA
Total Gate Charge V_{GS} = 4.5V	Q_g	—	0.6	—		
Gate-Source Charge	Q_{gs}	—	0.2	—		
Gate-Drain Charge	Q_{gd}	—	0.1	—		
Turn-On Delay Time	$t_{D(ON)}$	—	2.7	—	ns	V_{DD} = 30V, V_{GS} = 10V, R_G = 25Ω, I_D = 200mA
Turn-On Rise Time	t_R	—	2.5	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	18.9	—		
Turn-Off Fall Time	t_F	—	11.0	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

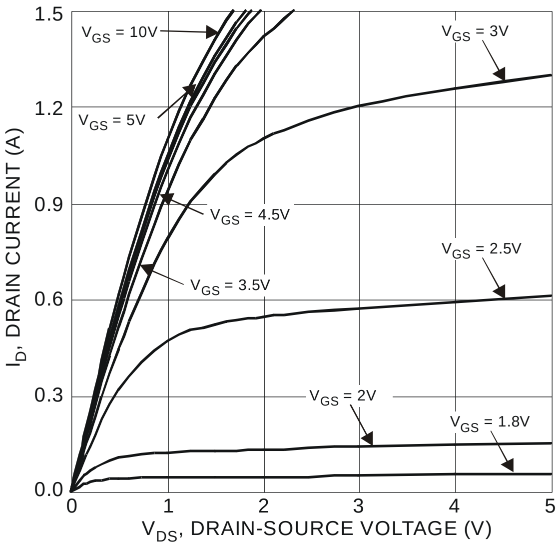


Figure 1 Typical Output Characteristics

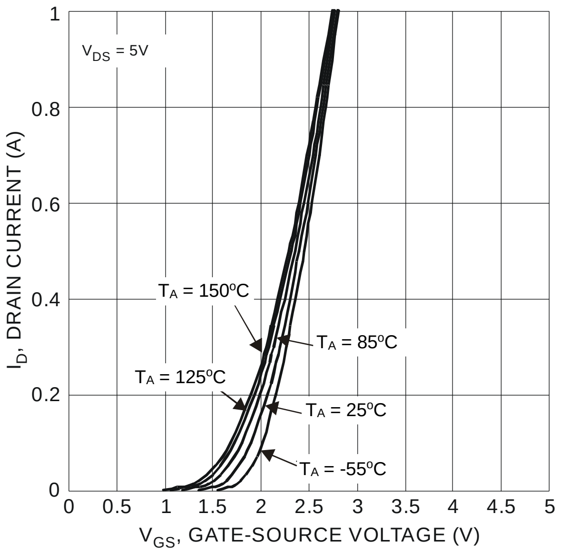


Figure 2 Typical Transfer Characteristics

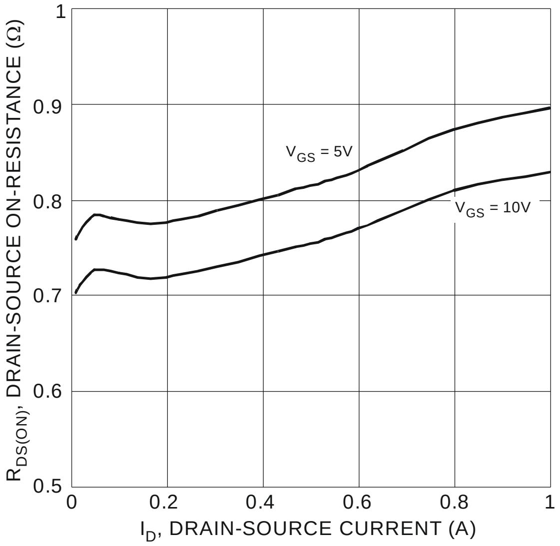


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

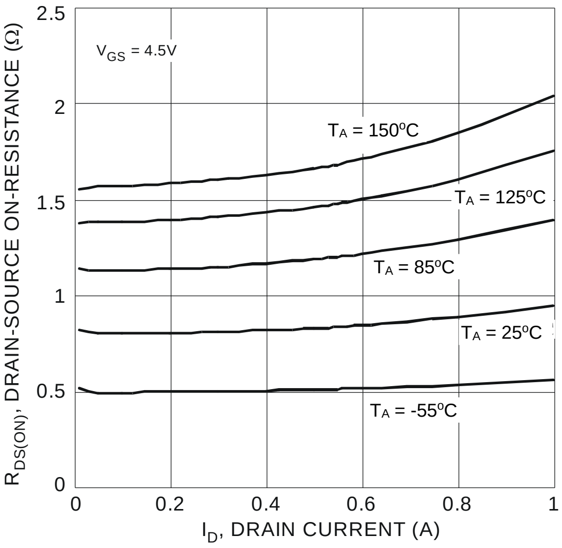


Figure 4 Typical On-Resistance vs.
Drain Current and Temperature

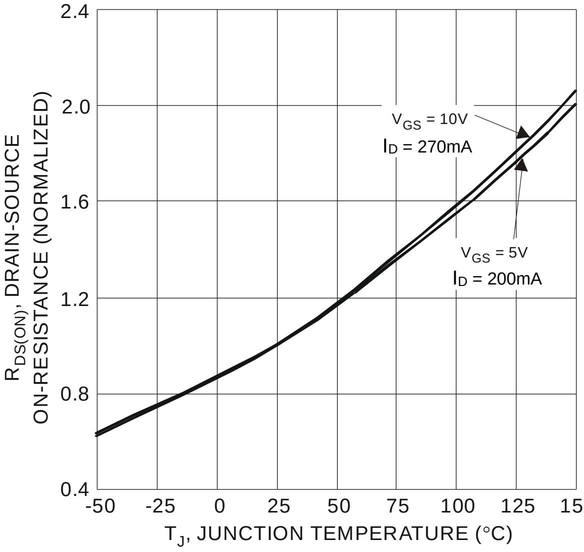


Figure 5 On-Resistance Variation with Temperature

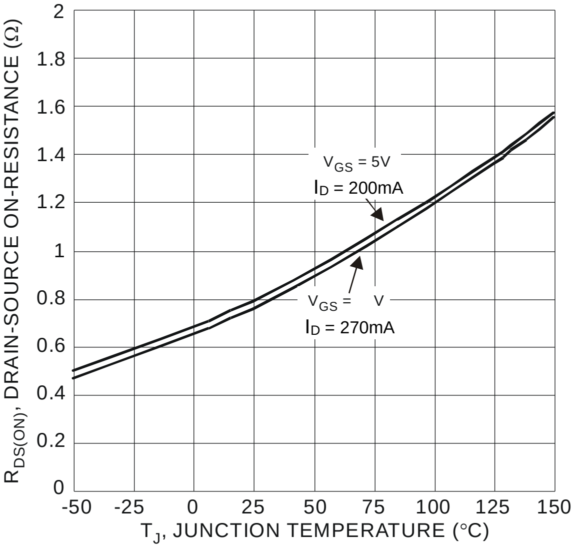


Figure 6 On-Resistance Variation with Temperature

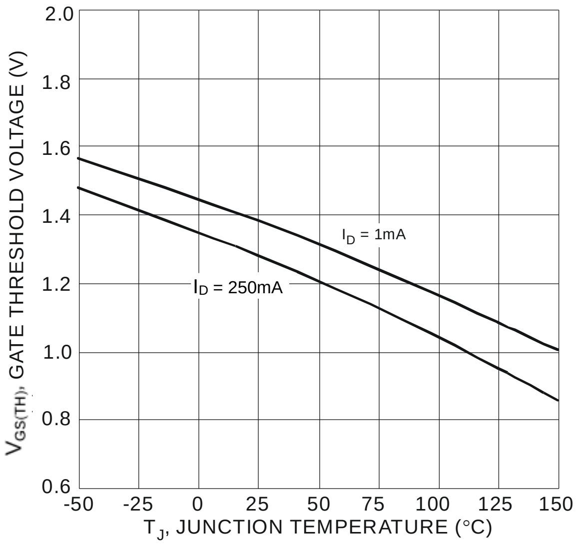


Figure 7 Gate Threshold Variation vs. Junction Temperature

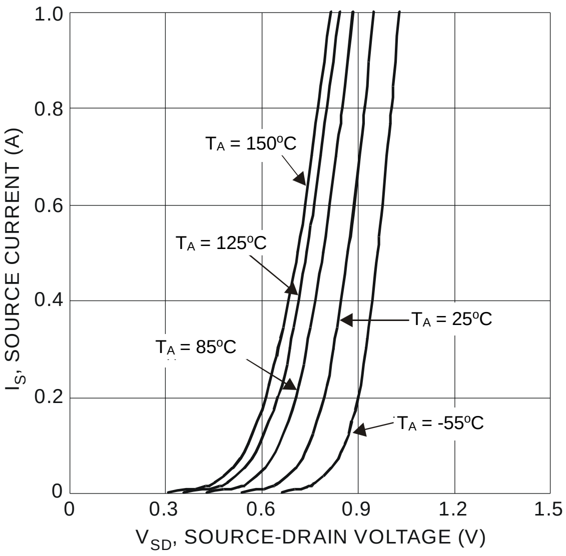


Figure 8 Diode Forward Voltage vs. Current

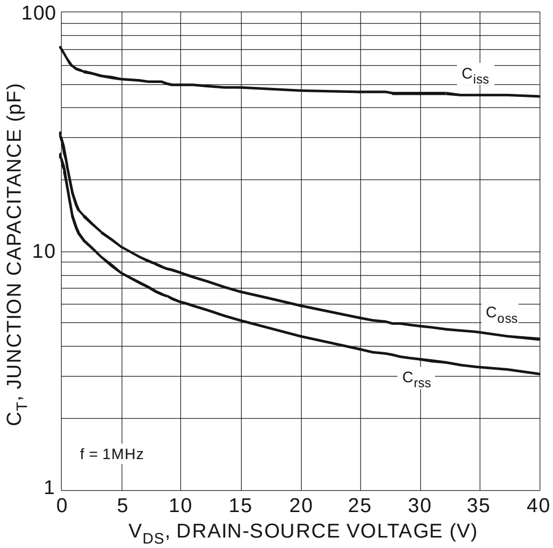


Figure 9 Typical Junction Capacitance

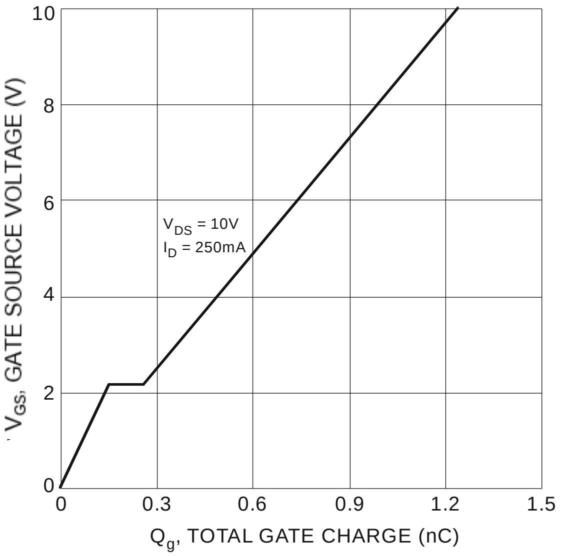


Figure 10 Gate Charge

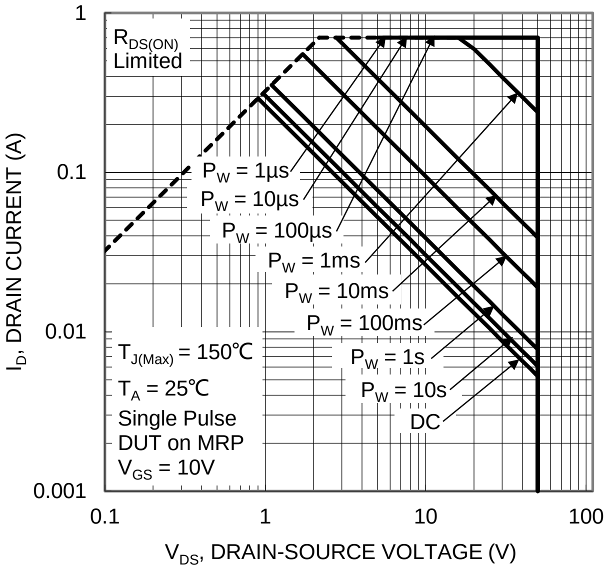
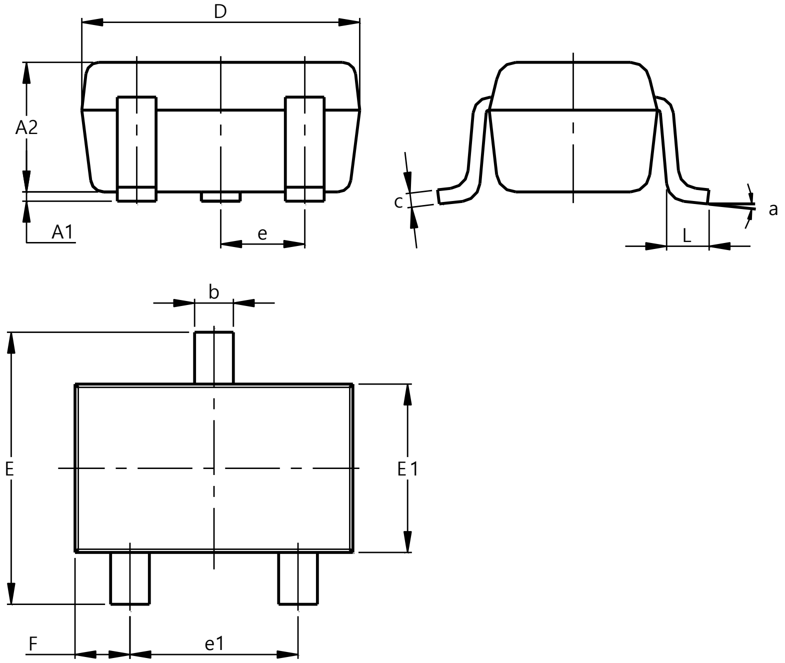


Figure 11 SOA, Safe Operation Area

Package Outline Dimensions

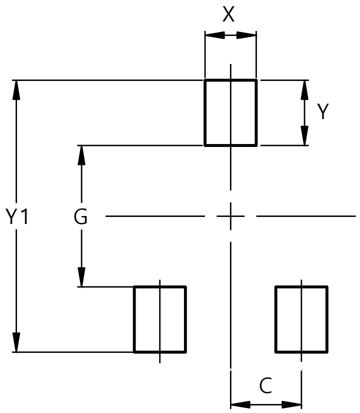
SOT323 (Standard)



SOT323 (Standard)			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.80	1.00	0.90
b	0.20	0.40	0.30
c	0.08	0.18	0.13
D	1.80	2.20	2.00
E	2.00	2.45	2.225
E1	1.15	1.35	1.25
e	--	--	0.65
e1	1.20	1.40	1.30
F	0.25	0.475	0.3625
L	0.25	0.46	0.355
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT323 (Standard)



Dimensions	**Value (in mm)**
C	0.650
G	1.300
X	0.470
Y	0.600
Y1	2.500