优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_A = +25°C
-20V	28mΩ @ V_{GS} = -4.5V	-6.1A
	43mΩ @ V_{GS} = -2.5V	-4.9A

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

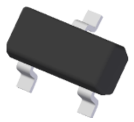
- Load Switch

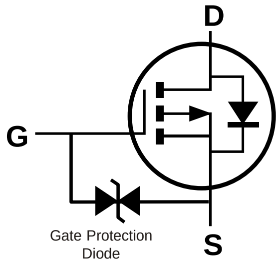
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ⓔ3
- Terminal Connections: See Diagram Below
- Weight: 0.009 grams (Approximate)

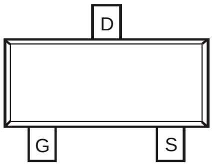

ESD PROTECTED

SOT23


Top View



Internal Schematic



Top View

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±10	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	T_C = +25°C T_C = +70°C	I_D	-6.1 -4.8	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	-38	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	-2.2	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.8	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	158	°C/W
Total Power Dissipation (Note 6)		P_D	1.6	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	81	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	14.3	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.5	—	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	20.3	28	mΩ	V_{GS} = -4.5V, I_D = -2A
		—	26.5	43		V_{GS} = -2.5V, I_D = -2A
Diode Forward Voltage	V_{SD}	—	-0.66	-1.1	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	803	—	pF	V_{DS} = -10V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	114	—		
Reverse Transfer Capacitance	C_{rss}	—	51	—		
Gate Resistance	R_G	—	65.5	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -8V)	Q_g	—	14.5	—	nC	V_{DD} = -10V, I_D = -20A
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	8.4	—		
Gate-Source Charge	Q_{gs}	—	1.5	—		
Gate-Drain Charge	Q_{gd}	—	1.9	—		
Turn-On Delay Time	$t_{D(ON)}$	—	12	—	ns	V_{GS} = -4.5V, V_{DD} = -10V, R_G = 1Ω, I_D = -10A
Turn-On Rise Time	t_R	—	6	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	81	—		
Turn-Off Fall Time	t_F	—	46	—		

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

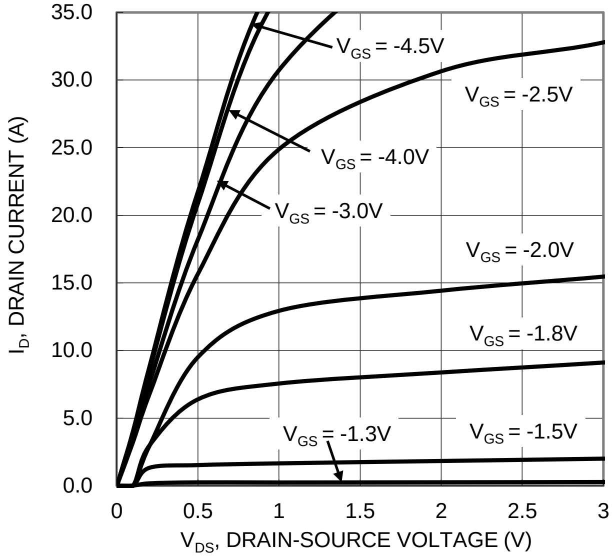


Figure 1. Typical Output Characteristic

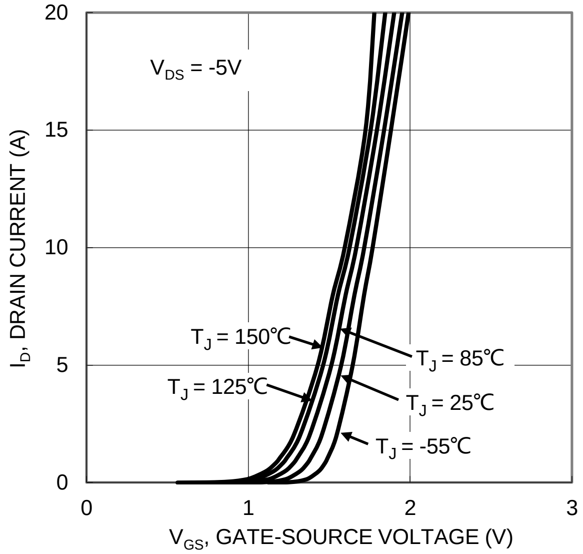


Figure 2. Typical Transfer Characteristic

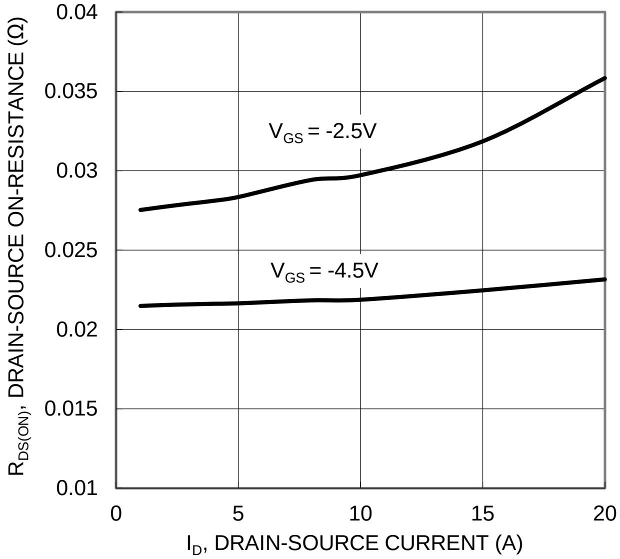


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

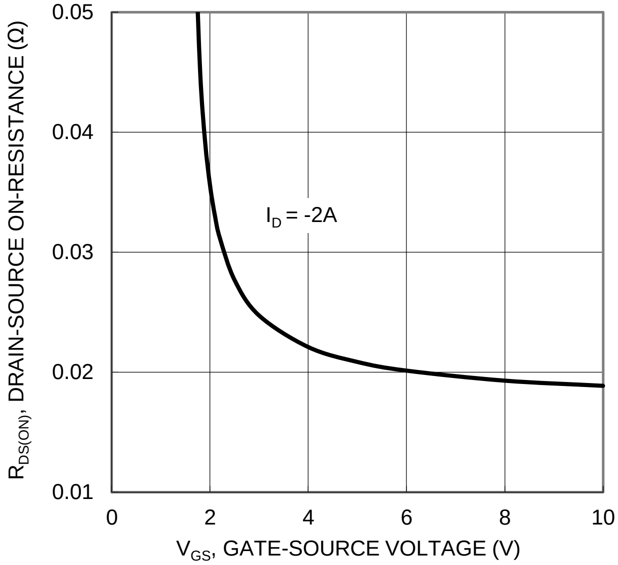


Figure 4. Typical Transfer Characteristic

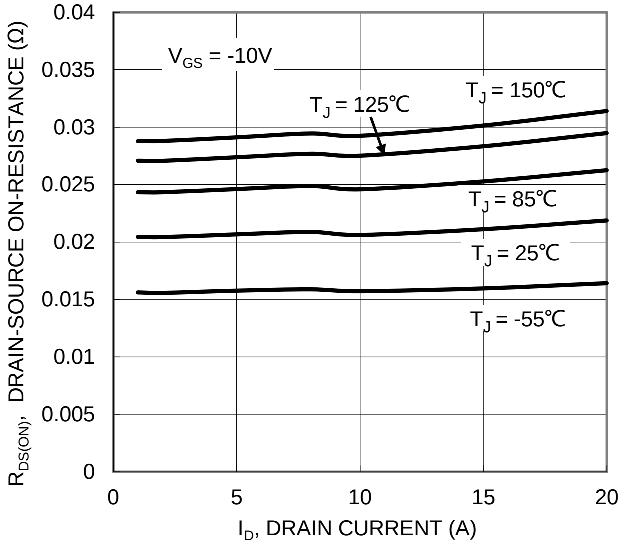


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

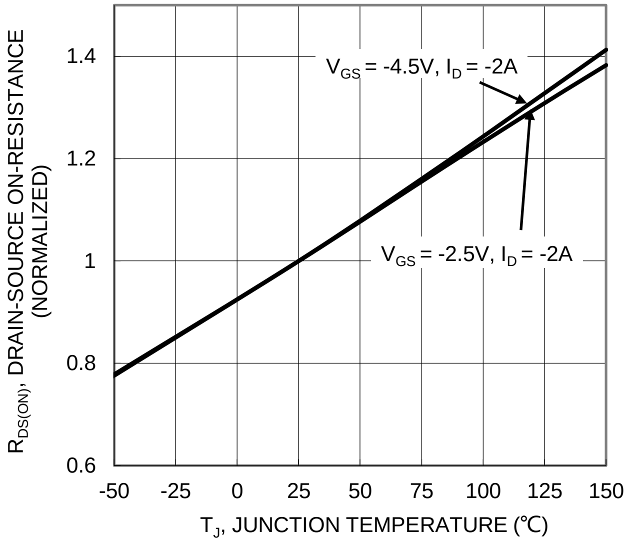


Figure 6. On-Resistance Variation with Temperature

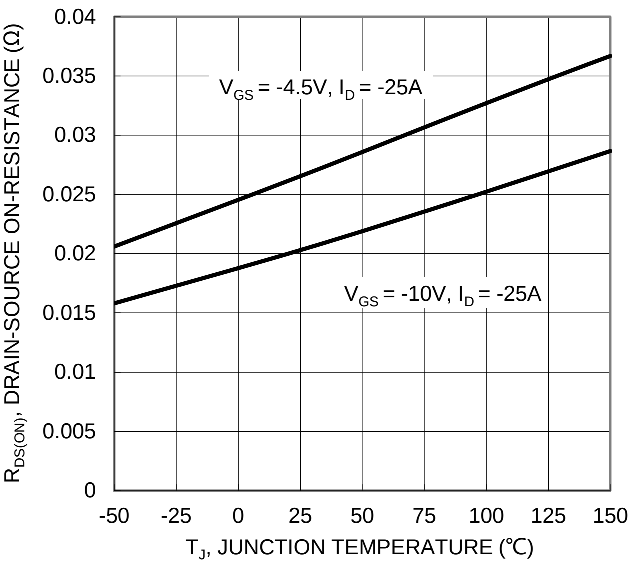


Figure 7. On-Resistance Variation with Temperature

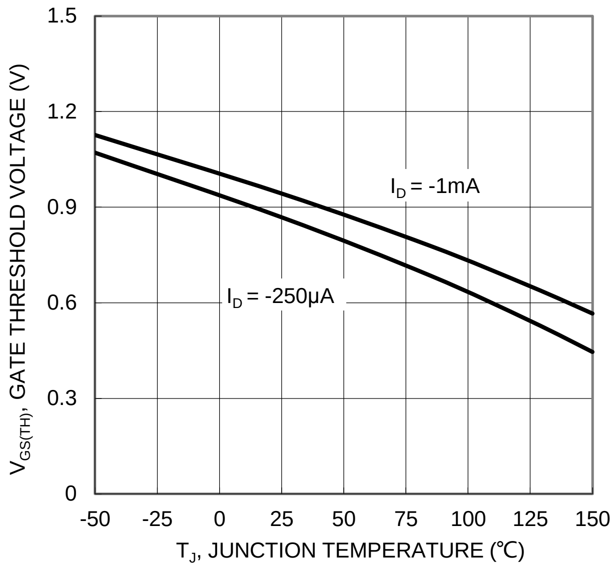


Figure 8. Gate Threshold Variation vs. Junction Temperature

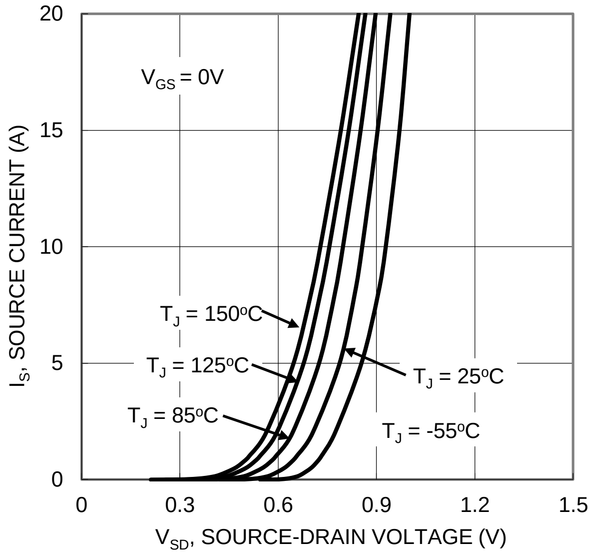


Figure 9. Diode Forward Voltage vs. Current

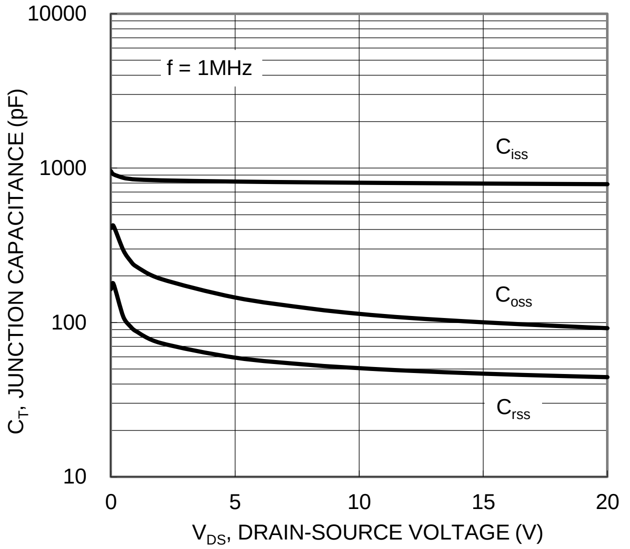


Figure 10. Typical Junction Capacitance

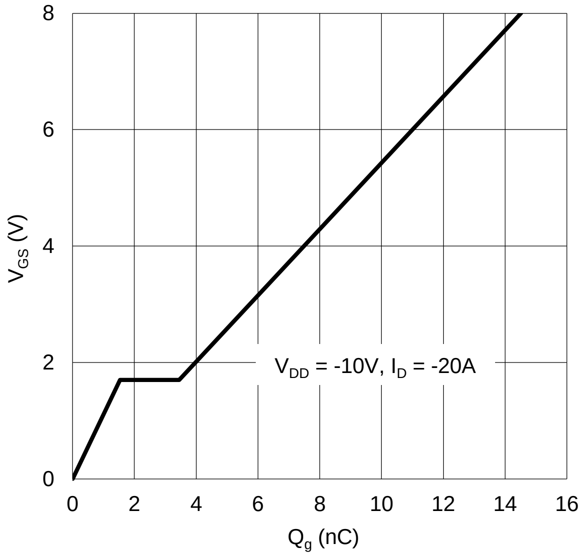


Figure 11. Gate Charge

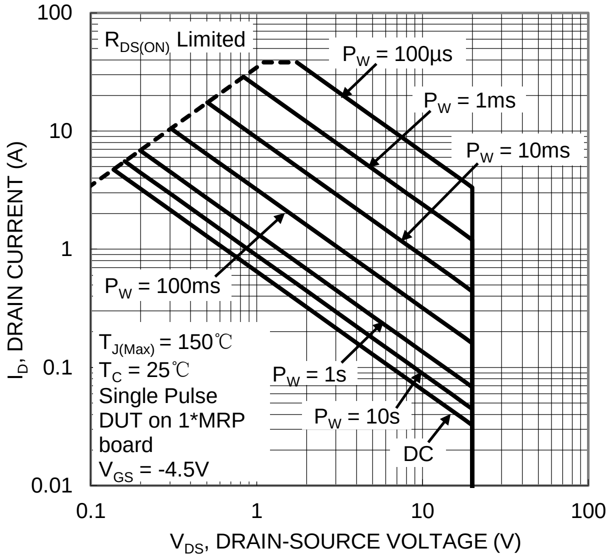


Figure 12. SOA, Safe Operation Area

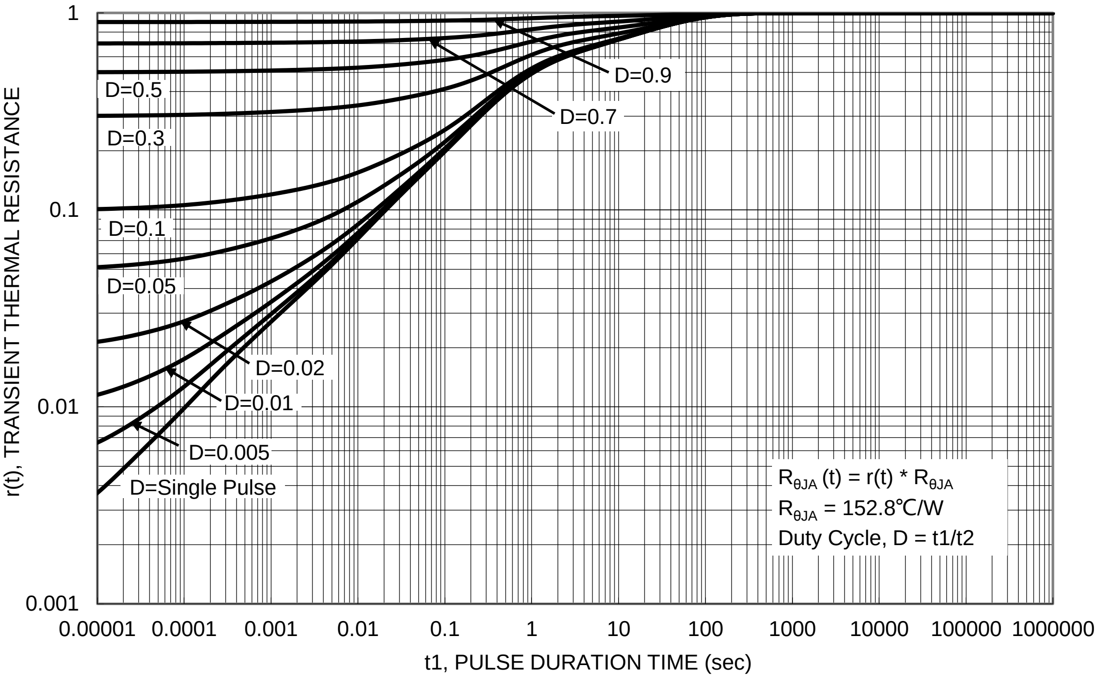
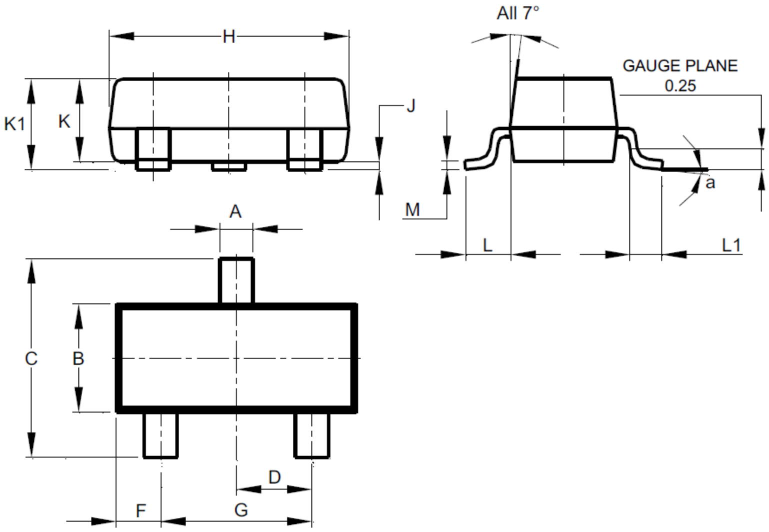


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

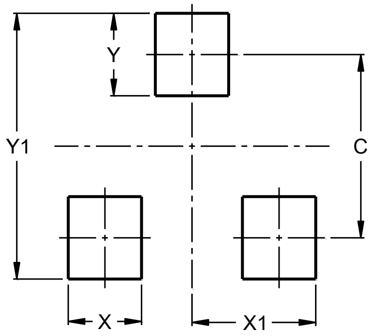
SOT23



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9