优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
-20V	45mΩ @ V_{GS} = -4.5V	-4.5A
	65mΩ @ V_{GS} = -2.5V	-3.8A

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

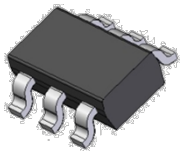
Applications

- General Purpose Interfacing Switch
- Power Management Functions

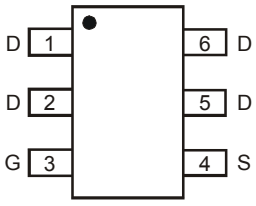
Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.015 grams (Approximate)

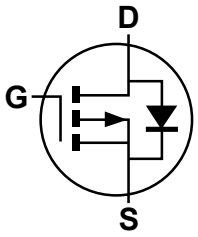
TSOT26



Top View



Top View
Pin-Out



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Note 5) Continuous	T_A = +25°C T_A = +70°C	I_D	-4.5 -3.7	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)		I_{DM}	-20	A
Body-Diode Continuous Current (Note 5)		I_S	-2.0	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	100	°C/W
	t<10s		74	
Total Power Dissipation (Note 6)		P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	70	°C/W
	t<10s		46	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC PARAMETERS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	I_D = -250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current @ T_J = +55°C (Note 8)	I_{DSS}	—	—	-1 -10	μA	V_{DS} = -16V, V_{GS} = 0V V_{DS} = -16V, V_{GS} = 0V
Zero Gate Voltage Drain Current @T_J = +150°C (Note 8)	I_{DSS}	—	—	-100	μA	V_{DS} = -16V, V_{GS} = 0V
Gate-Body Leakage Current	I_{GSS}	—	—	±100	nA	V_{DS} = 0V, V_{GS} = ±8V
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	—	-1.5	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	25 33	45 65	mΩ	V_{GS} = -4.5V, I_D = -4.5A V_{GS} = -2.5V, I_D = -3.8A
Static Drain-Source On-Resistance @ T_J = +125°C (Note 8)	$R_{DS\ ON)}$	—	—	72	mΩ	V_{GS} = -4.5V, I_D = -4.5A
Diode Forward Voltage	V_{SD}	-0.5	-0.72	-1.4	V	I_S = -2.1A, V_{GS} = 0V
On State Drain Current (Note 8)	$I_{D(ON)}$	10	—	—	A	V_{DS} ≦5V, V_{GS} = 4.5V
DYNAMIC PARAMETERS (Note 8)						
Input Capacitance	C_{iss}	—	1,496	2,990	pF	V_{DS} = -15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	130	260	pF	
Reverse Transfer Capacitance	C_{rss}	—	116	230	pF	
Total Gate Charge	Q_G	—	14.4	25	nC	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -4.5A
Gate-Source Charge	Q_{GS}	—	2.6	5		
Gate-Drain Charge	Q_{GD}	—	2.7	5.5		
Turn-On Delay Time	$t_{D(ON)}$	—	8.5	30	ns	V_{DS} = -5V, V_{GS} = -4.5V, I_D = -1A, R_G = 6.0Ω
Rise Time	t_R	—	11	60		
Turn-Off Delay Time	$t_{D(OFF)}$	—	61	130		
Fall Time	t_F	—	25	100		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

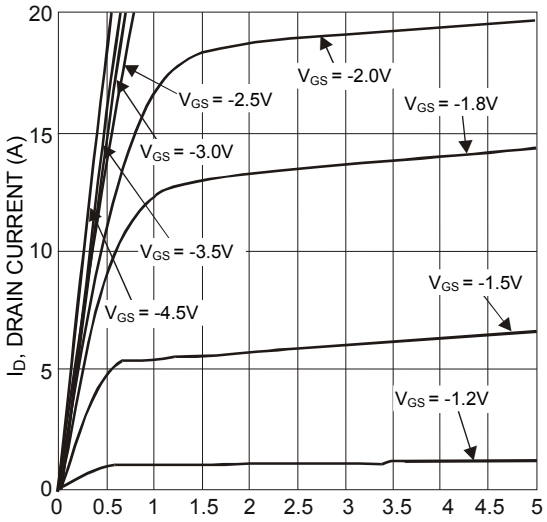


Figure 1 Typical Output Characteristics

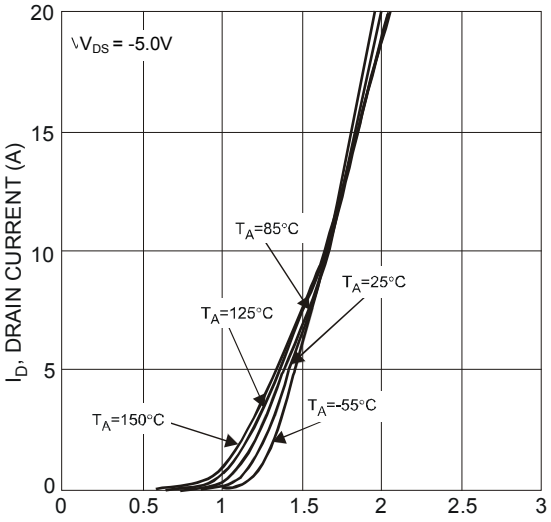


Figure 2 Typical Transfer Characteristics

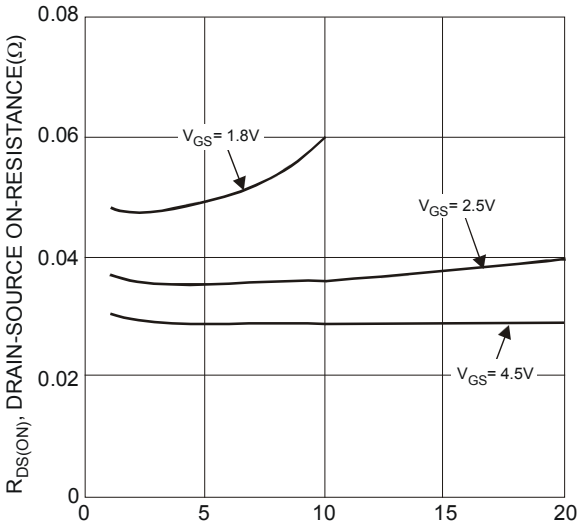


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

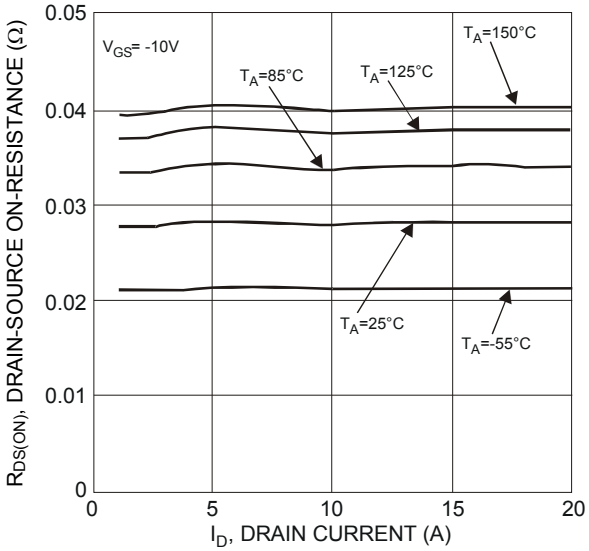


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

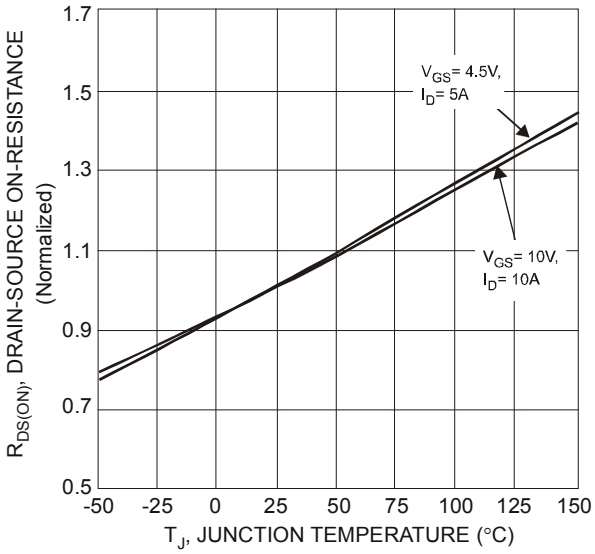


Figure 5 On-Resistance Variation with Temperature

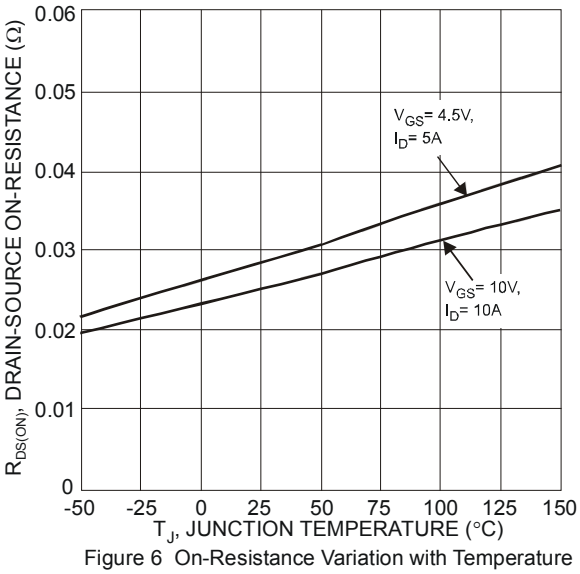


Figure 6 On-Resistance Variation with Temperature

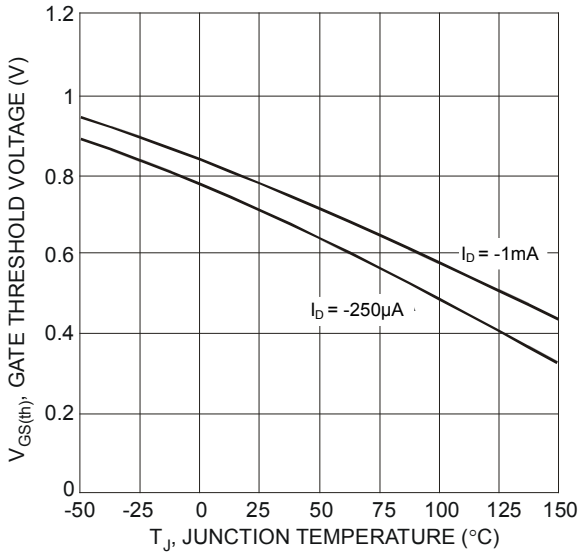


Figure 7 Gate Threshold Variation vs. Junction Temperature

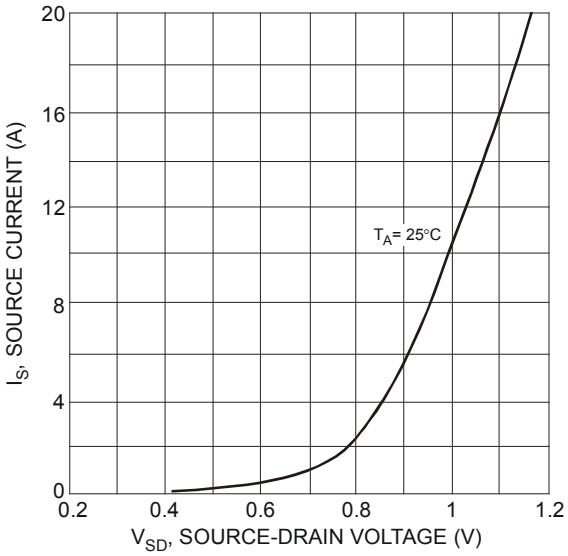


Figure 8 Diode Forward Voltage vs. Current

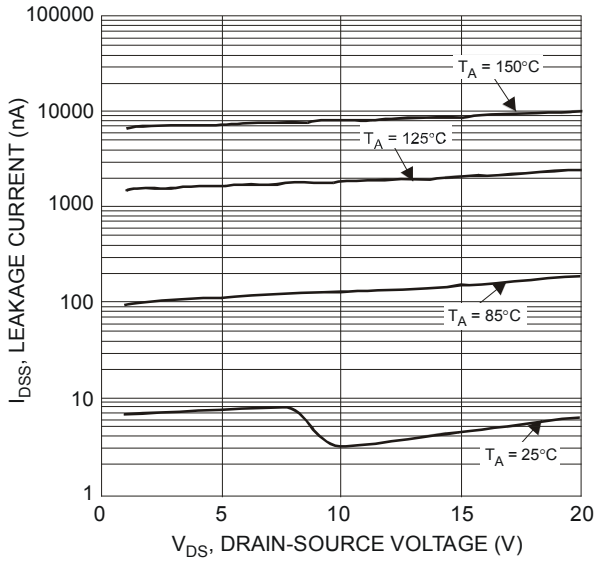


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

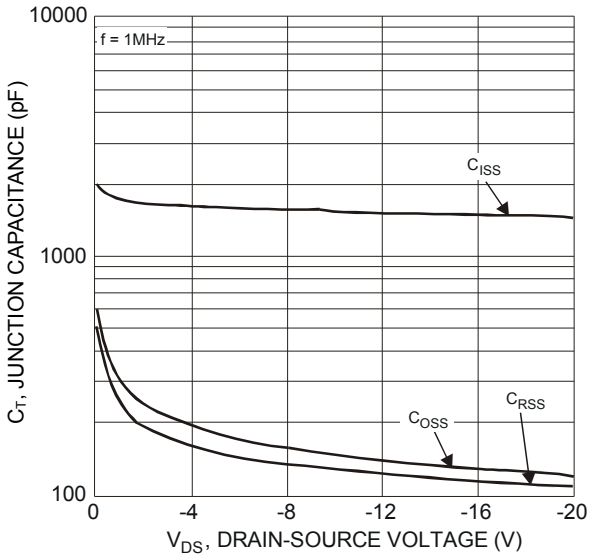


Figure 10 Typical Junction Capacitance

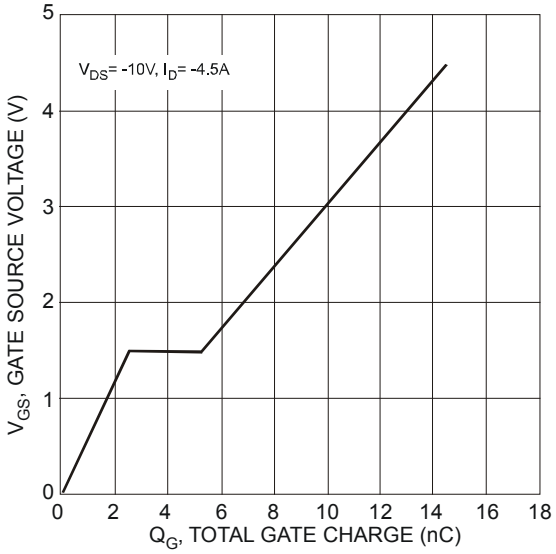
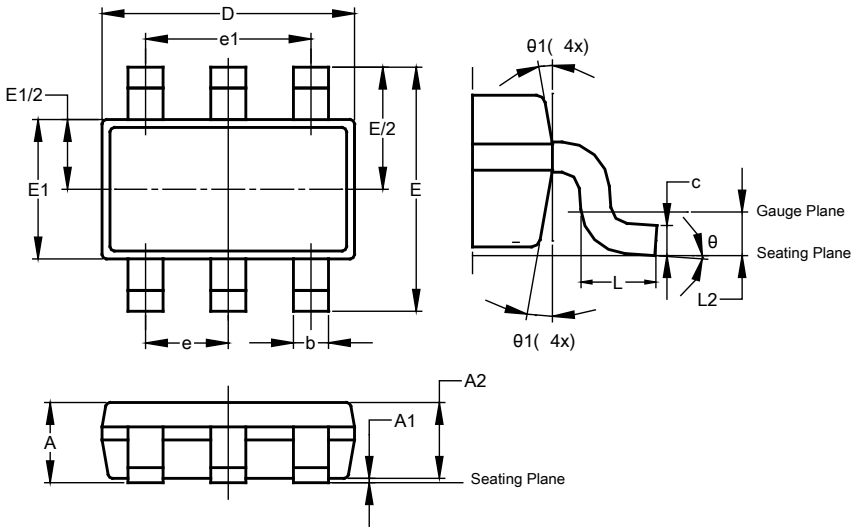


Figure 11 Gate Charge Characteristics

Package Outline Dimensions

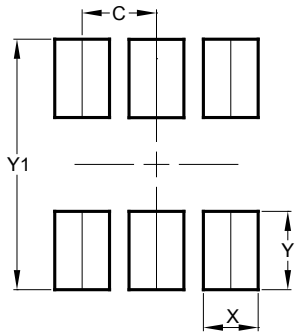
TSOT26



TSOT26			
Dim	**Min**	**Max**	**Typ**
A	–	1.00	–
A1	0.010	0.100	–
A2	0.840	0.900	–
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	–
c	0.120	0.200	–
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	–
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199