



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

Description

This MOSFET is designed to minimize on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

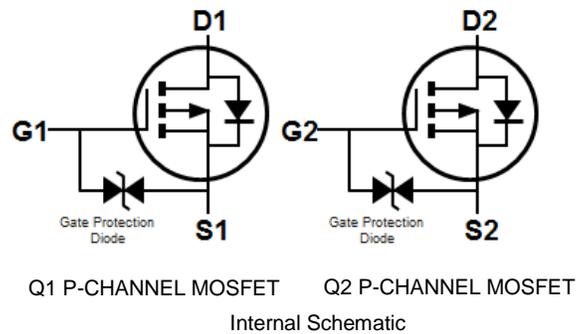
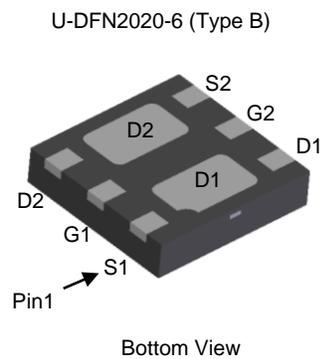
- Load Switch
- Power Management Functions
- Portable Power Adaptors

Features

- Low On-Resistance
- Low Input Capacitance
- Low Profile, 0.6mm Max Height
- ESD Protected Gate

Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^(e4)
- Terminals Connections: See Diagram Below
- Weight: 0.0065 grams (Approximate)



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	-20	V		
Gate-Source Voltage	V _{GSS}	±8	V		
Continuous Drain Current (Note 5) V _{GS} = -4.5V	I _D	Steady State	T _A = +25°C	-3.8	A
			T _A = +70°C	-3.0	
Maximum Continuous Body Diode Forward Current (Note 5)	I _S	-1.0	A		
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)	I _{DM}	-25	A		
Avalanche Current (Note 7) L = 0.1mH	I _{AS}	-13	A		
Avalanche Energy (Note 7) L = 0.1mH	E _{AS}	8.5	mJ		

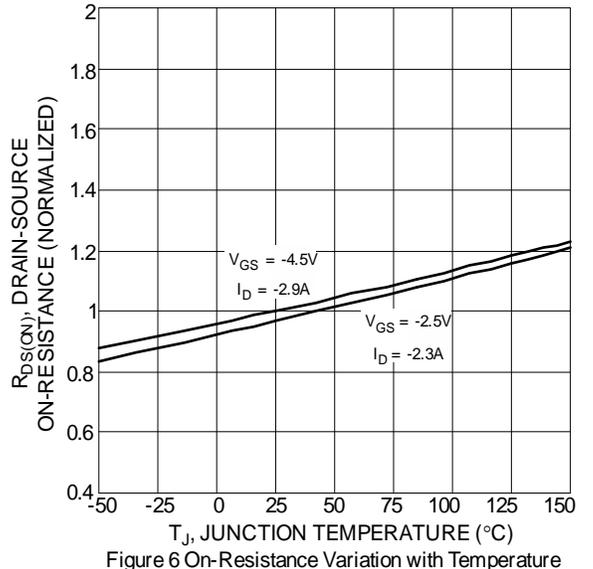
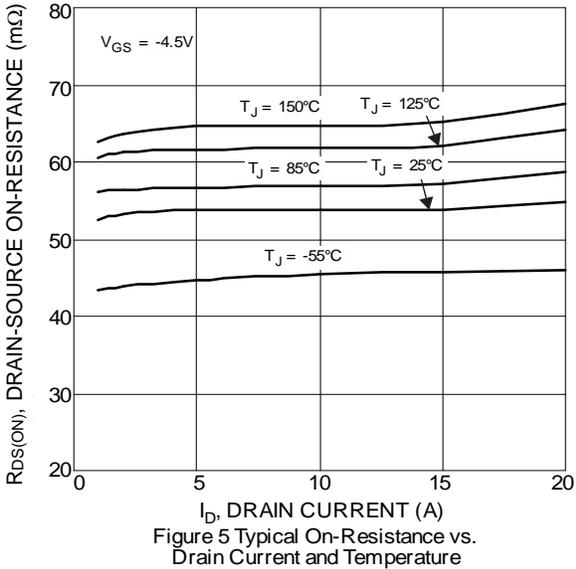
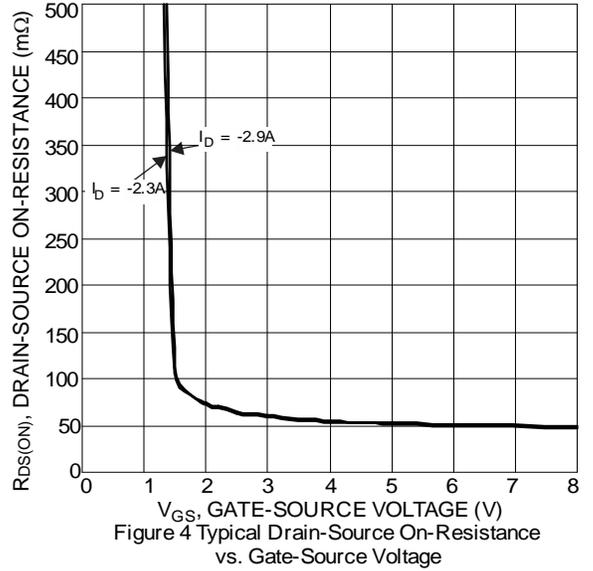
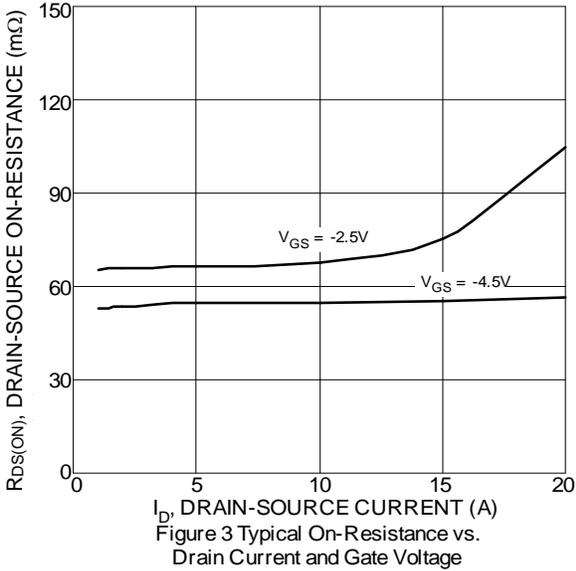
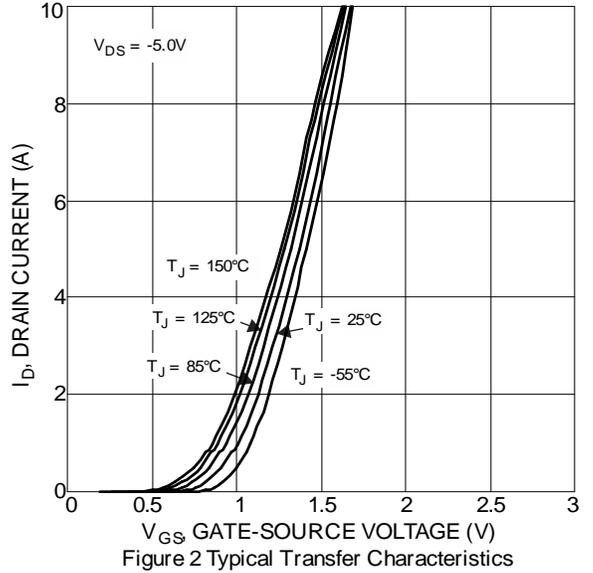
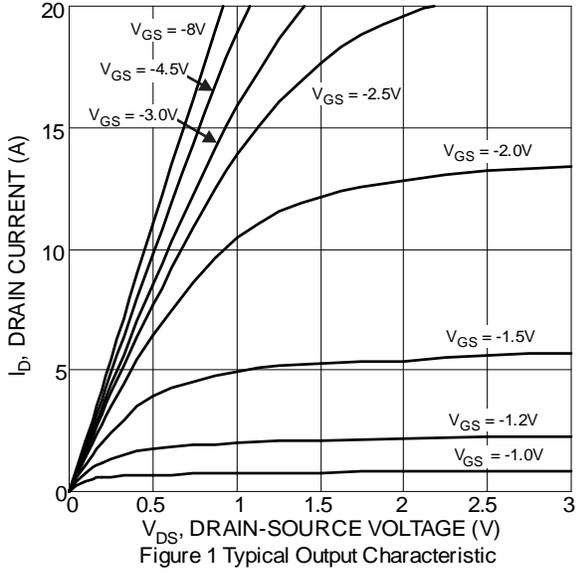
Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	P _D	T _A = +25°C	0.7	W
Thermal Resistance, Junction to Ambient (Note 5)		Steady State	R _{θJA}	178
Total Power Dissipation (Note 6)	P _D	T _A = +25°C	1.4	W
Thermal Resistance, Junction to Ambient (Note 6)		Steady State	R _{θJA}	92
Thermal Resistance, Junction to Case (Note 6)	R _{θJC}	22		
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C	

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1.0	μA	V _{DS} = -20V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±6.4V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	-0.35	—	-1.4	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	53	75	mΩ	V _{GS} = -4.5V, I _D = -2.9A
		—	64	137		V _{GS} = -2.5V, I _D = -2.3A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0V, I _S = -3.0A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	642	—	pF	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	98	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	87	—	pF	
Gate Resistance	R _g	—	26.5	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	8.8	—	nC	V _{DS} = -10V, I _D = -3.7A
Total Gate Charge (V _{GS} = -8V)		—	15	—	nC	
Gate-Source Charge	Q _{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q _{gd}	—	2.9	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	5.5	—	ns	V _{DD} = -10V, V _{GS} = -4.5V, R _L = 3.3Ω, R _g = 1Ω
Turn-On Rise Time	t _R	—	22.6	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	34.1	—	ns	
Turn-Off Fall Time	t _F	—	34.3	—	ns	
Body Diode Reverse Recovery Time	t _{RR}	—	13	—	ns	I _S = -3.0A, dI/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{RR}	—	3.3	—	nC	I _S = -3.0A, dI/dt = 100A/μs

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided
 - Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.



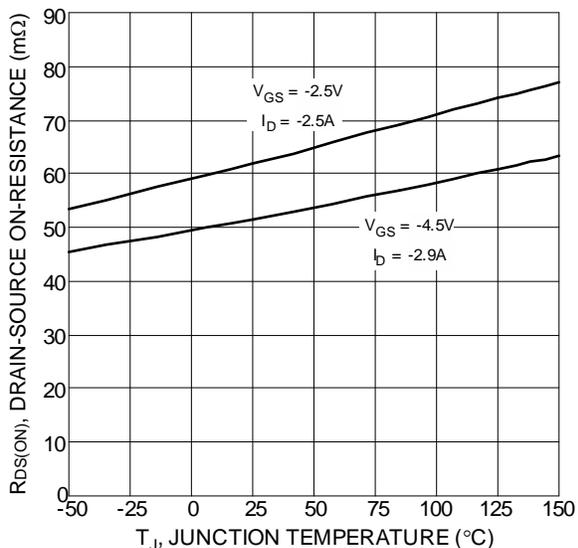


Figure 7 On-Resistance Variation with Temperature

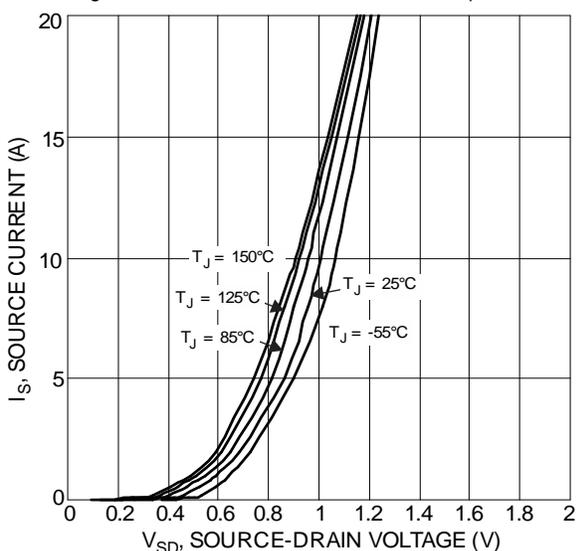


Figure 9 Diode Forward Voltage vs. Current

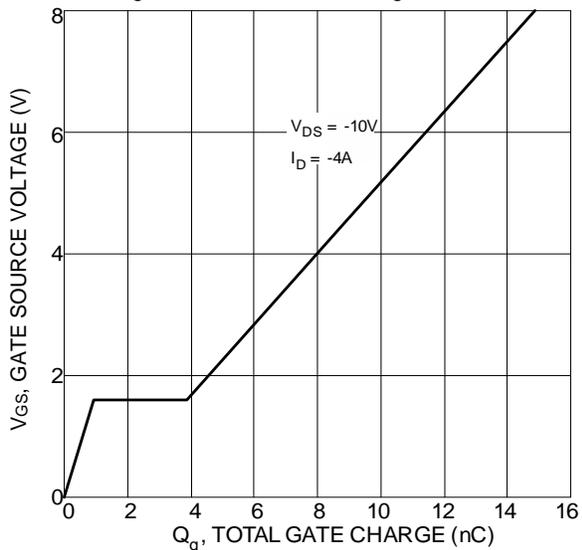


Figure 11 Gate Charge

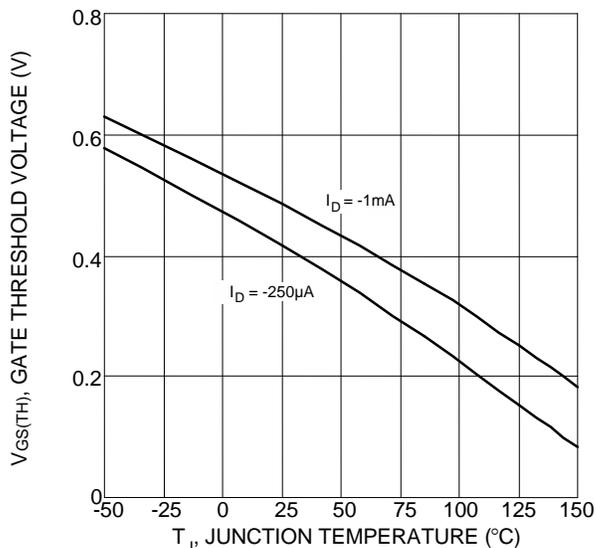


Figure 8 Gate Threshold Variation vs. Junction Temperature

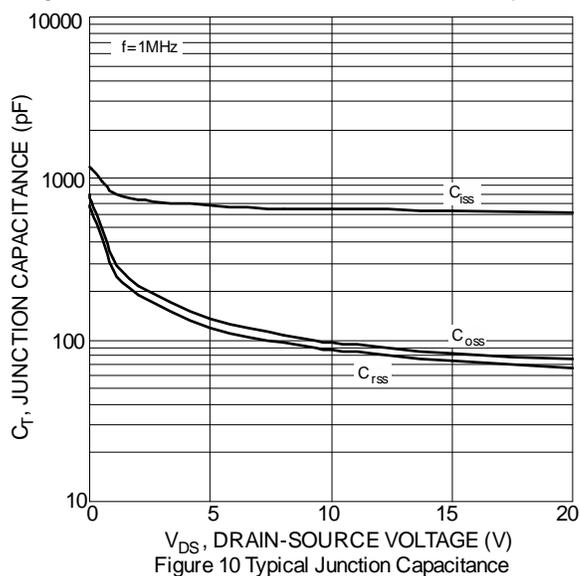


Figure 10 Typical Junction Capacitance

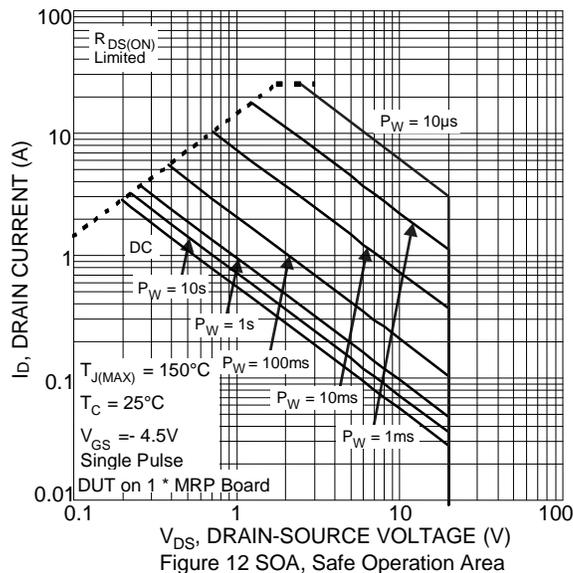


Figure 12 SOA, Safe Operation Area

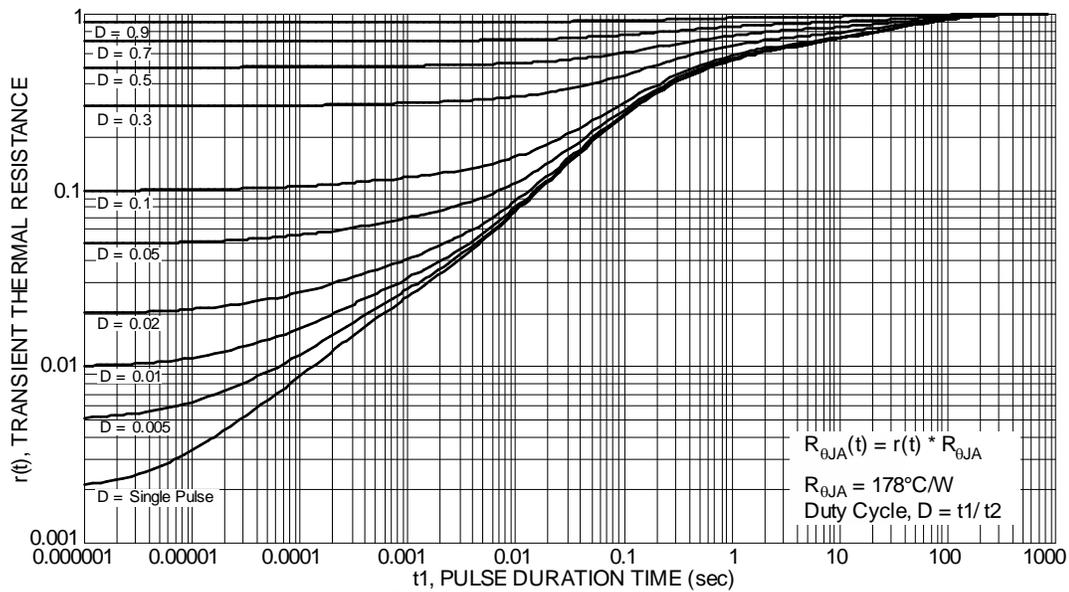
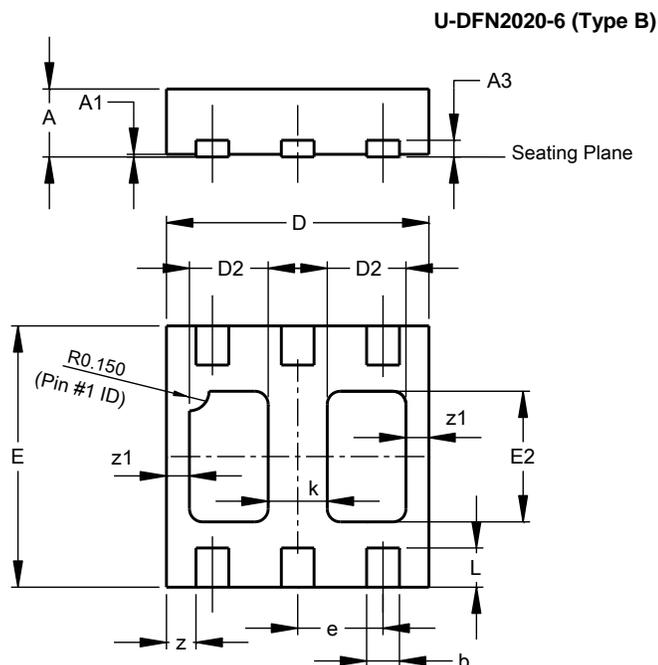


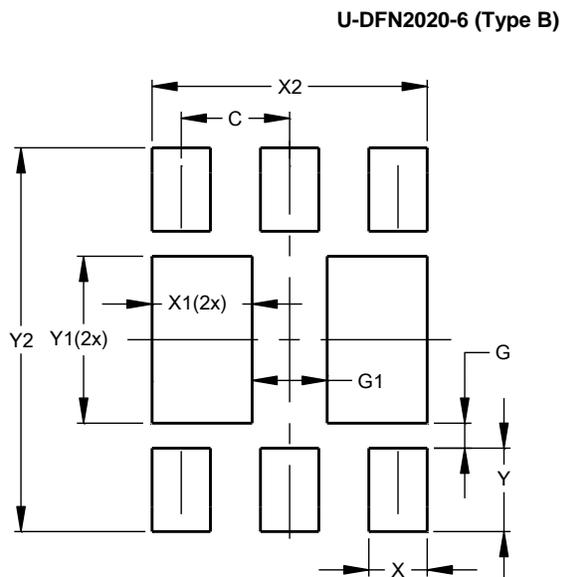
Figure 13 Transient Thermal Resistance

Package Outline Dimensions



U-DFN2020-6 (Type B)			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	0.50	0.70	0.60
e	-	-	0.65
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
k	-	-	0.45
L	0.25	0.35	0.30
z	-	-	0.225
z1	-	-	0.175
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
G	0.150
G1	0.450
X	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2.300