优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D $T_A = +25°C$
-20V	710mΩ @ V_{GS} = -4.5V	-0.63A
	930mΩ @ V_{GS} = -2.5V	-0.55A
	1250mΩ @ V_{GS} = -1.8V	-0.48A

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- DC-DC converters
- Load switches
- Power-management functions

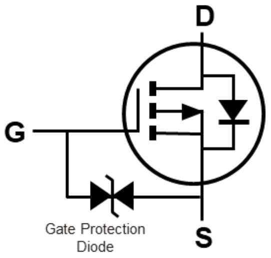
Mechanical Data

- Package: SOT523
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Annealed over Alloy 42 Leadframe. Solderable per MIL-STD-202, Method 208 ⓔ3
- Terminal Connections: See Diagram
- Weight: 0.002 grams (Approximate)

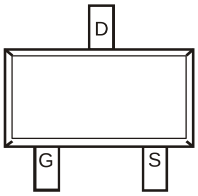
ESD PROTECTED

SOT523

Top View



Equivalent Circuit



Top View

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +75°C	I_D	-0.63 -0.51	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-0.4	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-2.5	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	Steady State	P_D	0.26	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	480	°C/W
Total Power Dissipation (Note 6)	Steady State	P_D	0.44	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	287	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.5	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	390	710	mΩ	V_{GS} = -4.5V, I_D = -400mA
		—	590	930		V_{GS} = -2.5V, I_D = -300mA
		—	770	1250		V_{GS} = -1.8V, I_D = -100mA
Diode Forward Voltage (Note 7)	V_{SD}	—	-0.8	-1.2	V	V_{GS} = 0V, I_S = -300mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	33	—	pF	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	10	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3	—	pF	
Total Gate Charge	Q_g	—	1.4	—	nC	V_{GS} = -4.5V, V_{DS} = -15V, I_D = -1A
Gate-Source Charge	Q_{gs}	—	0.5	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.6	—	ns	V_{DS} = -10V, I_D = -1A V_{GS} = -4.5V, R_G = 6Ω
Turn-On Rise Time	t_R	—	2.2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	14.4	—	ns	
Turn-Off Fall Time	t_F	—	7.9	—	ns	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

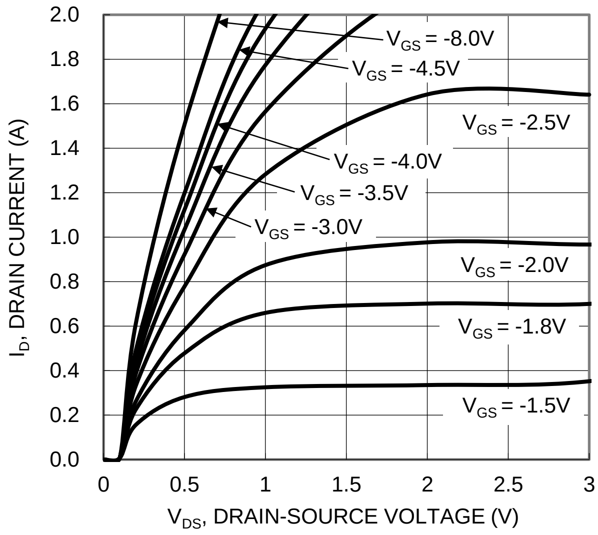


Figure 1. Typical Output Characteristic

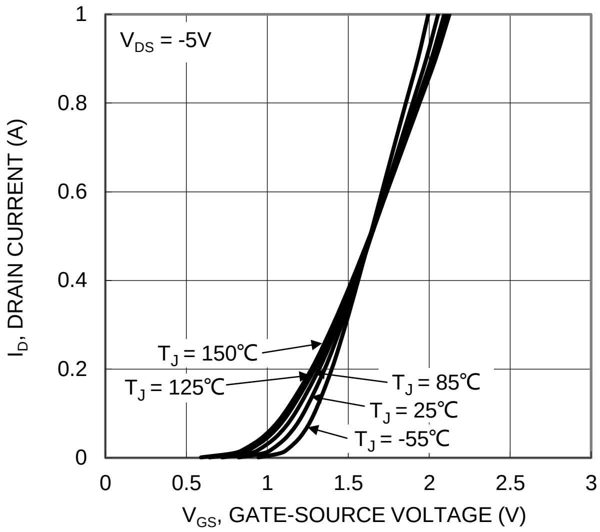


Figure 2. Typical Transfer Characteristic

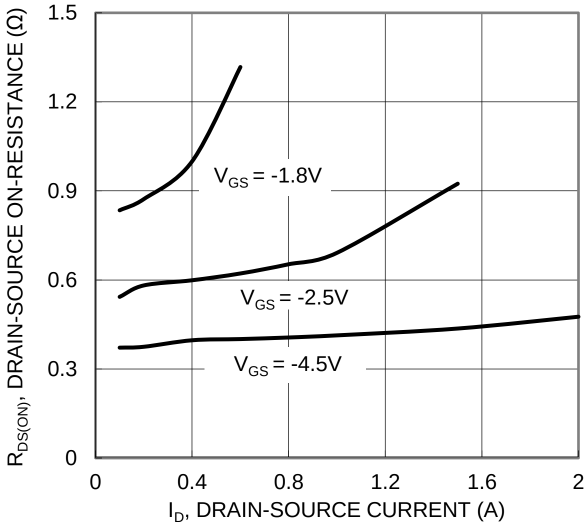


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

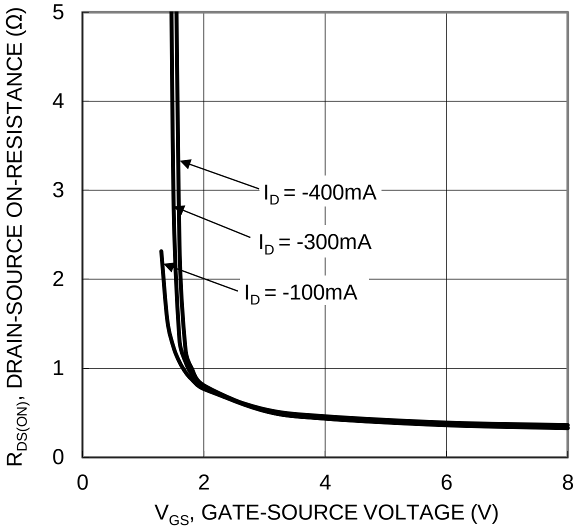


Figure 4. Typical Transfer Characteristic

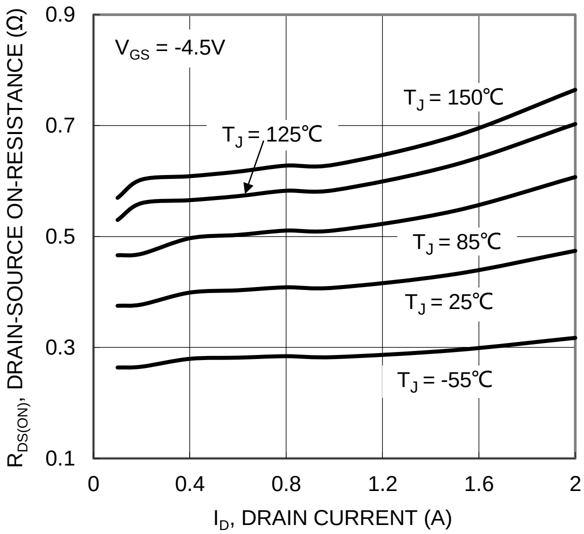


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

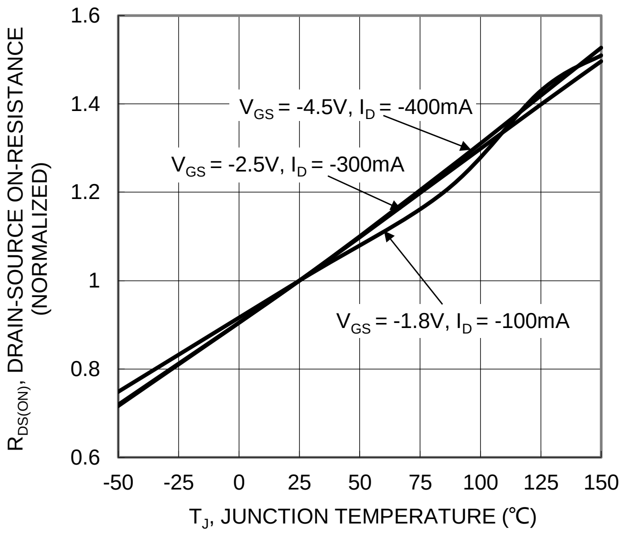


Figure 6. On-Resistance Variation with Junction Temperature

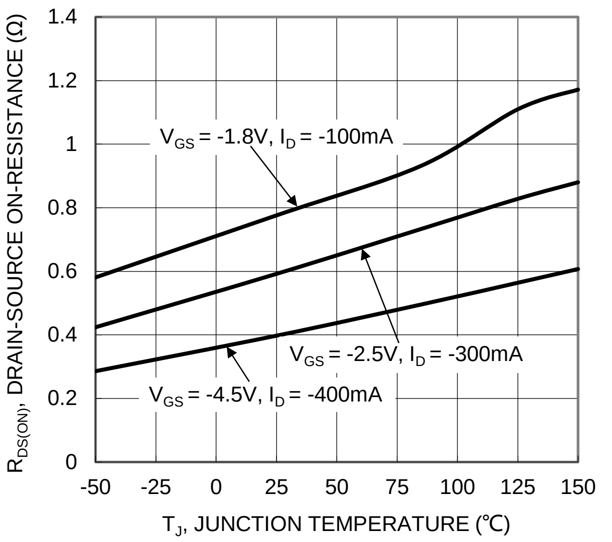


Figure 7. On-Resistance Variation with Junction Temperature

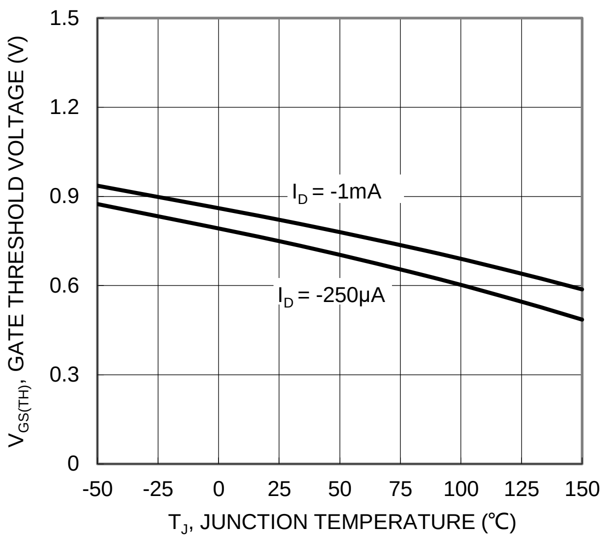


Figure 8. Gate Threshold Variation vs. Junction Temperature

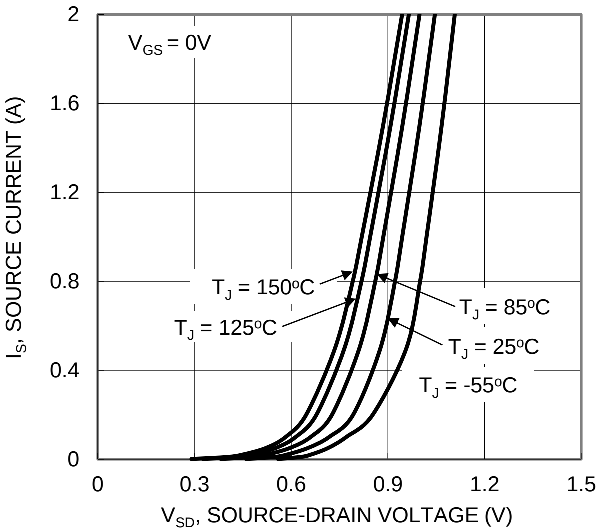


Figure 9. Diode Forward Voltage vs. Current

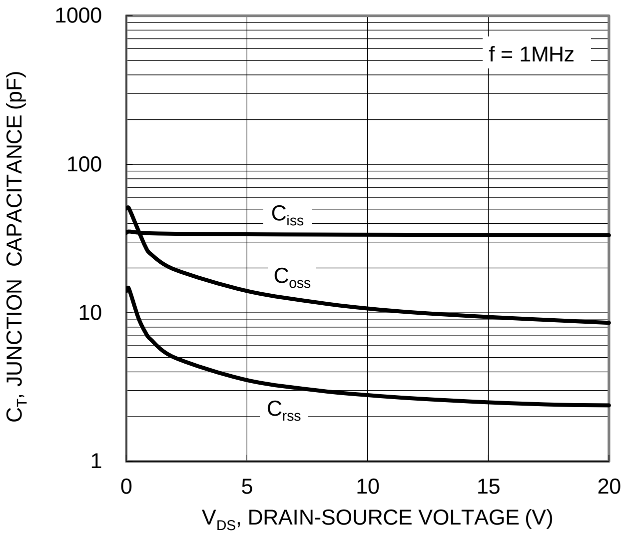


Figure 10. Typical Junction Capacitance

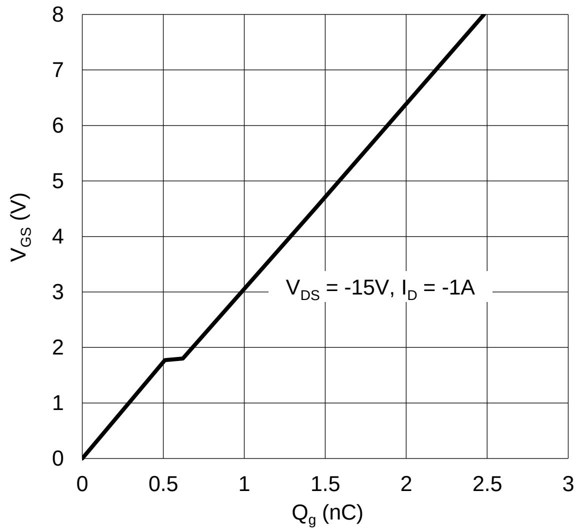


Figure 11. Gate Charge

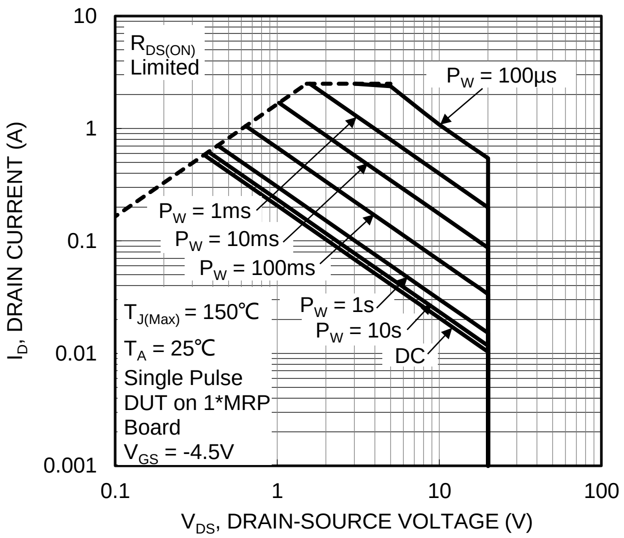


Figure 12. SOA, Safe Operation Area

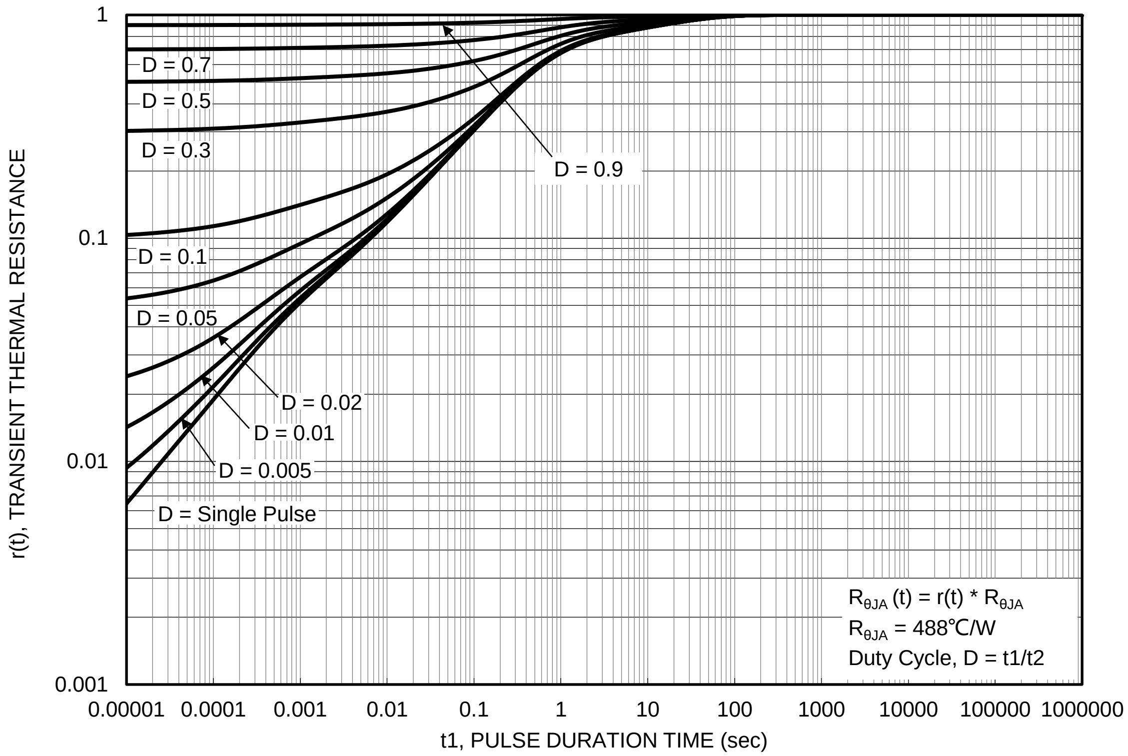
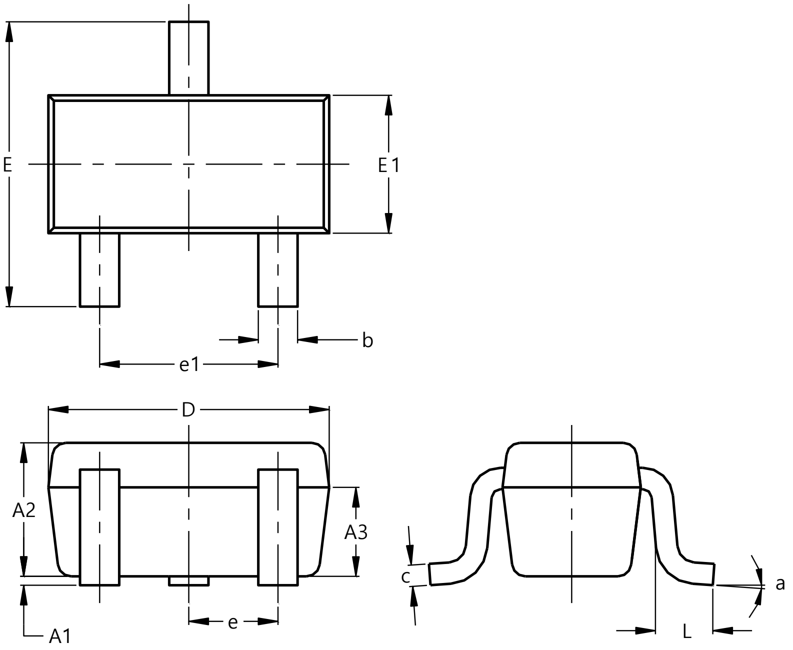


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

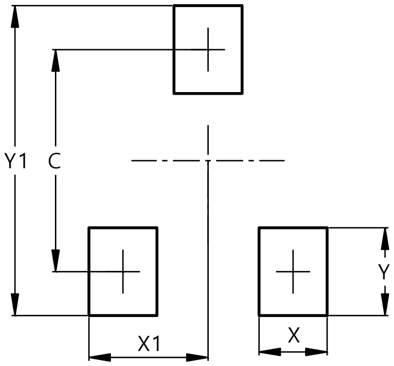
SOT523



SOT523			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.60	0.80	0.75
A3	0.45	0.65	0.50
b	0.15	0.30	0.22
c	0.10	0.20	0.12
D	1.50	1.70	1.60
E	1.45	1.75	1.60
E1	0.75	0.85	0.80
e	0.50 BSC		
e1	0.90	1.10	1.00
L	0.20	0.40	0.33
a	0°	--	8°
All Dimensions in mm			

Suggested Pad Layout

SOT523



Dimensions	Value (in mm)
C	1.29
X	0.40
X1	0.70
Y	0.51
Y1	1.80