优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(on)}$ Max	I_D T_A = +25°C
-20V	0.75Ω @ V_{GS} = -4.5V	-0.99A
	1.05Ω @ V_{GS} = -2.5V	-0.83A

Features and Benefits

- 0.6mm^2 Footprint—Thirteen Times Smaller than SOT23
- Low Gate Threshold Voltage
- Fast Switching Speed

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Load Switch

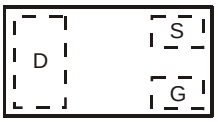
Mechanical Data

- Package: X1-DFN1006-3
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.001 grams (Approximate)

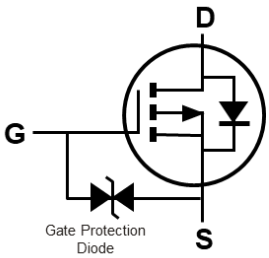
ESD Protected Gate

X1-DFN1006-3

Bottom View



Top View
Internal Schematic



Equivalent Circuit

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±6	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-0.99 -0.79	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)			I_{DM}	-2.6	A

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.55	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\Theta JA}$	229	°C/W
Total Power Dissipation (Note 6)	P_D	1.11	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\Theta JA}$	113	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-100	nA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±2.0	μA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	0.4	0.75	Ω	V_{GS} = -4.5V, I_D = -430mA
		—	0.5	1.05		V_{GS} = -2.5V, I_D = -300mA
		—	0.67	1.5		V_{GS} = -1.8V, I_D = -150mA
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0V, I_S = -150mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	49	—	pF	V_{DS} = -16V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	12	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3.4	—	pF	
Total Gate Charge	Q_g	—	0.7	—	nC	V_{GS} = -4.5V, V_{DS} = -10V, I_D = -250mA
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	16	—	ns	V_{DS} = -10V, V_{GS} = -4.5V, R_g = 10Ω, R_L = 47Ω I_D = -200mA
Turn-On Rise Time	t_R	—	15	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	213	—	ns	
Turn-Off Fall Time	t_F	—	89	—	ns	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 25mm × 25mm square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

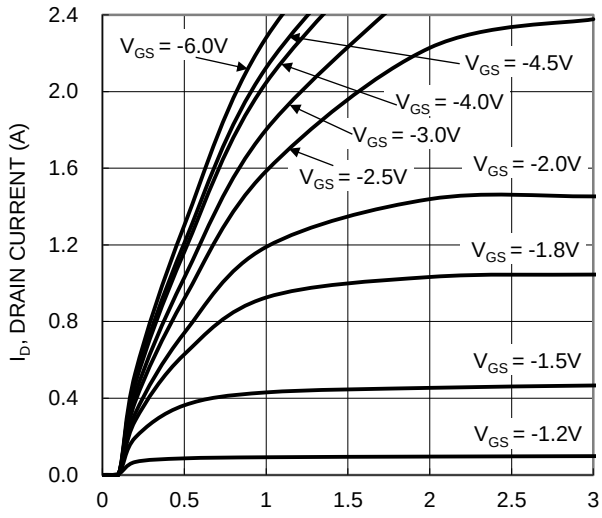


Figure 1. Typical Output Characteristic

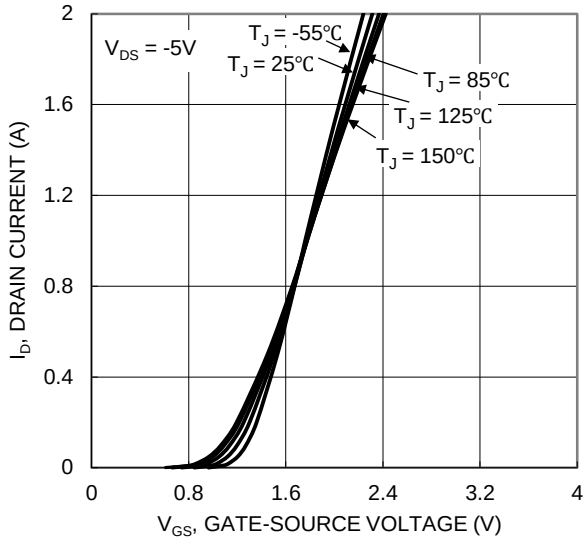


Figure 2. Typical Transfer Characteristic

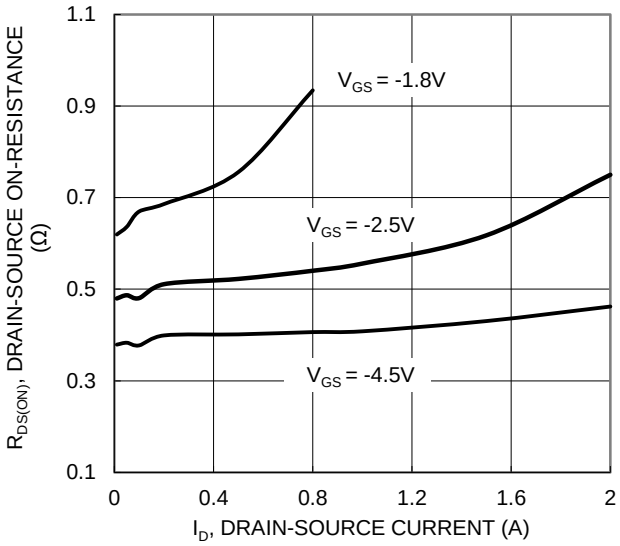


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

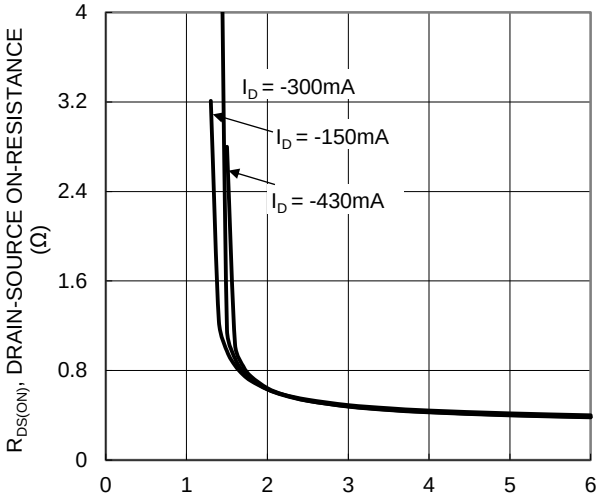


Figure 4. Typical Transfer Characteristic

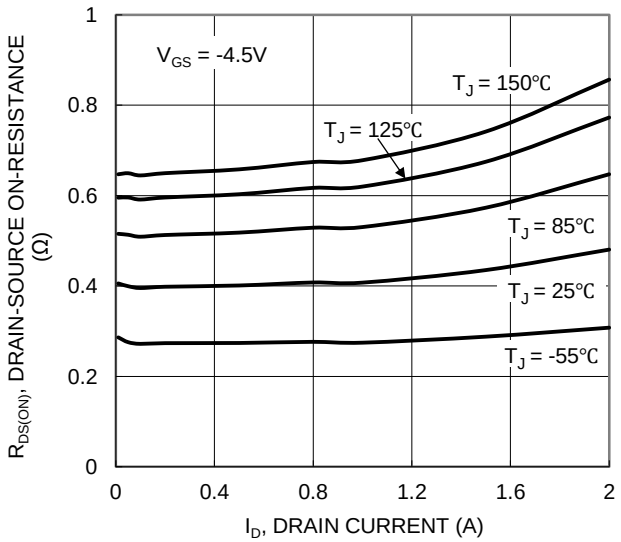


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

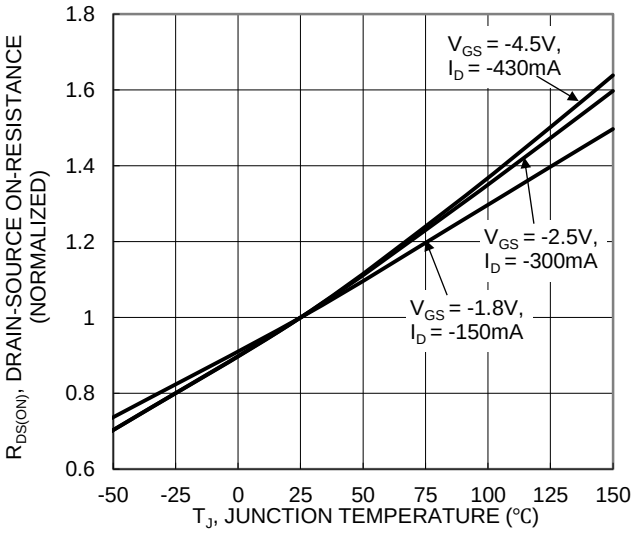


Figure 6. On-Resistance Variation with Temperature

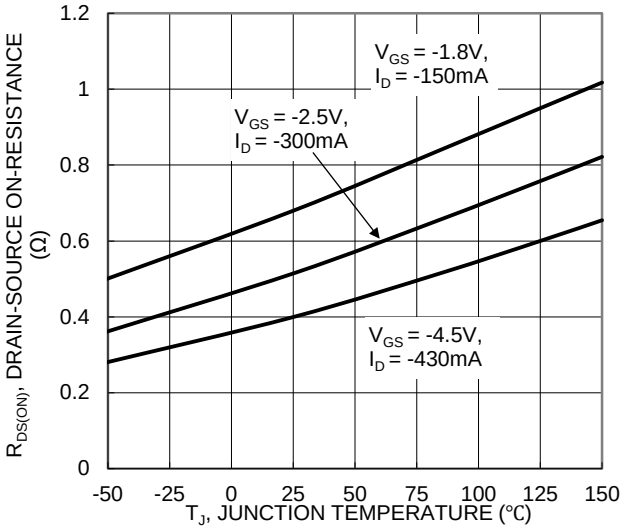


Figure 7. On-Resistance Variation with Temperature

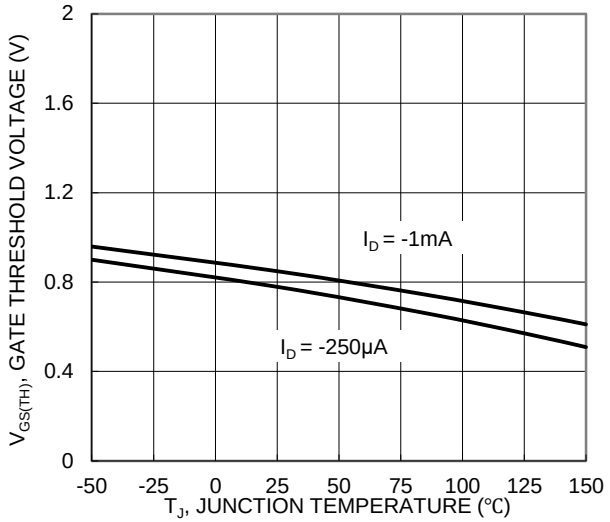


Figure 8. Gate Threshold Variation vs. Junction Temperature

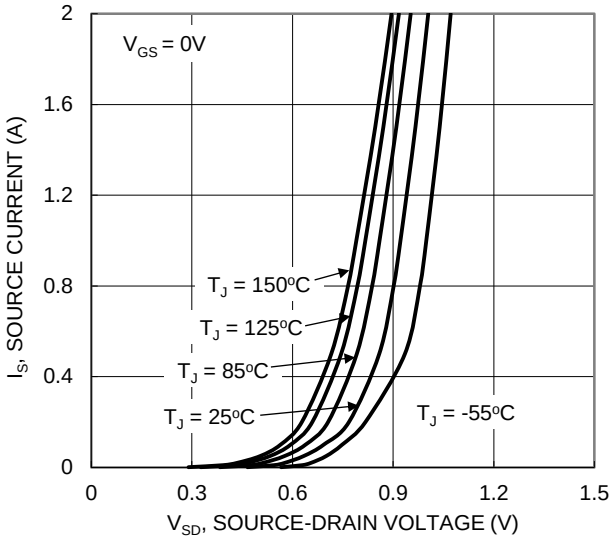


Figure 9. Diode Forward Voltage vs. Current

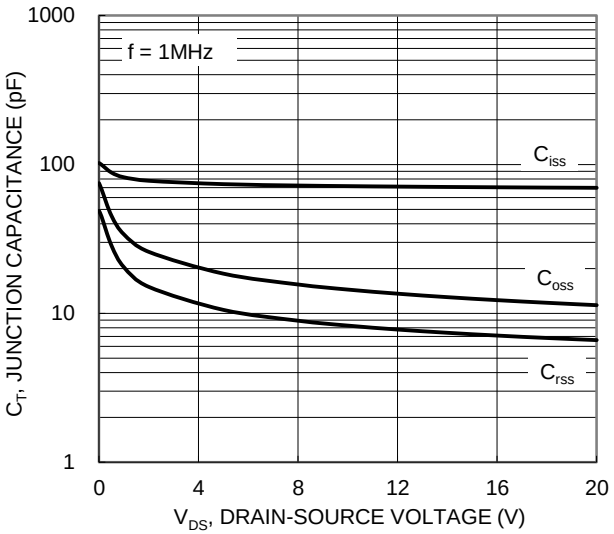


Figure 10. Typical Junction Capacitance

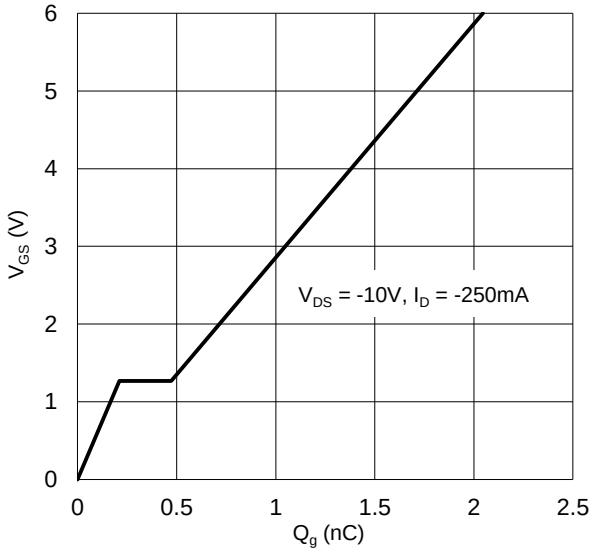


Figure 11. Gate Charge

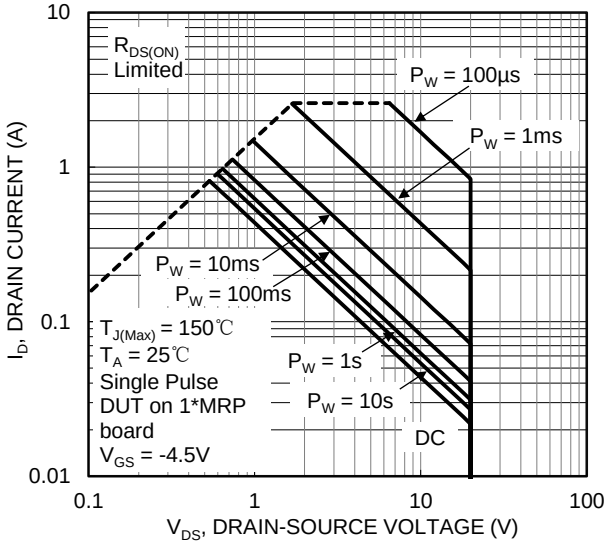


Figure 12. SOA, Safe Operation Area

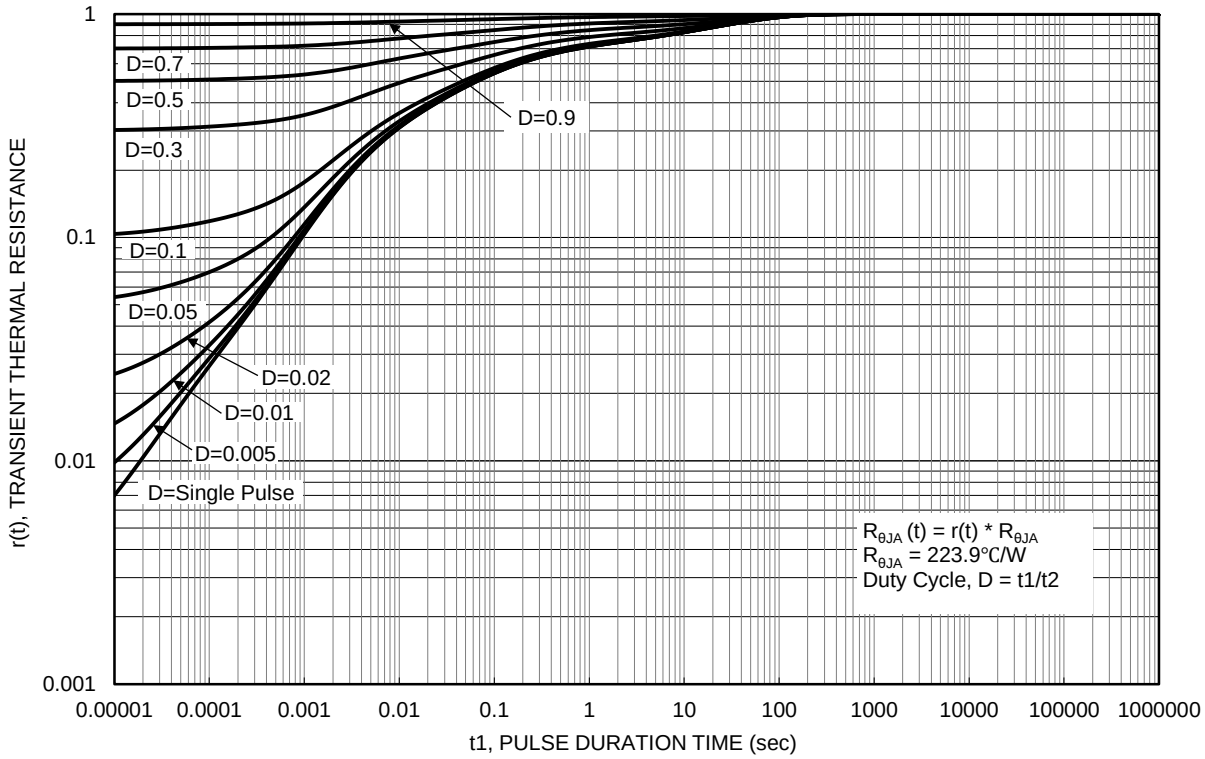
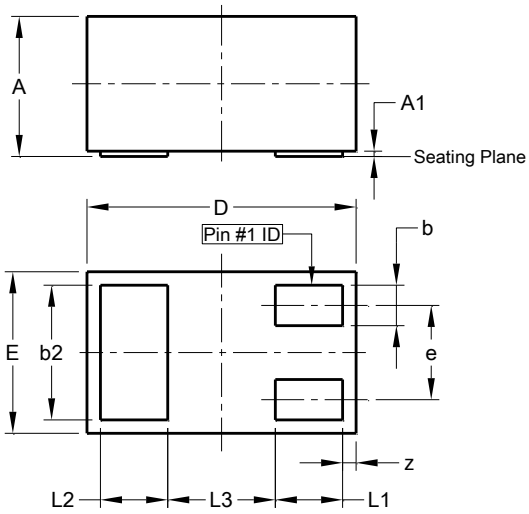


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

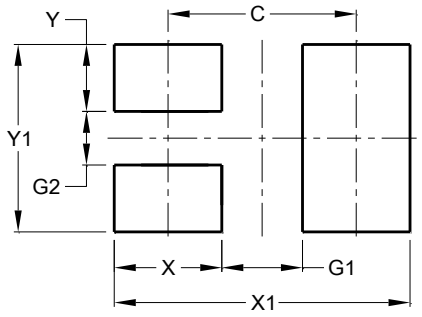
X1-DFN1006-3



X1-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

X1-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70