



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



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Product Summary

BV _{DSS}	R _{DS(ON)} MAX	I _D MAX T _A = +25°C
-30V	50mΩ @ V _{GS} = -10V	-4.3A
	70mΩ @ V _{GS} = -4.5V	-3.7A

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

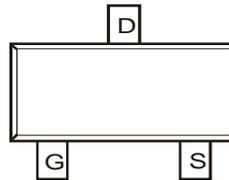
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.009 grams (Approximate)

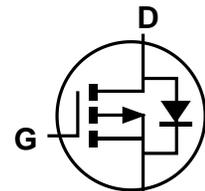
SOT23 (Standard)



Top View



Top View
Pin Configuration



Equivalent Circuit

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Drain Current (Note 5) $V_{GS} = -10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	-4.3	A
		$T_A = +70^\circ\text{C}$		-3.4	
Pulsed Drain Current (Note 6)			I_{DM}	-20	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.38	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	91	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100 ± 800	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ $V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1	—	-2.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	35 50	50 70	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -6.0\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$
Diode Forward Voltage	V_{SD}	—	—	-1.2	V	$V_{GS} = 0\text{V}, I_S = -1.7\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	642	—	pF	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	65	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	48	—	pF	
Gate Resistance	R_G	—	15	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_G	—	5.8	—	nC	$V_{DS} = -15\text{V}, I_D = -6\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_G	—	11.8	—	nC	$V_{DS} = -15\text{V}, I_D = -6\text{A}$
Gate-Source Charge	Q_{GS}	—	2.0	—		
Gate-Drain Charge	Q_{GD}	—	2.4	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.9	—	ns	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V},$ $I_D = -1\text{A}, R_G = 6.0\Omega$
Rise Time	t_R	—	4.7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	35.2	—		
Fall Time	t_F	—	18.2	—		

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
 - Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

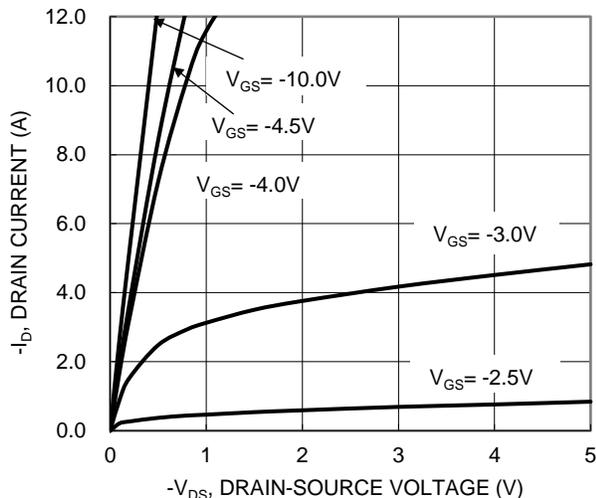


Figure 1. Typical Output Characteristic

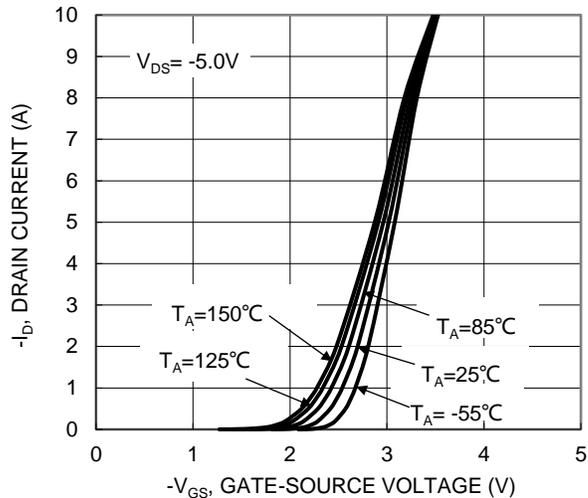


Figure 2. Typical Transfer Characteristic

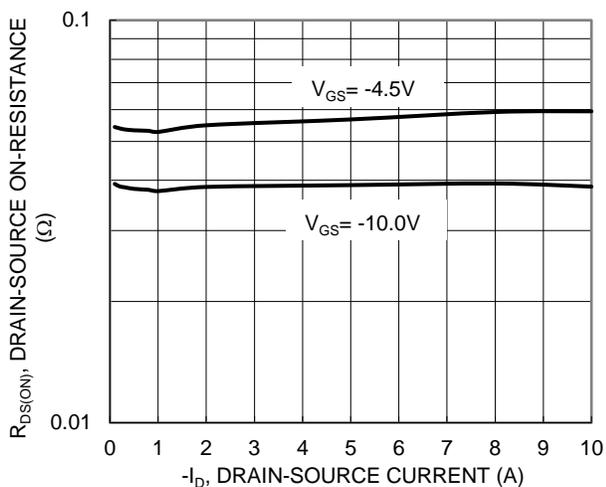


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

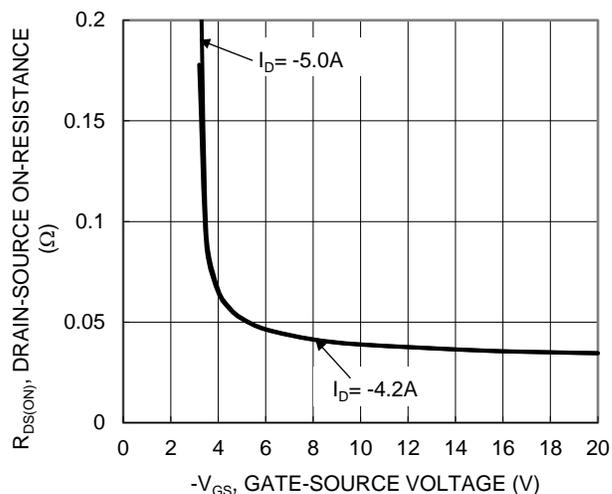


Figure 4. Typical Transfer Characteristic

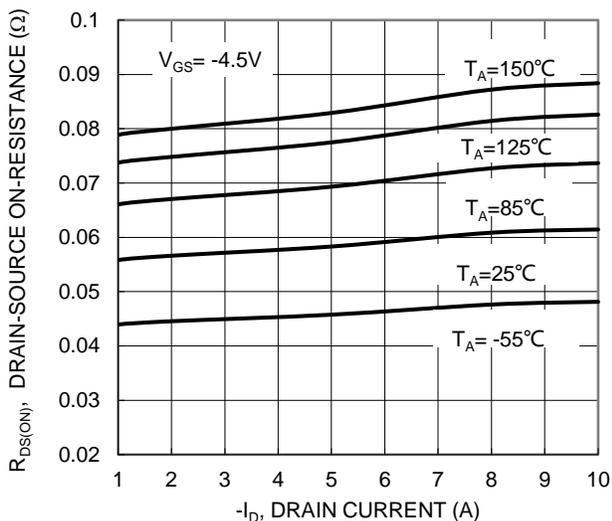


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

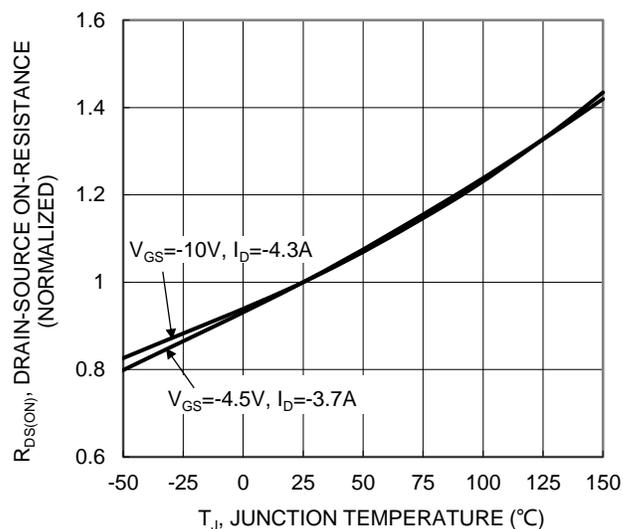


Figure 6. On-Resistance Variation with Temperature

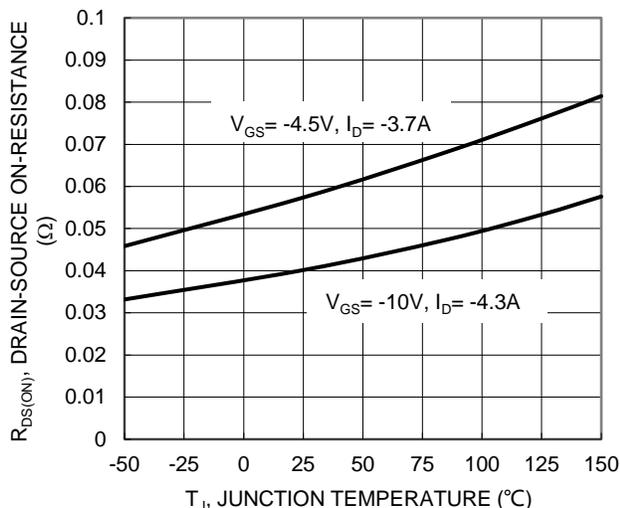


Figure 7. On-Resistance Variation with Temperature

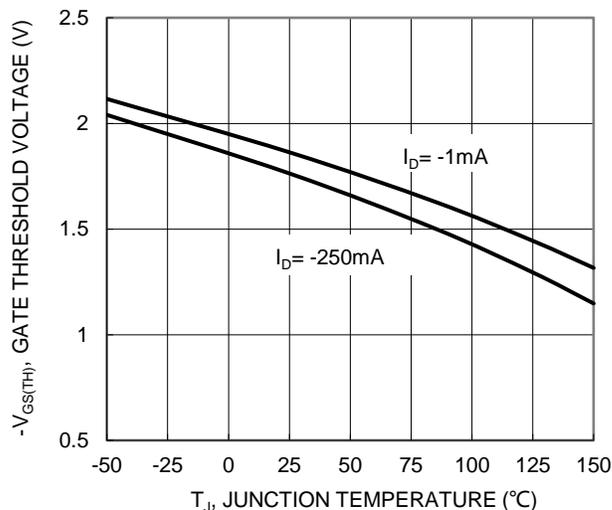


Figure 8. Gate Threshold Variation vs. Junction Temperature

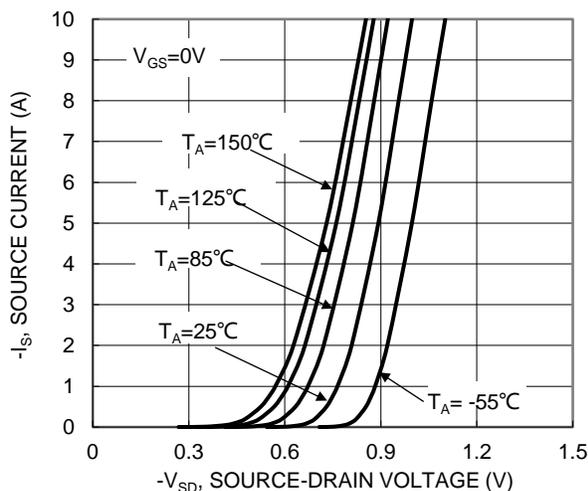


Figure 9. Diode Forward Voltage vs. Current

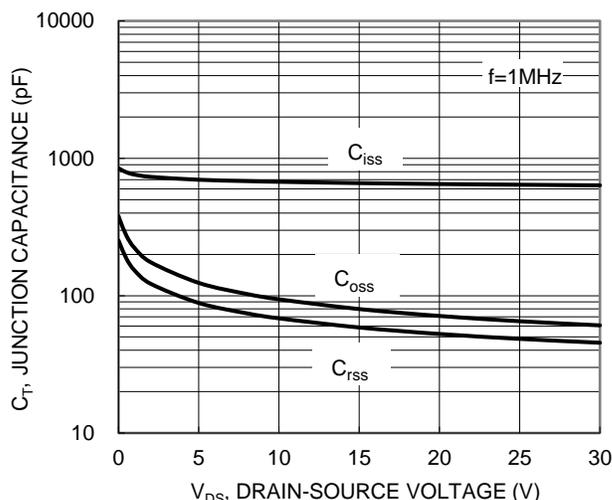


Figure 10. Typical Junction Capacitance

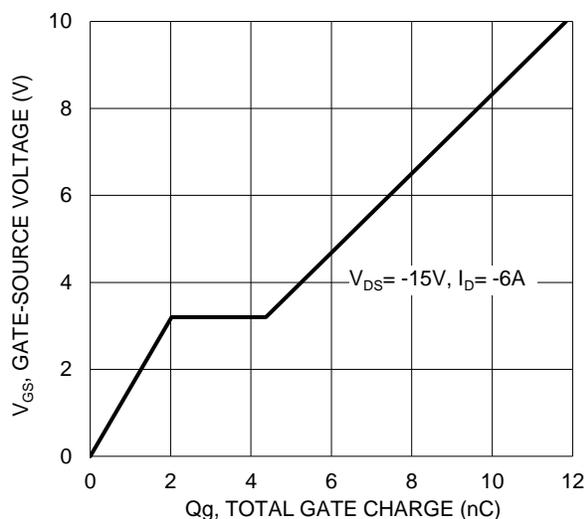


Figure 11. Gate Charge

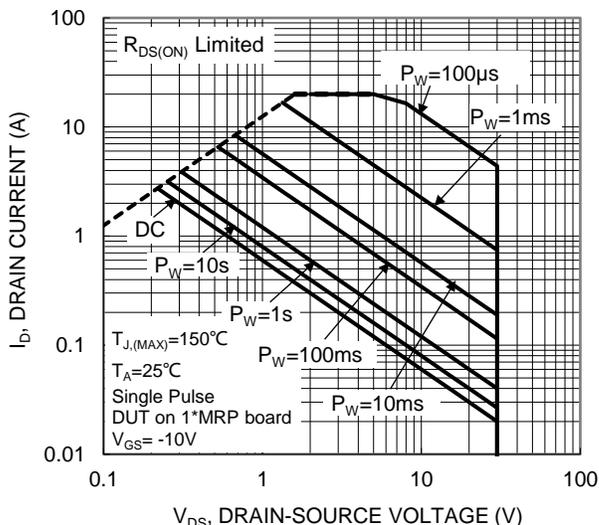


Figure 12. SOA, Safe Operation Area

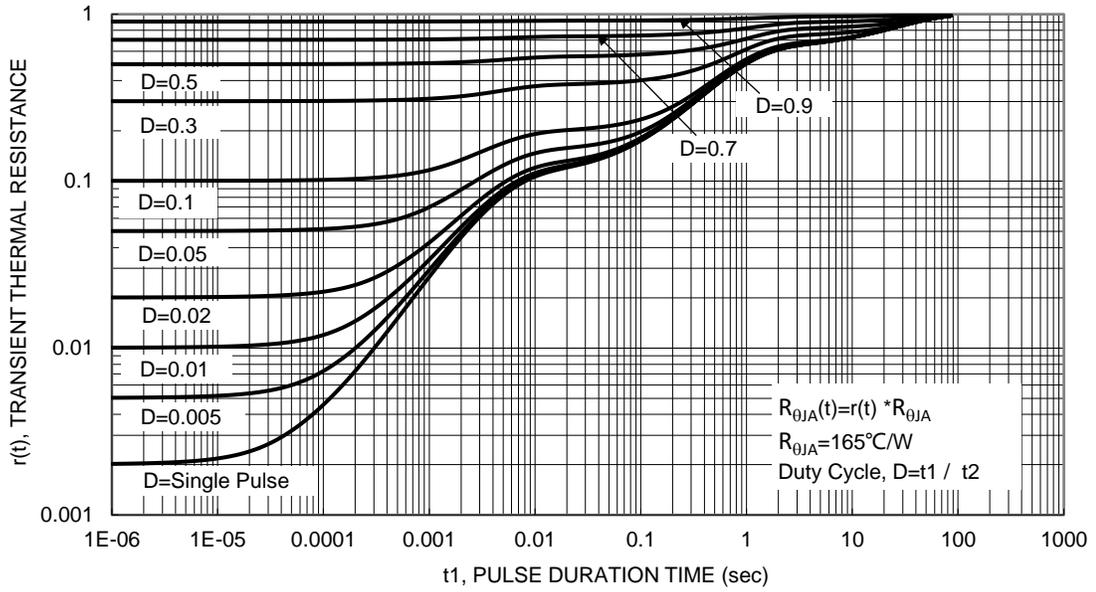
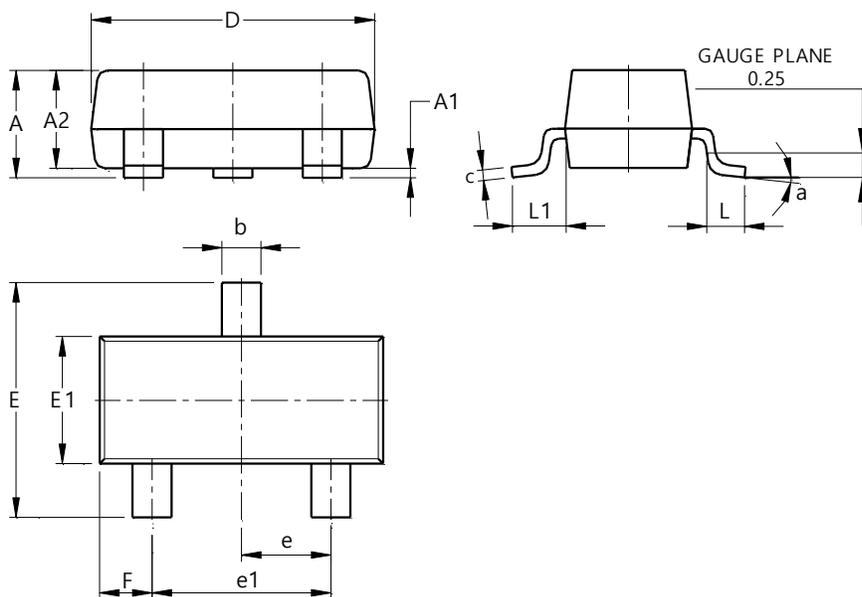


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

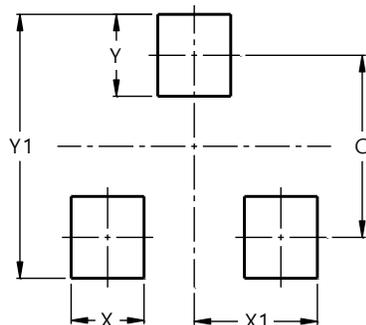
SOT23 (Standard)



SOT23 (Standard)			
Dim	Min	Max	Typ
A	0.90	1.15	1.025
A1	0.00	0.10	0.05
A2	0.85	1.10	0.975
b	0.30	0.51	0.40
c	0.080	0.202	0.11
D	2.80	3.00	2.90
E	2.25	2.55	2.40
E1	1.20	1.40	1.30
e	0.89	1.03	0.915
e1	1.78	2.05	1.83
F	0.40	0.60	0.535
L1	0.45	0.61	0.55
L	0.25	0.55	0.40
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23 (Standard)



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9