优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

企业微信二维码

企业QQ二维码

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D $T_A = +25°C$
-30V	70mΩ @V_{GS} = -10V	-3.4A
	130mΩ @V_{GS} = -4.5V	-2.5A

Features and Benefits

- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description

This MOSFET is designed to minimize on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

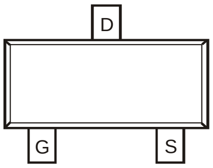
- Load switches
- Power management functions

Mechanical Data

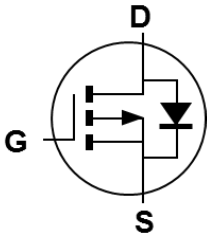
- Package: SOT23
- Package Material: Molded Plastic, "Green" Molding Compound UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.008 grams (Approximate)

SOT23

Top View



Pin Configuration



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-3.4 -2.7	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)			I_{DM}	-22	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	0.8	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{θJA}$	158	°C/W
Power Dissipation (Note 6)	P_D	1.2	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{θJA}$	100	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-800	nA	V_{DS} = -30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-2.1	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	48 83	70 130	mΩ	V_{GS} = -10V, I_D = -3.8A V_{GS} = -4.5V, I_D = -3.0A
Diode Forward Voltage	V_{SD}	—	-0.8	-1.26	V	V_{GS} = 0V, I_S = -2.7A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	366	—	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	51	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	39	—	pF	
Gate Resistance	R_G	—	9.2	—	Ω	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	3.8	—	nC	V_{DS} = -15V, I_D = -3.8A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	7.5	—		
Gate-Source Charge	Q_{gs}	—	1.0	—		
Gate-Drain Charge	Q_{gd}	—	1.1	—		
Turn-On Delay Time	$t_{d(on)}$	—	3.2	—	ns	V_{DS} = -15V, V_{GS} = -10V, I_D = -1A, R_G = 6.0Ω
Rise Time	t_r	—	8.2	—		
Turn-Off Delay Time	$t_{d(off)}$	—	21.7	—		
Fall Time	t_f	—	13.1	—		

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

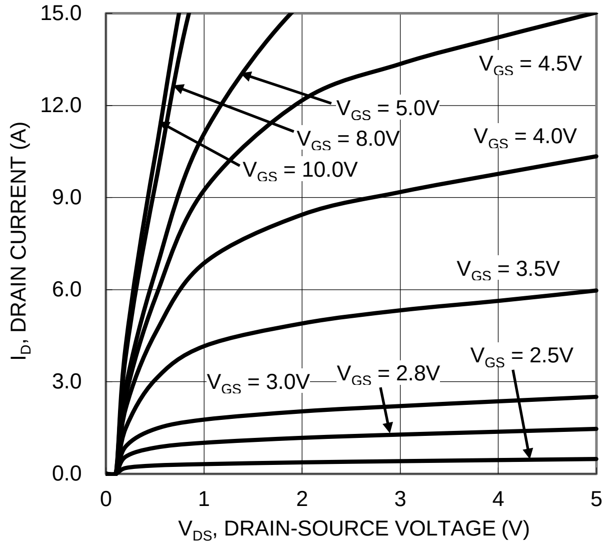


Figure 1. Typical Output Characteristic

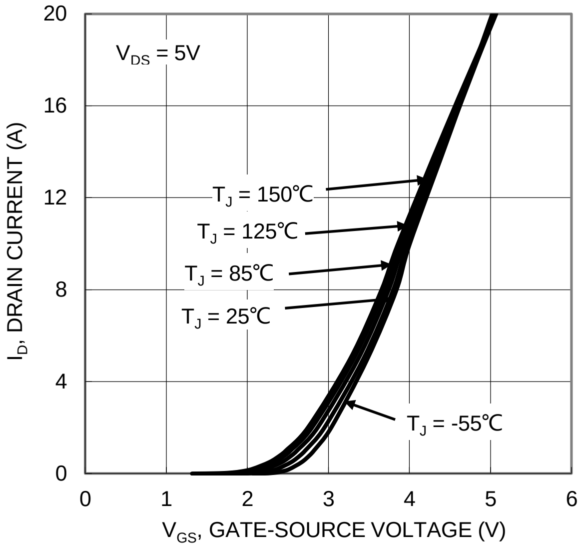


Figure 2. Typical Transfer Characteristic

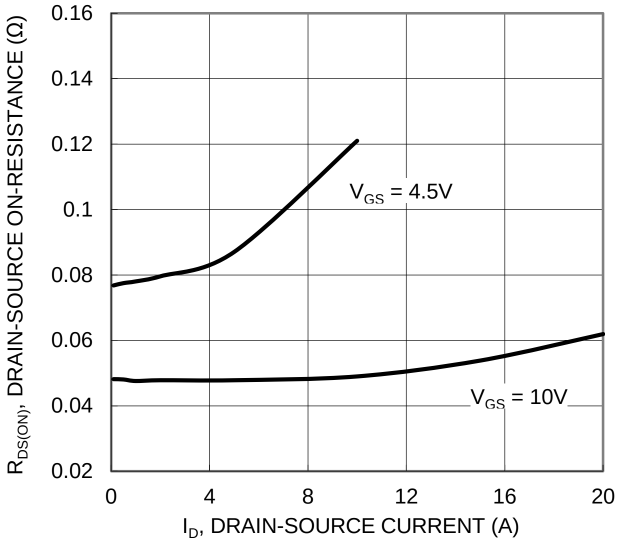


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

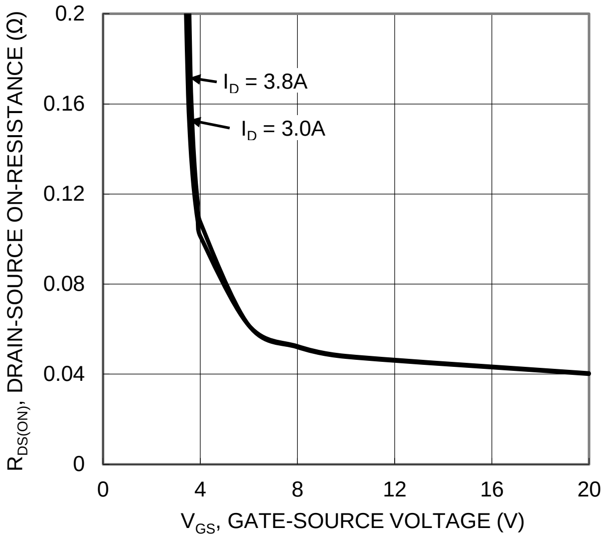


Figure 4. Typical Transfer Characteristic

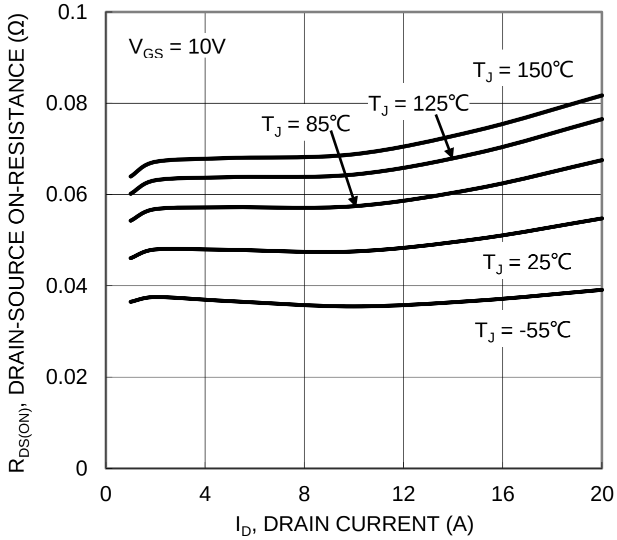


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

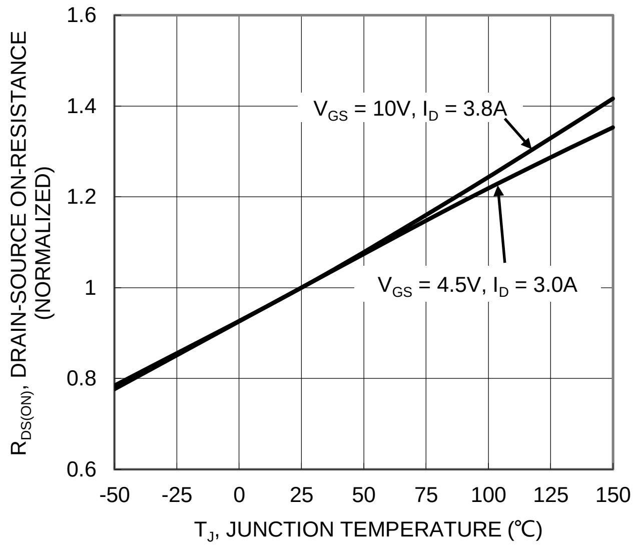


Figure 6. On-Resistance Variation with Junction Temperature

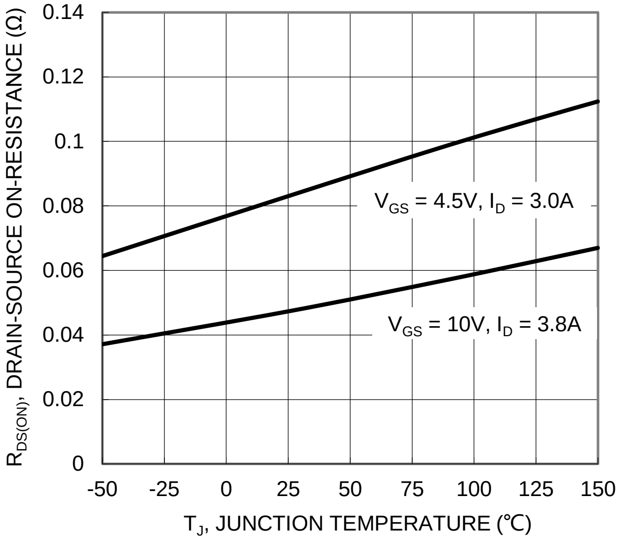


Figure 7. On-Resistance Variation with Junction Temperature

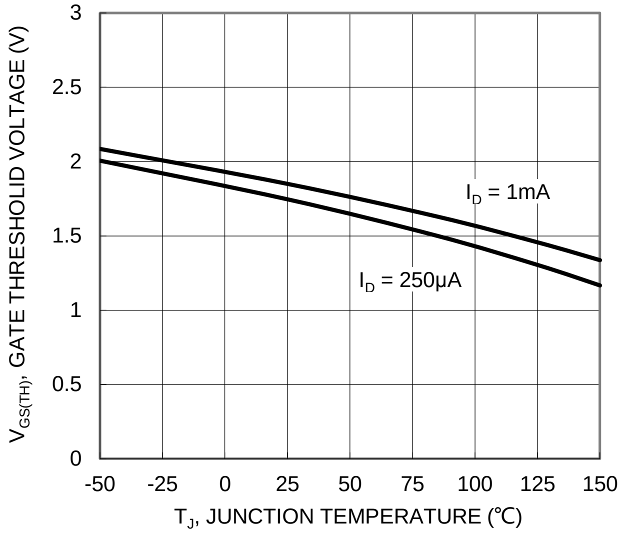


Figure 8. Gate Threshold Variation vs. Junction Temperature

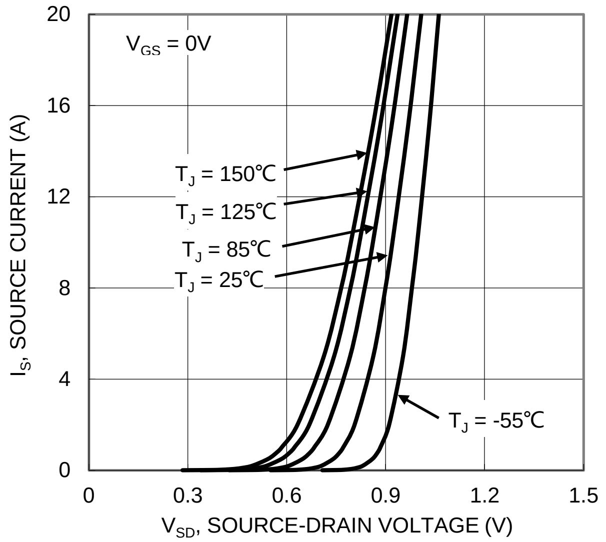


Figure 9. Diode Forward Voltage vs. Current

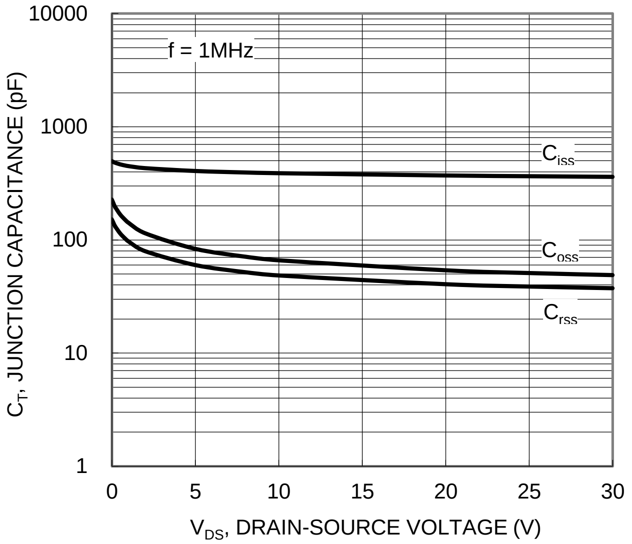


Figure 10. Typical Junction Capacitance

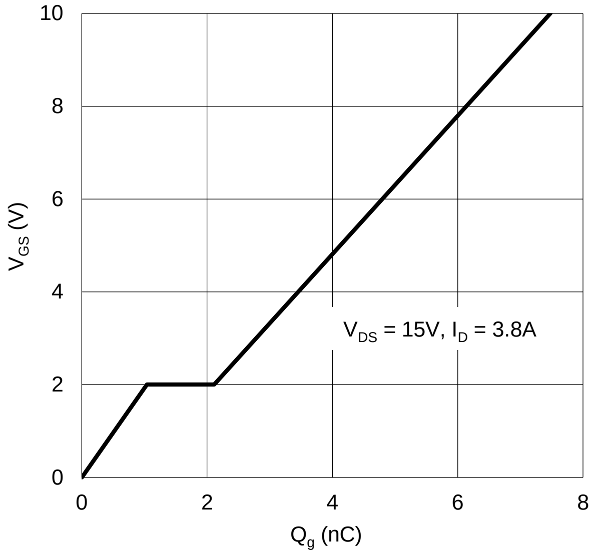


Figure 11. Gate Charge

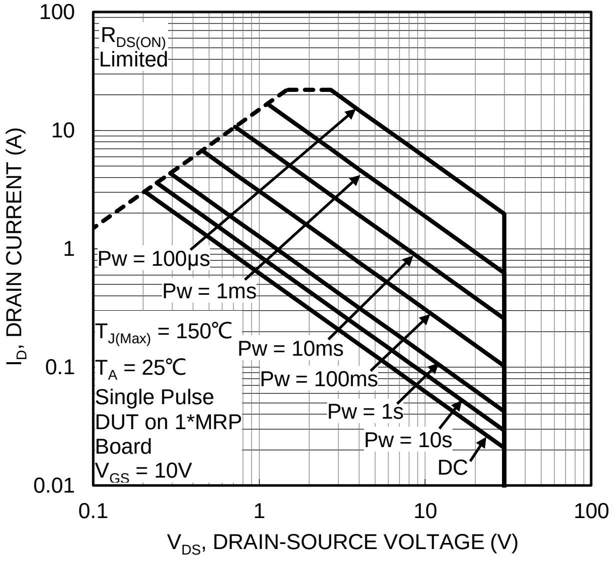


Figure 12. SOA, Safe Operation Area

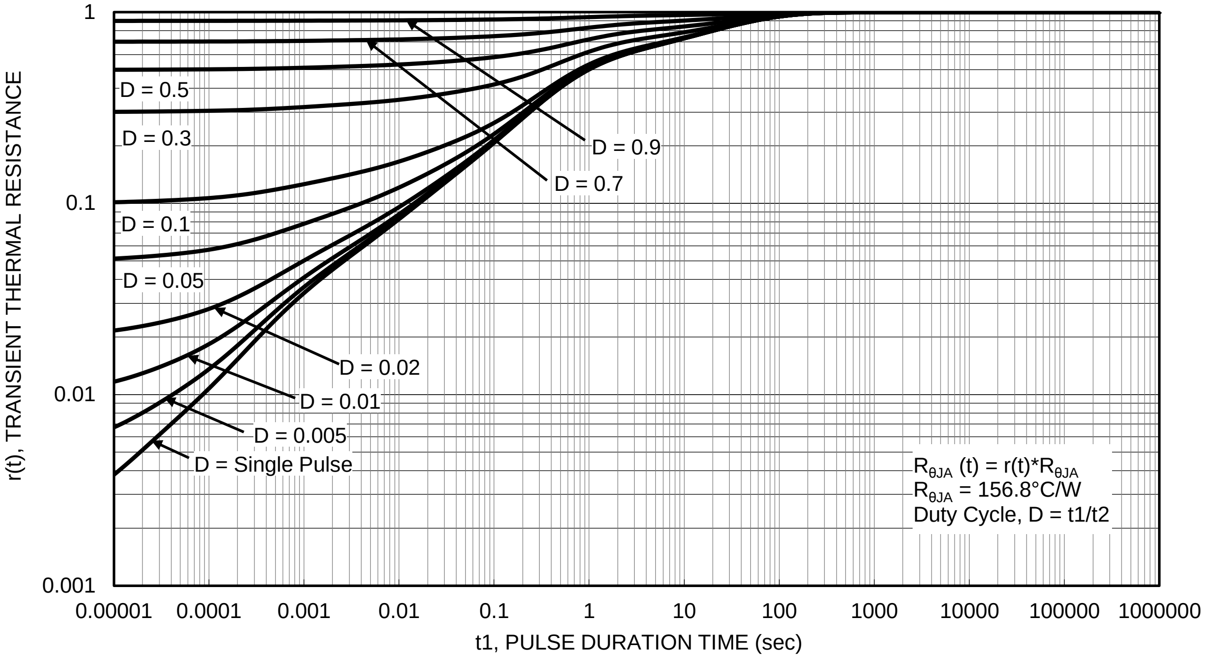
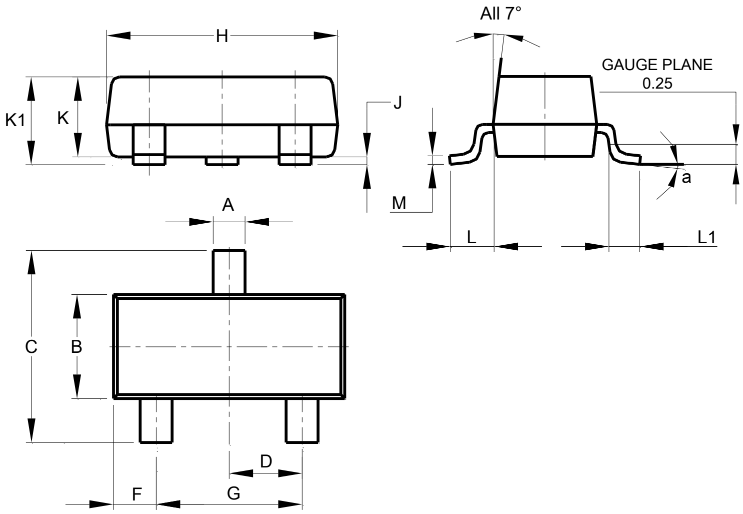


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

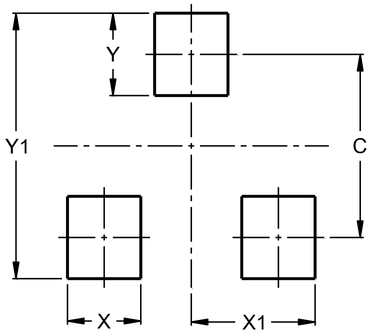
SOT23



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9