优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D T_A = +25°C
-50V	8Ω @ V_{GS} = -5V	-220mA

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed

Description and Applications

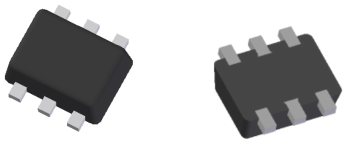
This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- General purpose interfacing switches
- Power management functions
- Analog switches

Mechanical Data

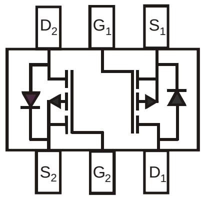
- Package: SOT563
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ⓔ3
- Weight: 0.003 grams (Approximate)

SOT563



Top View

Bottom View



Top View
Internal Schematic

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-50	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = -5V	Steady State	T_A = +25°C	I_D	-220	mA
		T_A = +70°C		-180	
Maximum Body Diode Forward Current (Note 6)			I_S	-220	mA
Pulsed Drain Current (Note 6)			I_{DM}	-1	A
Pulsed Source Current (Note 6)			I_{SM}	-1	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.49	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	259	°C/W
Total Power Dissipation (Note 6)		P_D	0.78	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	159	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-50	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = -50V, V_{GS} = 0V
		—	—	500	nA	V_{DS} = -25V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.8	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250uA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	2.2	8	Ω	V_{GS} = -5V, I_D = -100mA
Diode Forward Voltage	V_{SD}	—	-0.8	-1.4	V	V_{GS} = 0V, I_S = -100mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	37	—	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	5.8	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3.5	—	pF	
Gate Resistance	R_g	—	240	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -5V)	Q_g	—	0.6	—	nC	V_{DS} = -10V, I_D = -100mA
Total Gate Charge (V_{GS} = -10V)	Q_g	—	1.2	—	nC	
Gate-Source Charge	Q_{gs}	—	0.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.01	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	2.6	—	ns	V_{DD} = -30V, V_{GS} = -10V, R_G = 50Ω, I_D = -270mA
Turn-On Rise Time	t_r	—	12	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	36.6	—	ns	
Turn-Off Fall Time	t_f	—	21	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	67	—	ns	I_F = -1A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	78	—	nC	I_F = -1A, di/dt = 100A/μs

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

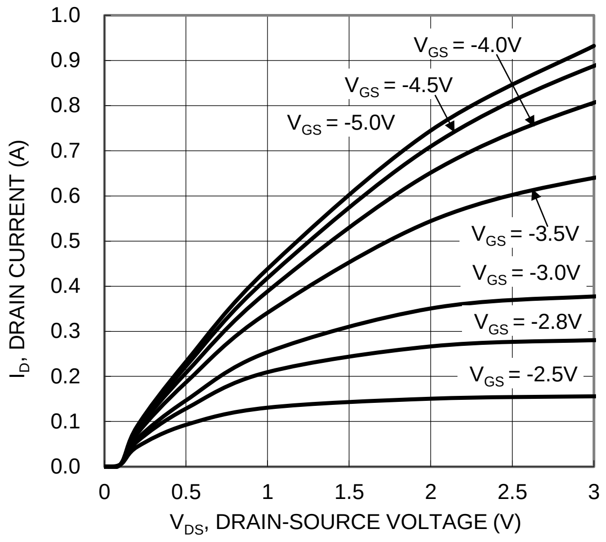


Figure 1. Typical Output Characteristic

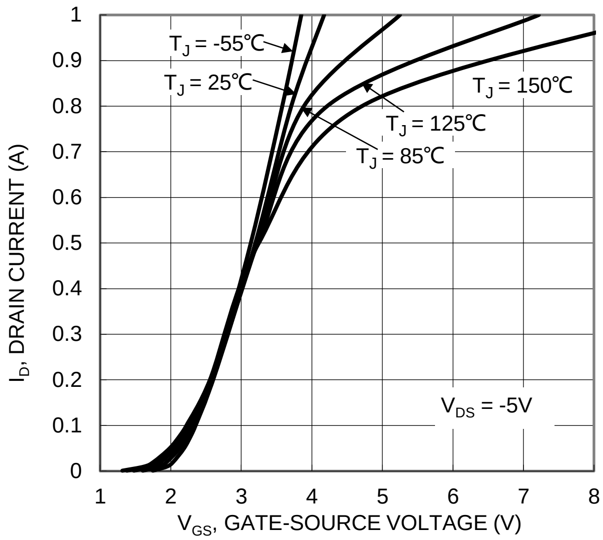


Figure 2. Typical Transfer Characteristic

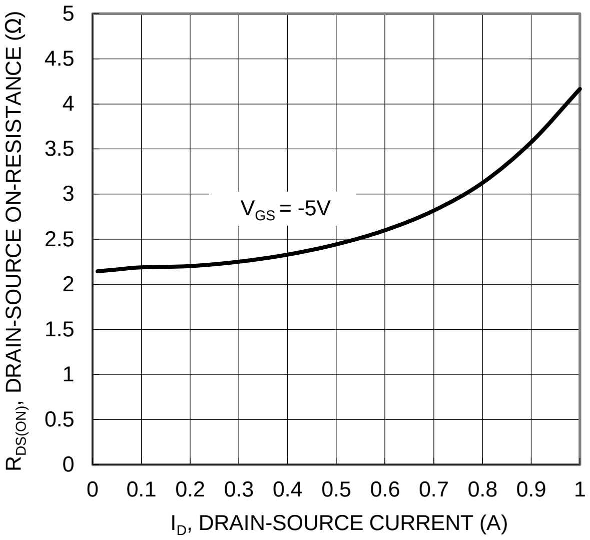


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

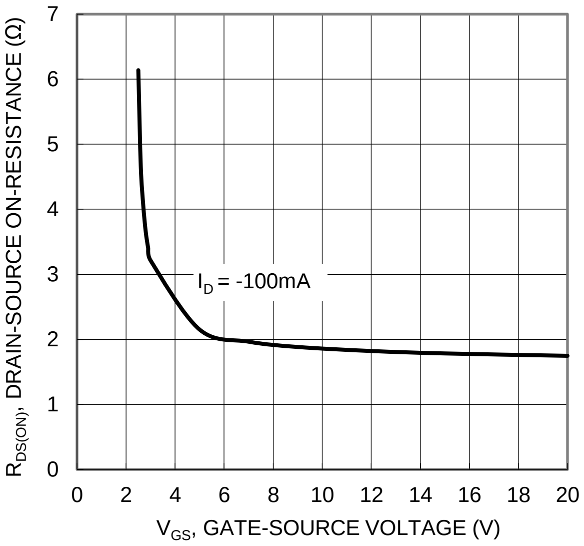


Figure 4. Typical Transfer Characteristic

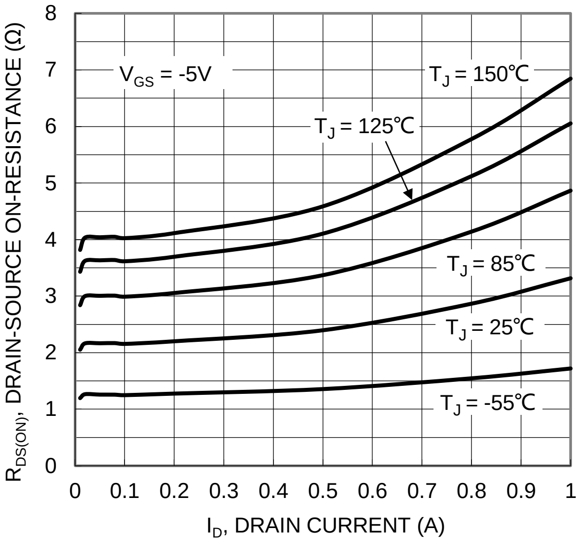


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

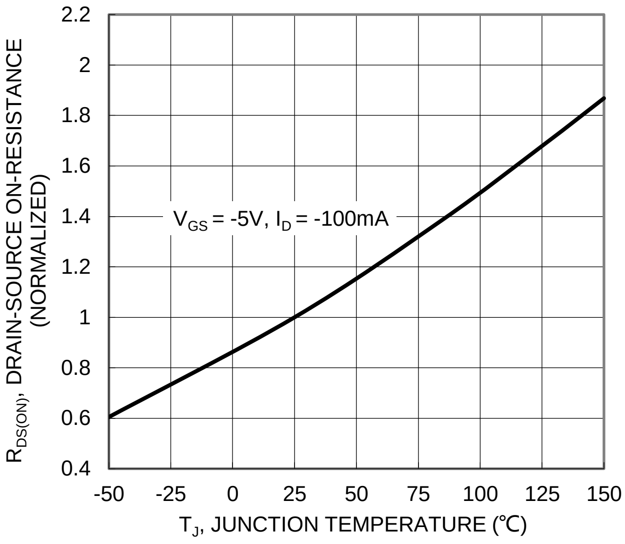


Figure 6. On-Resistance Variation with Temperature

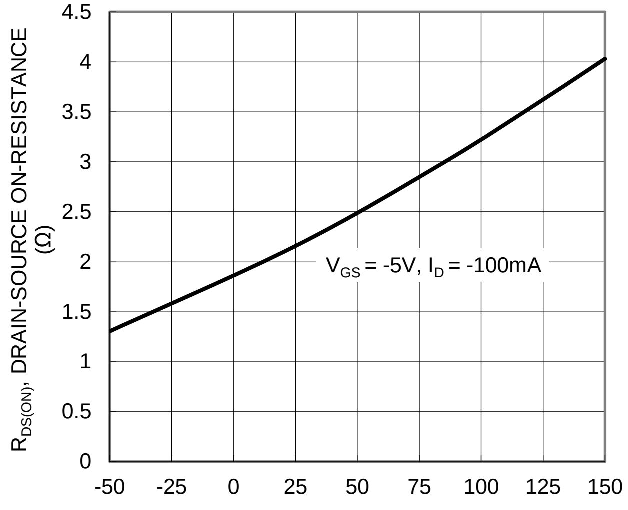


Figure 7. On-Resistance Variation with Temperature

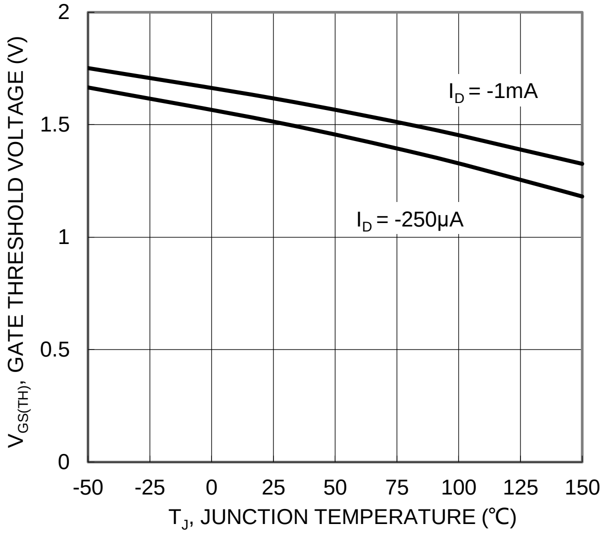


Figure 8. Gate Threshold Variation vs. Junction Temperature

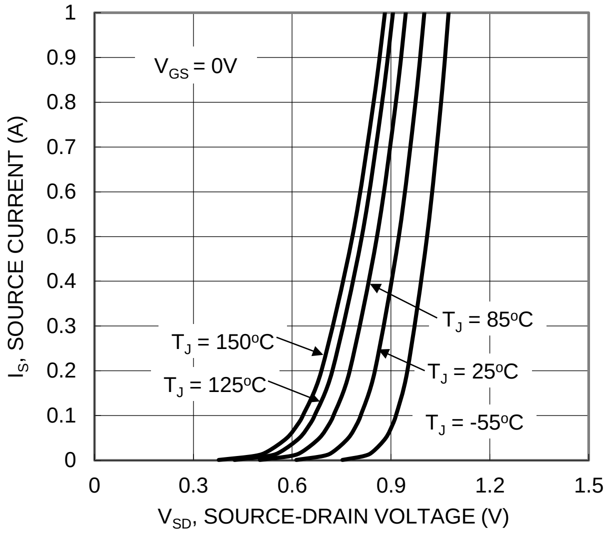


Figure 9. Diode Forward Voltage vs. Current

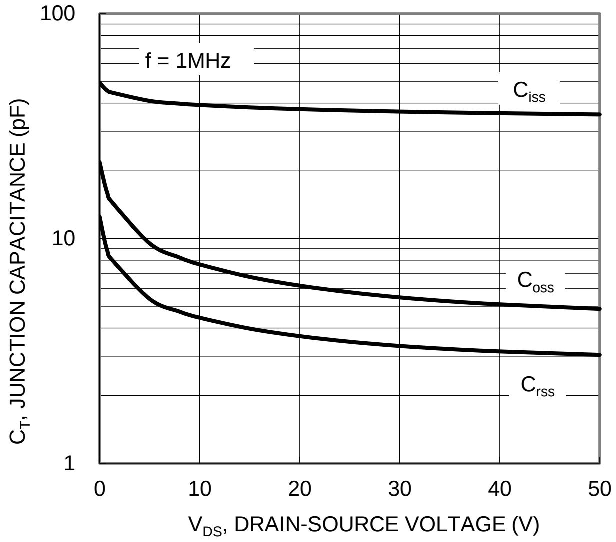


Figure 10. Typical Junction Capacitance

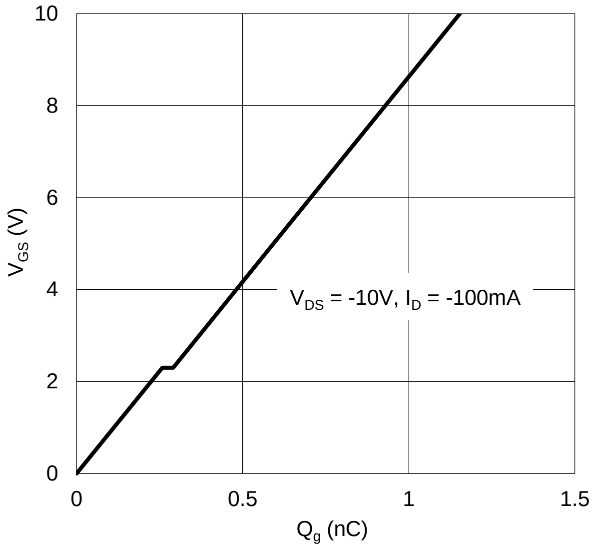


Figure 11. Gate Charge

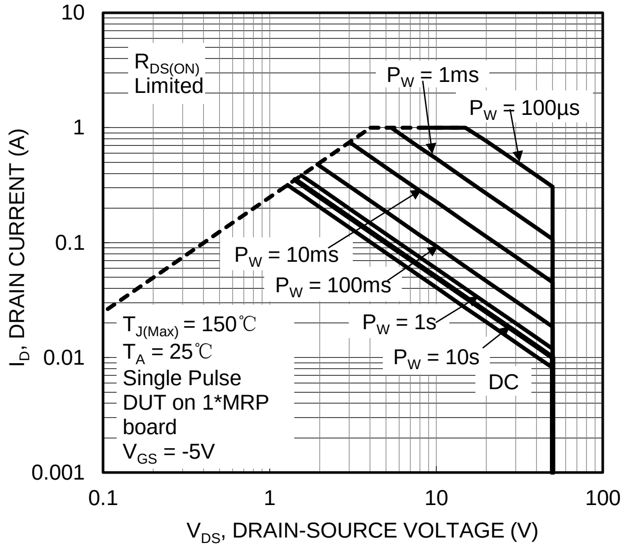


Figure 12. SOA, Safe Operation Area

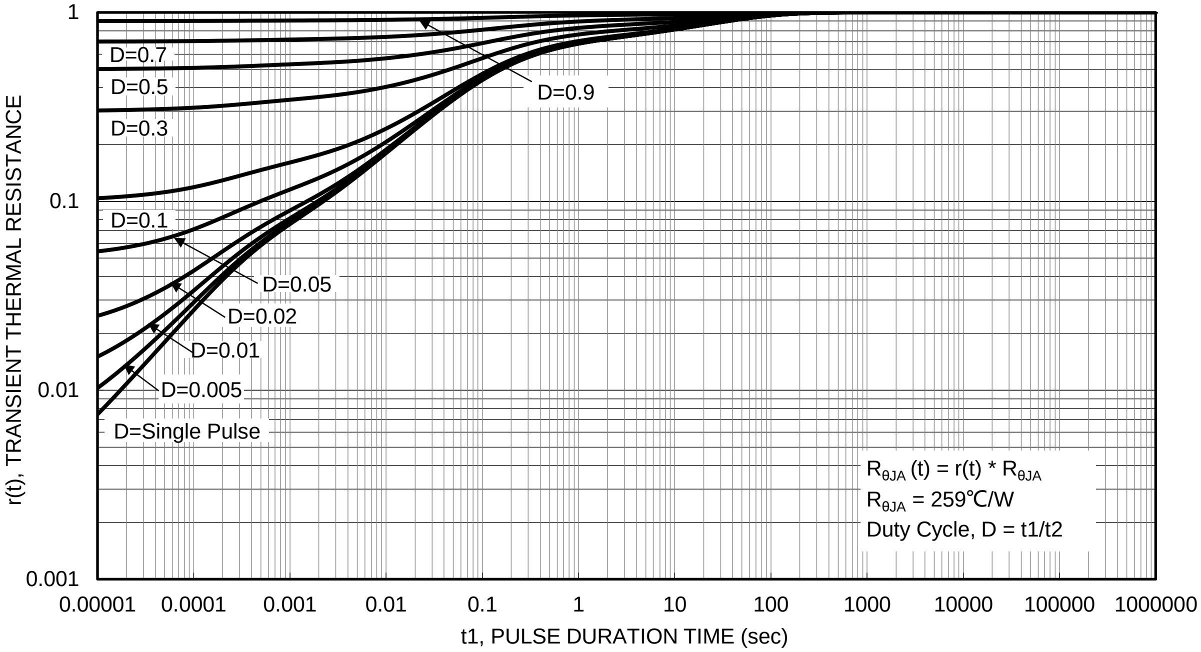
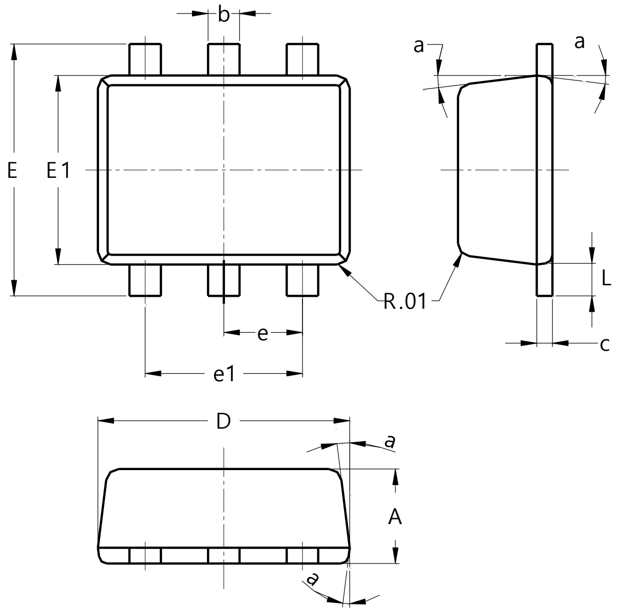


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

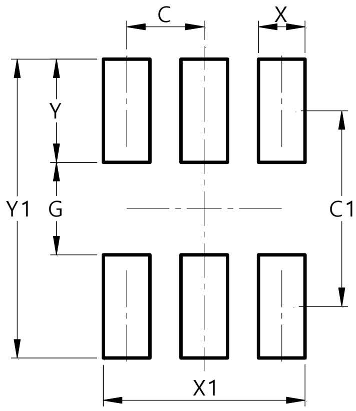
SOT563



SOT563			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.60	--
b	0.15	0.30	0.20
c	0.10	0.18	0.11
D	1.50	1.70	1.60
E	1.55	1.70	1.60
E1	1.10	1.25	1.20
e	--	--	0.50
e1	0.90	1.10	1.00
L	0.10	0.30	0.20
a	8°	9°	7°
All Dimensions in mm			

Suggested Pad Layout

SOT563



Dimensions	**Value (in mm)**
C	0.500
C1	1.270
G	0.600
X	0.300
X1	1.300
Y	0.670
Y1	1.940