优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	**$R_{DS(ON)}$ Max**	**I_D Max T_C = +25°C**
100V	32mΩ @ V_{GS} = 10V	26A
	48mΩ @ V_{GS} = 4.5V	21A

Description

This new generation MOSFET features low on-resistance and fast switching, making it ideal for high efficiency power management applications.

Applications

- Power Management Functions
- DC-DC Converters
- Backlighting

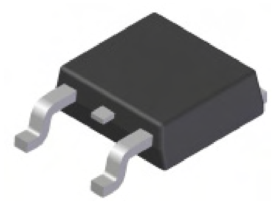
Features

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ – Minimizes Power Losses
- Low Q_g – Minimizes Switching Losses

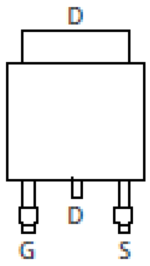
Mechanical Data

- Package: TO252
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.33 grams (Approximate)

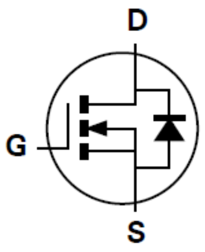
TO252 (DPAK)



Top View



Pin Out
Top View



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V	T_C = +25°C	I_D	26	A
	T_C = +70°C		21	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	104	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	26	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	104	A
Avalanche Current, L = 0.3mH		I_{AS}	13	A
Avalanche Energy, L = 0.3mH		E_{AS}	25.3	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.6	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	78	°C/W
Total Power Dissipation (Note 6)		P_D	3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction to Case		$R_{\theta JC}$	3	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	22	32	mΩ	V_{GS} = 10V, I_D = 6A
		—	34	48		V_{GS} = 4.5V, I_D = 4A
Diode Forward Voltage	V_{SD}	—	0.8	1.3	V	V_{GS} = 0V, I_S = 6A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	683	—	pF	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	165	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	6.9	—	pF	
Gate Resistance	R_g	—	1.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	6.3	—	nC	V_{DS} = 50V, I_D = 6A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	11.9	—	nC	
Gate-Source Charge	Q_{gs}	—	2.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.1	—	ns	V_{DS} = 50V, R_L = 5.85Ω V_{GS} = 10V, R_{GEN} = 3Ω
Turn-On Rise Time	t_R	—	4.5	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	12.5	—	ns	
Turn-Off Fall Time	t_F	—	9.3	—	ns	
Reverse Recovery Time	t_{RR}	—	31.5	—	ns	I_F = 6A, di/dt = 500A/µs
Reverse Recovery Charge	Q_{RR}	—	94.6	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

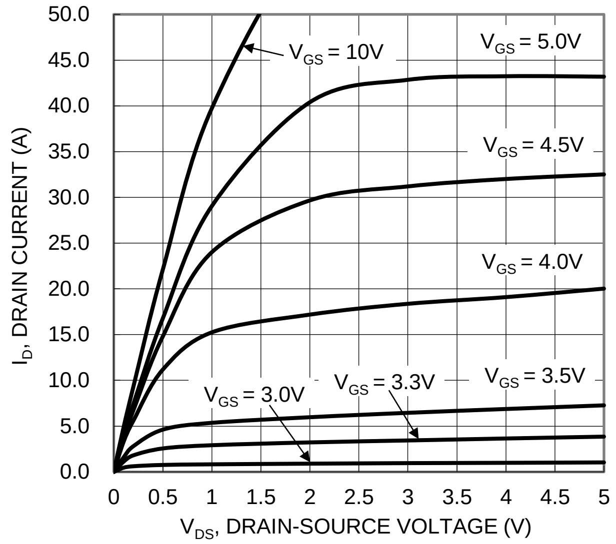


Figure 1. Typical Output Characteristic

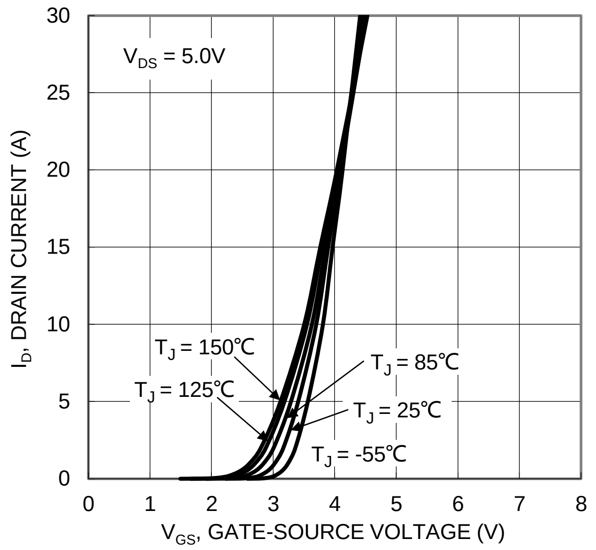


Figure 2. Typical Transfer Characteristic

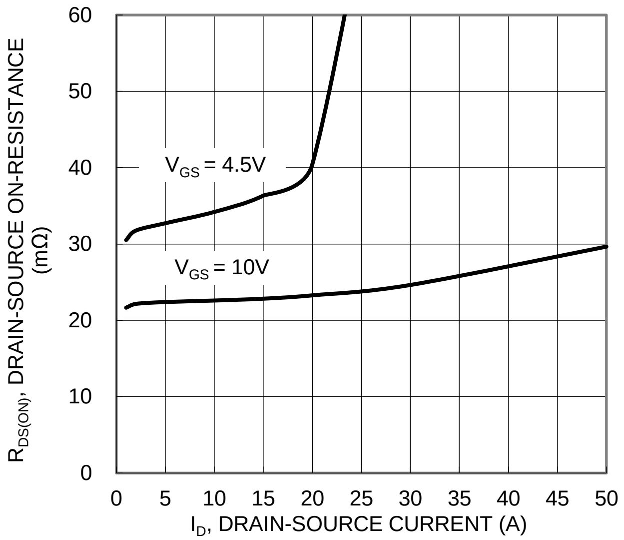


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

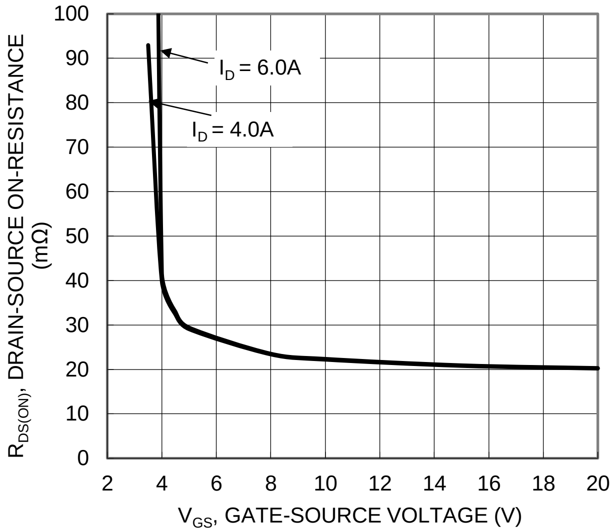


Figure 4. Typical Transfer Characteristic

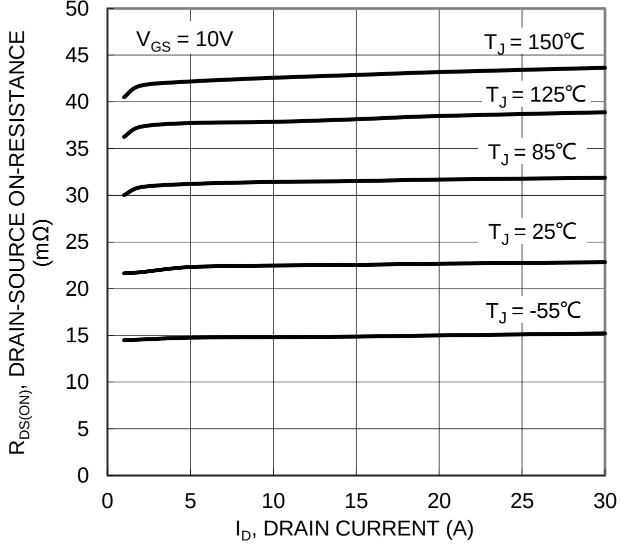


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

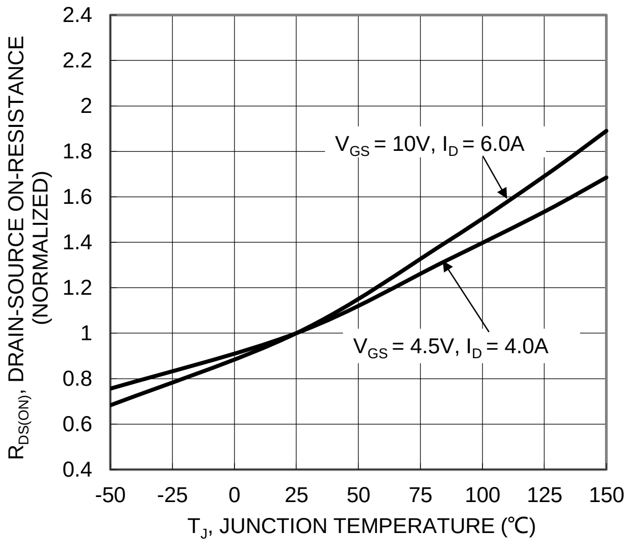


Figure 6. On-Resistance Variation with Temperature

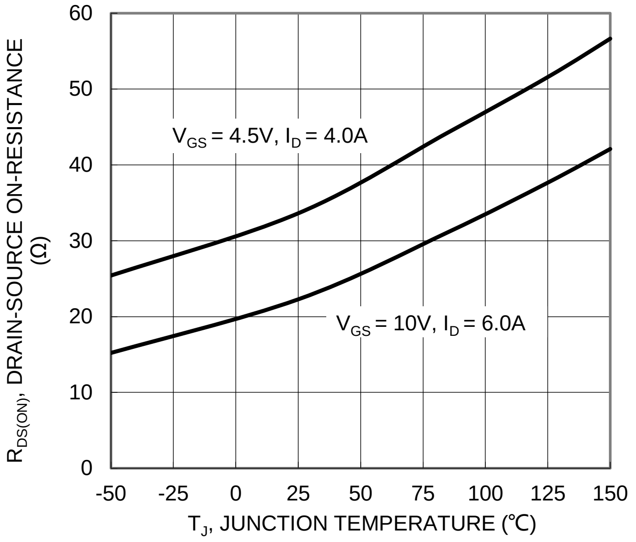


Figure 7. On-Resistance Variation with Temperature

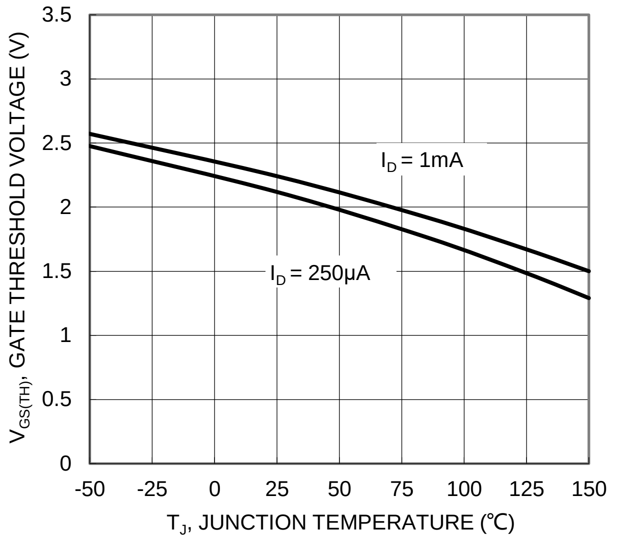


Figure 8. Gate Threshold Variation vs. Junction Temperature

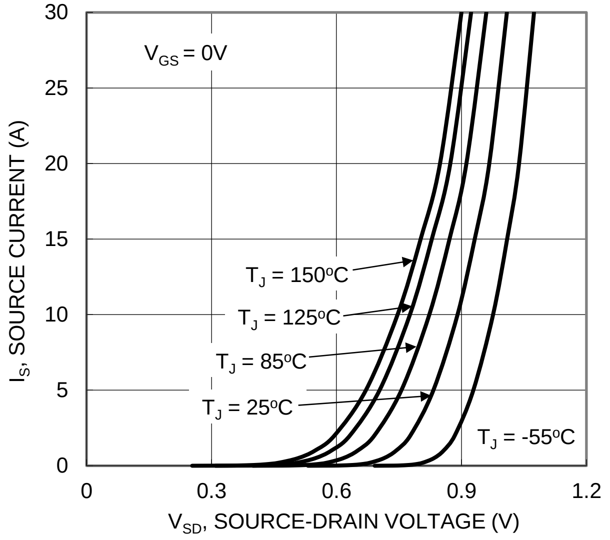


Figure 9. Diode Forward Voltage vs. Current

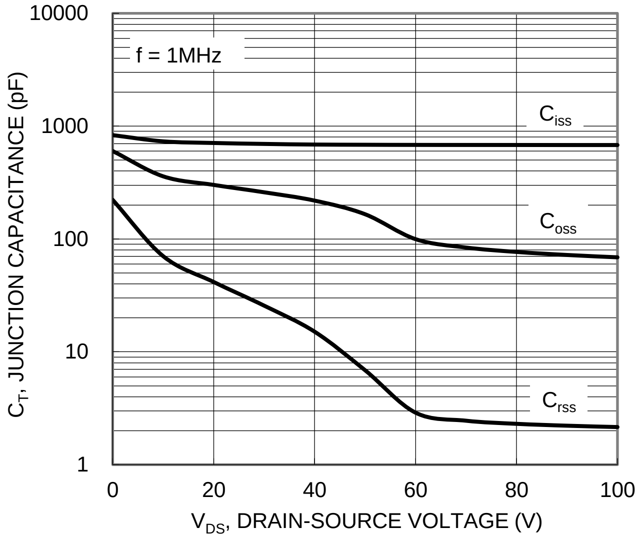


Figure 10. Typical Junction Capacitance

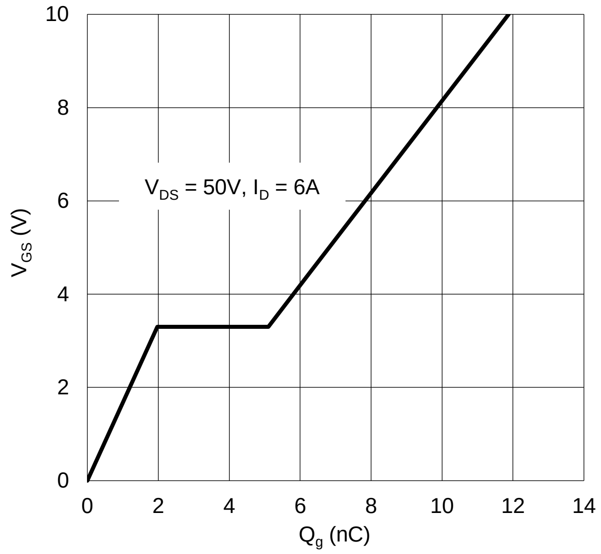


Figure 11. Gate Charge

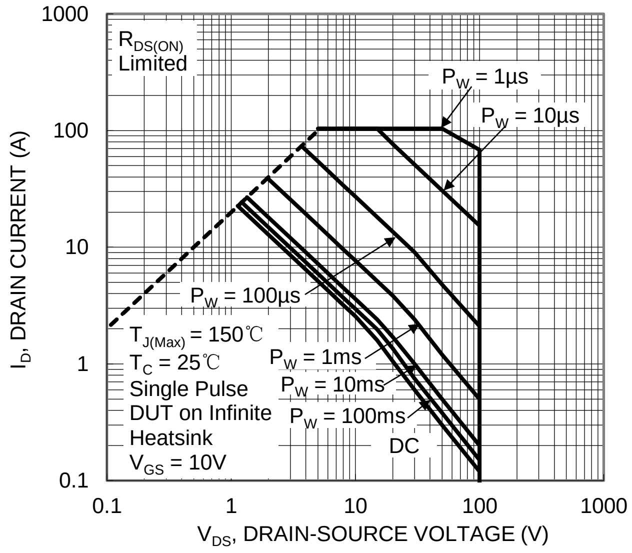


Figure 12. SOA, Safe Operation Area

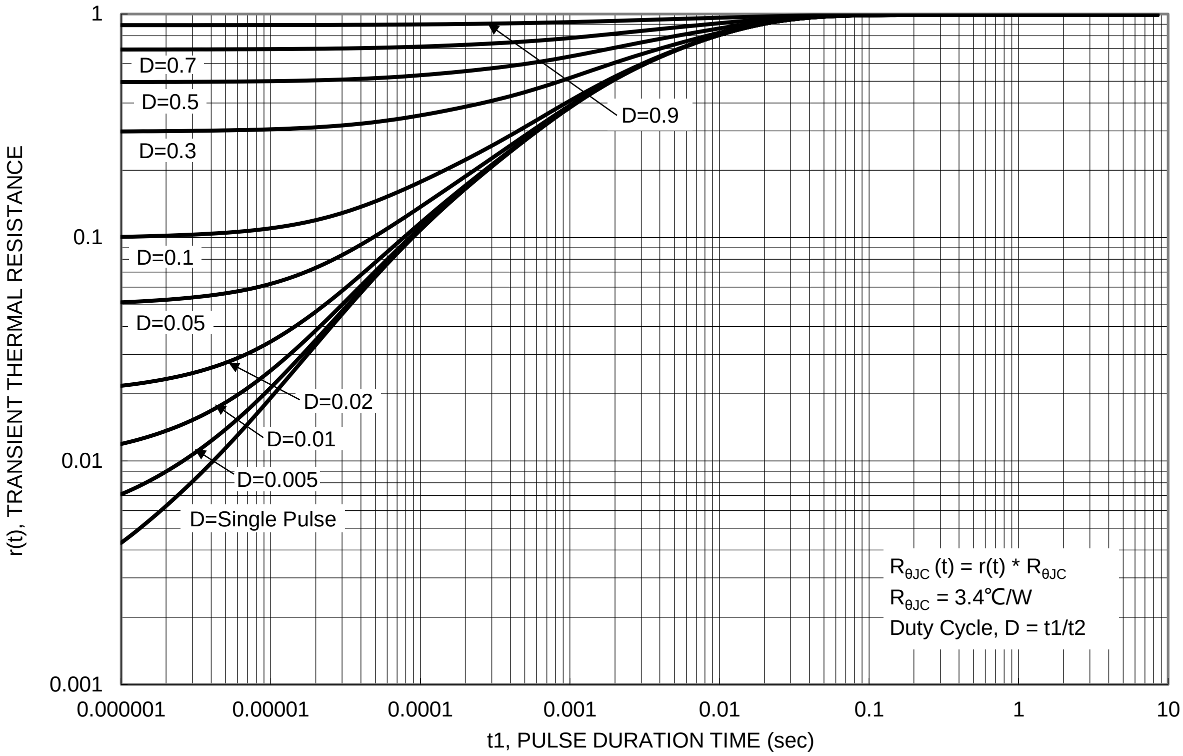
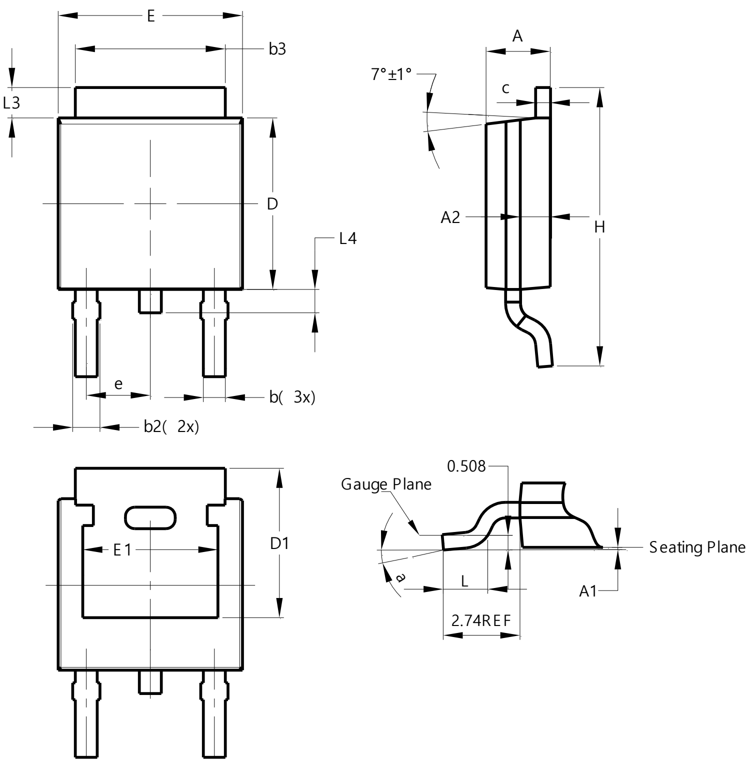


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

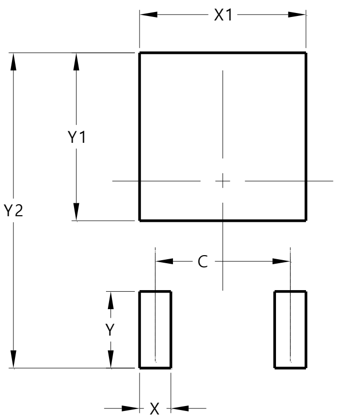
TO252 (DPAK)



TO252 (DPAK)			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700