优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D $T_C = +25°C$ (Note 5)
100V	8.8mΩ @ V_{GS} = 10V	100A
	11.5mΩ @ V_{GS} = 6V	100A

Features and Benefits

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- Fast Switching Speed

Description and Applications

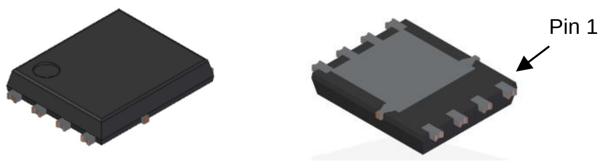
This new generation N-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switches.

- Motor controls
- DC-DC converters
- Power management

Mechanical Data

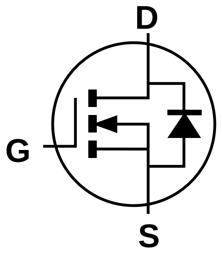
- Package: PowerDI®5060-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal: Finish – Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

PowerDI5060-8/SWP (Type UX)

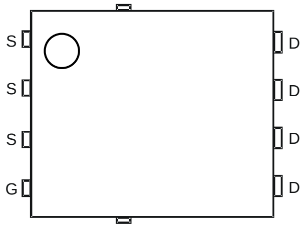


Top View

Bottom View



Internal Schematic



Top View
Pin Configuration

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	T_A = +25°C T_A = +100°C	I_D	15 11	A
Continuous Drain Current, V_{GS} = 10V (Note 7)	T_C = +25°C (Note 5) T_C = +100°C	I_D	100 87	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	250	A
Maximum Continuous Body Diode Forward Current		I_S	100	A
Avalanche Current, L = 0.3mH		I_{AS}	25	A
Avalanche Energy, L = 0.3mH		E_{AS}	93.7	mJ
Avalanche Current (Note 8), L = 3mH		I_{AS}	14.3	A
Avalanche Energy (Note 8), L = 3mH		E_{AS}	307	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	3	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	49	°C/W
Total Power Dissipation (Note 7)	T_C = +25°C	P_D	166	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	0.9	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Notes:
5. Package limited.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. Guaranteed by design. Not subject to product testing.

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	6.6	8.8	mΩ	V_{GS} = 10V, I_D = 13A
		—	8.5	11.5		V_{GS} = 6V, I_D = 13A
Diode Forward Voltage	V_{SD}	—	0.8	1.3	V	V_{GS} = 0V, I_S = 13A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	4,468	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	746	—		
Reverse Transfer Capacitance	C_{rss}	—	32	—		
Gate Resistance	R_g	—	0.91	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	56.4	—	nC	V_{DD} = 50V, I_D = 13A V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	15.4	—		
Gate-Drain Charge	Q_{gd}	—	14	—		
Turn-On Delay Time	$t_{D(ON)}$	—	18.6	—	ns	V_{DD} = 50V, V_{GS} = 10V I_D = 13A, R_g = 6Ω
Turn-On Rise Time	t_R	—	22.5	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	44.8	—		
Turn-Off Fall Time	t_F	—	29.5	—		
Reverse Recovery Time	t_{RR}	—	54.5	—	ns	I_F = 13A, dI/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	106.4	—	nC	

Notes: 8. Guaranteed by design. Not subject to product testing.
9. Short duration pulse test used to minimize self-heating effect.

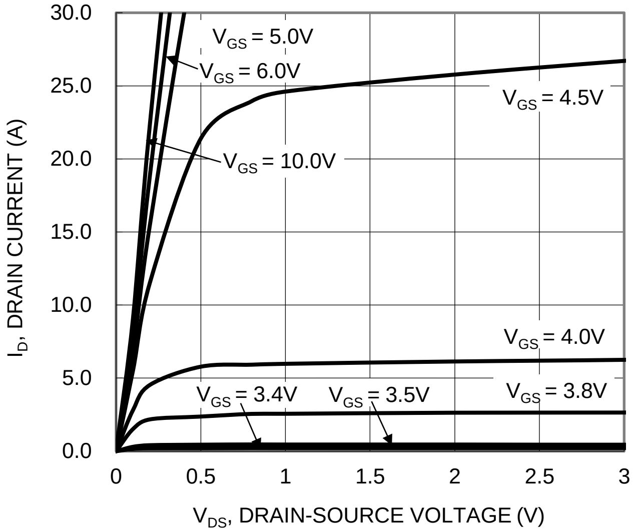


Figure 1. Typical Output Characteristic

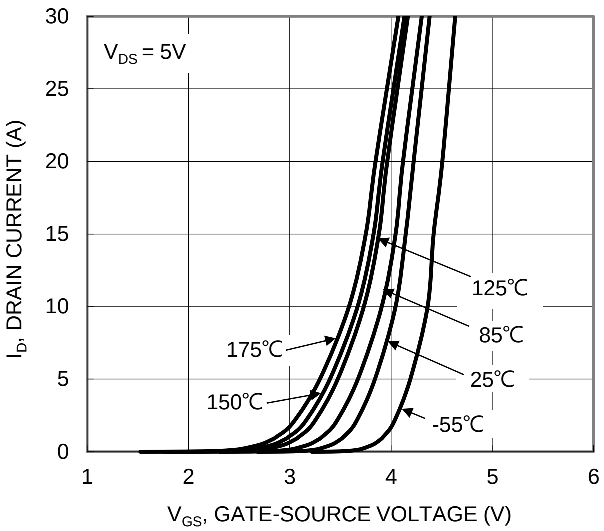


Figure 2. Typical Transfer Characteristic

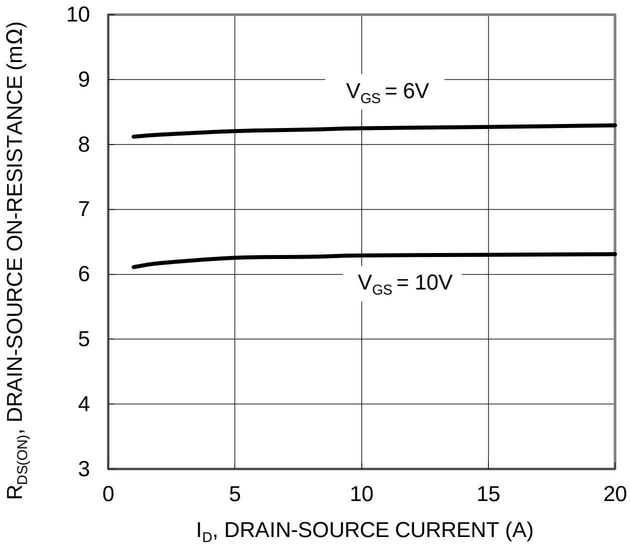


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

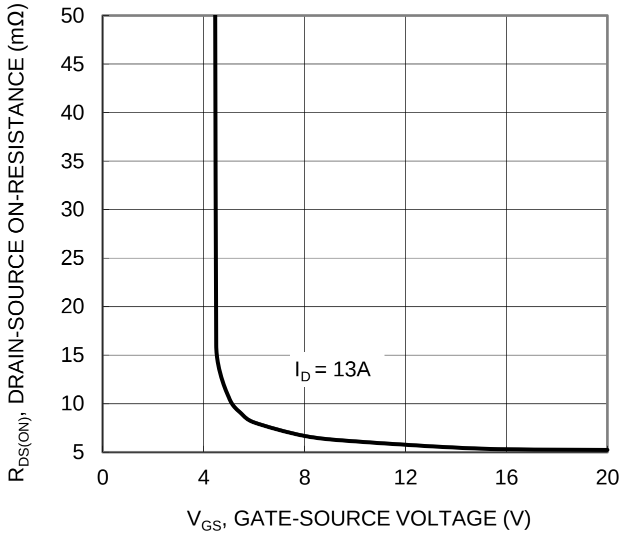


Figure 4. Typical Transfer Characteristic

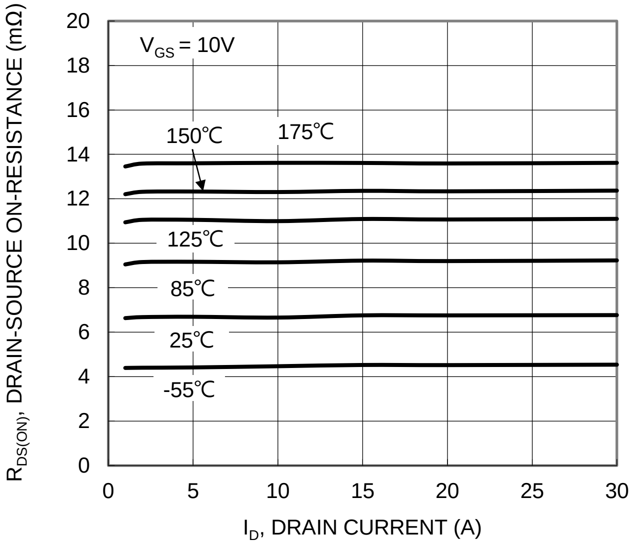


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

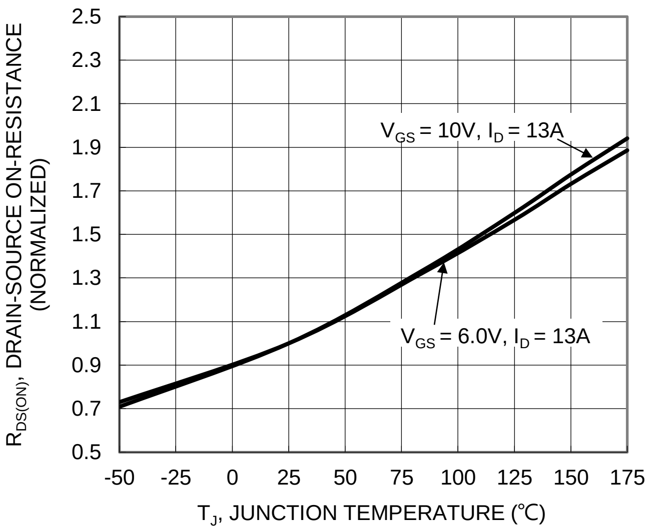


Figure 6. On-Resistance Variation with Junction Temperature

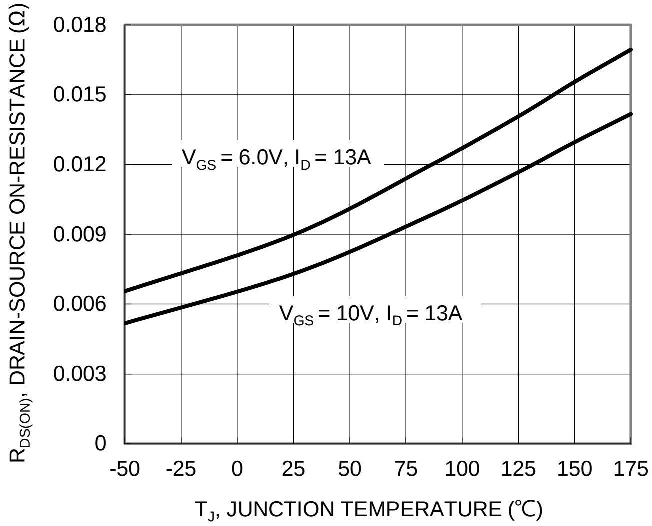


Figure 7. On-Resistance Variation with Junction Temperature

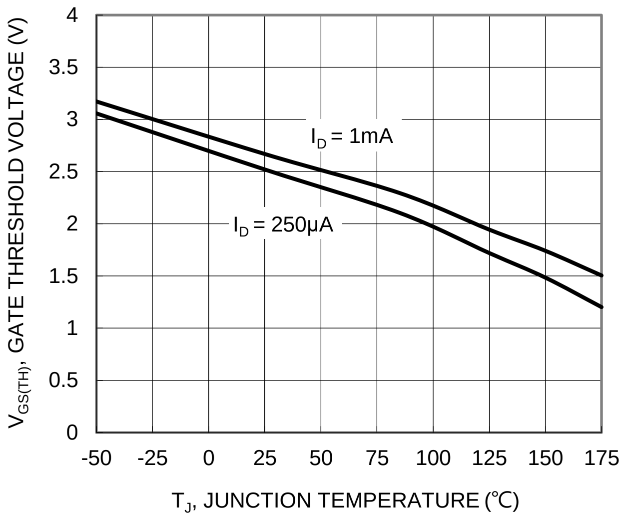


Figure 8. Gate Threshold Variation vs. Junction Temperature

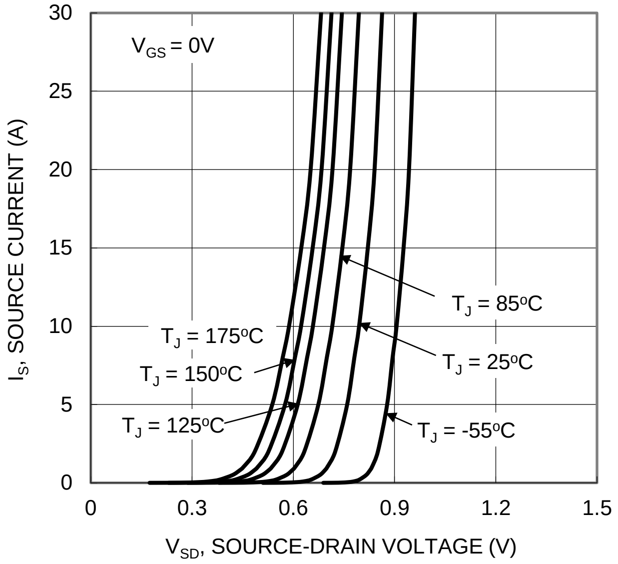


Figure 9. Diode Forward Voltage vs. Current

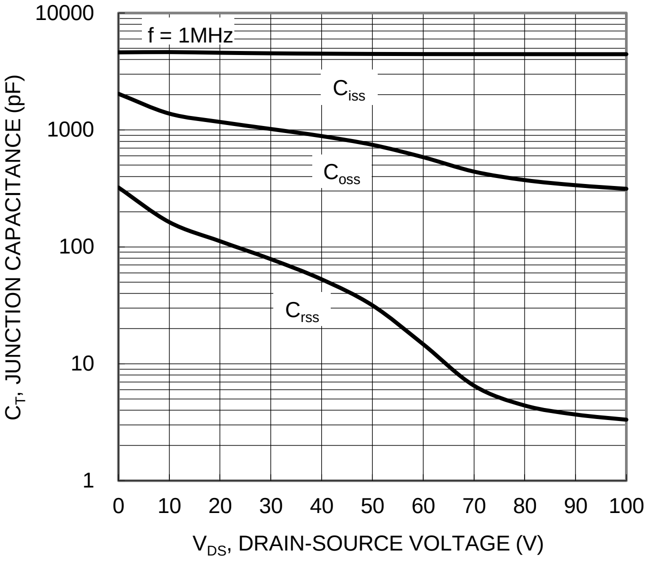


Figure 10. Typical Junction Capacitance

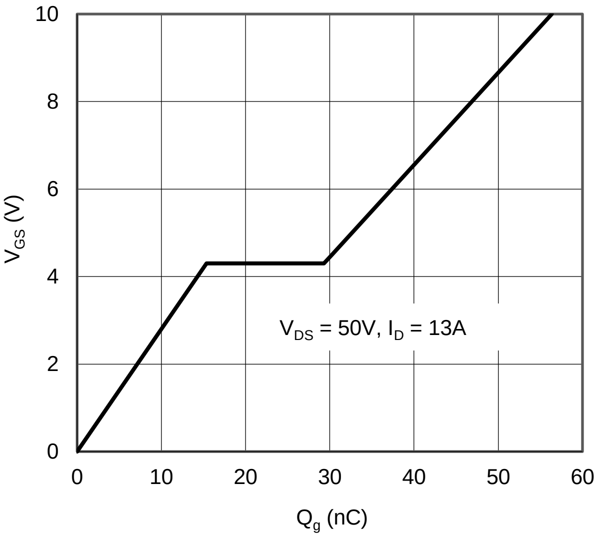


Figure 11. Gate Charge

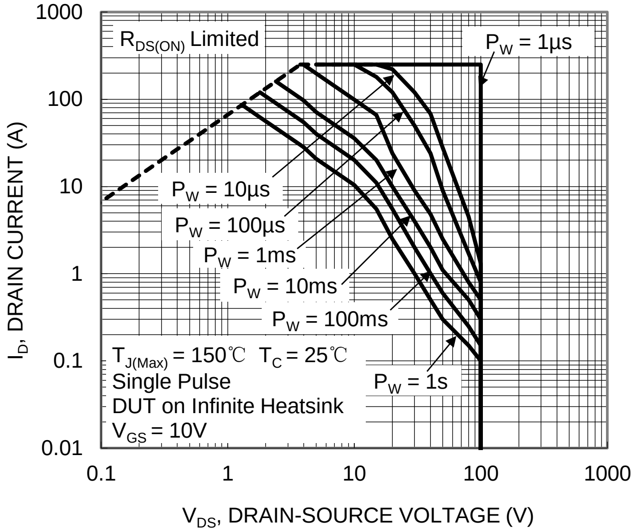


Figure 12. SOA, Safe Operation Area

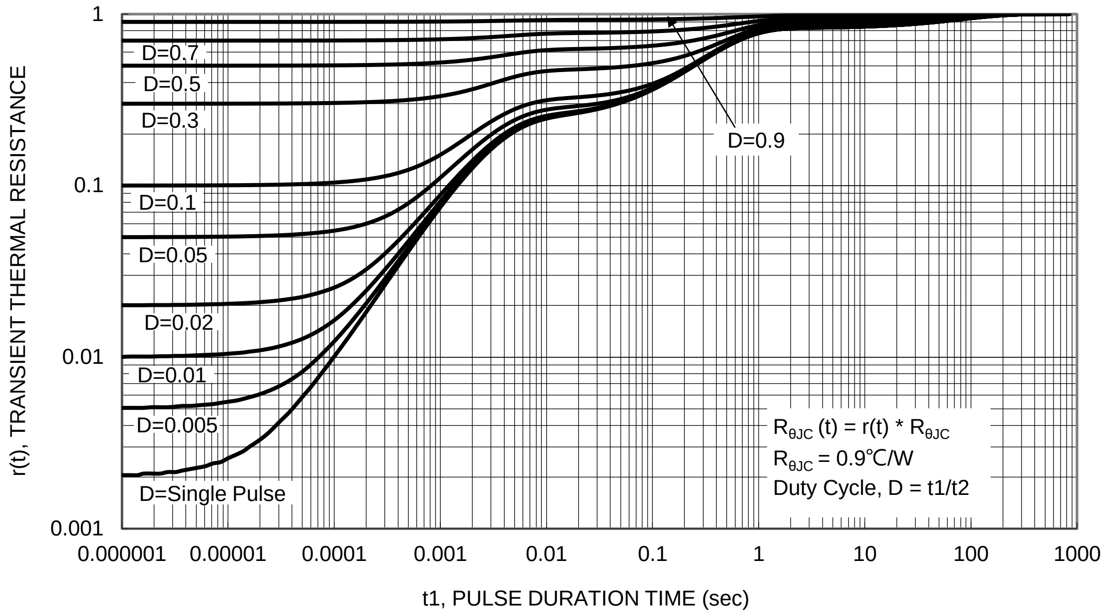
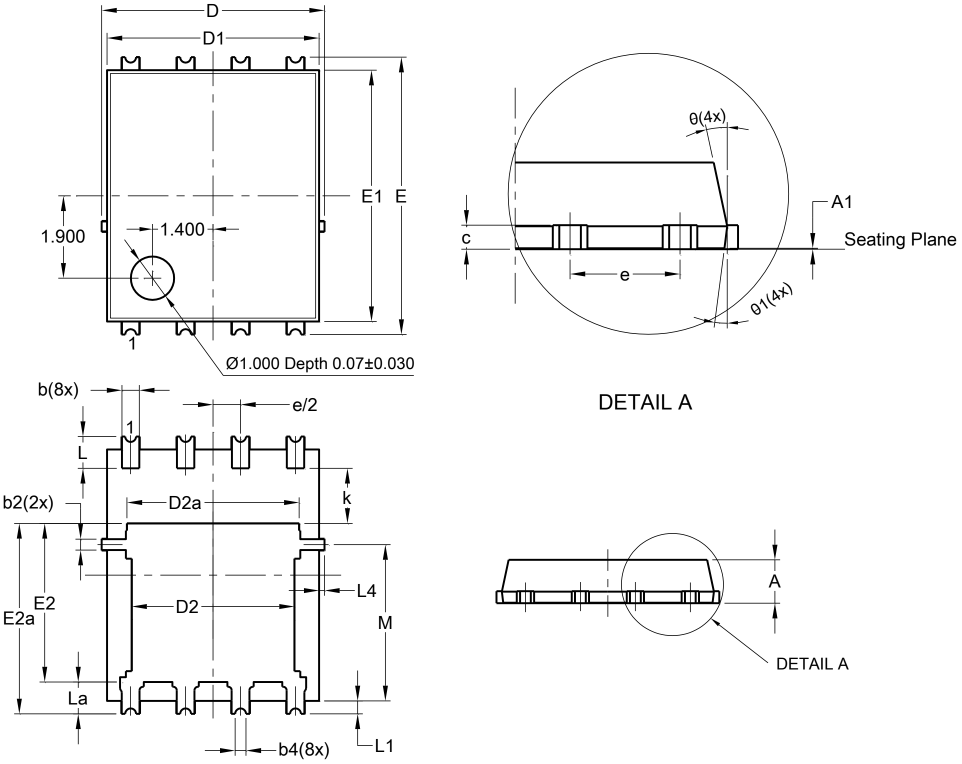


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

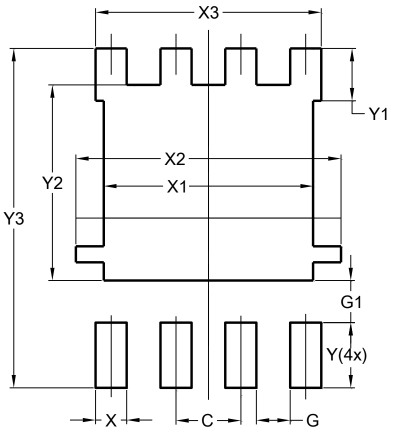
PowerDI5060-8/SWP (Type UX)



PowerDI5060-8/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

PowerDI5060-8/SWP (Type UX)



Dimensions	**Value (in mm)**
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610