



YOUSHANG SEMICONDUCTOR

**设计研发新型功率器件**

**各类小信号开关**

**中低压及高压大电流等场效应管**

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企业微信二维码



企业QQ二维码

## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$ Max	$I_D$ Max $T_C = +25^\circ C$
150V	19m $\Omega$ @ $V_{GS} = 10V$	61A
	22m $\Omega$ @ $V_{GS} = 8V$	40A

## Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize  $R_{DS(ON)}$  yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and load switch.

## Applications

- Motor Control
- DC-DC Converters
- Power Management

## Features

- Rated to  $+175^\circ C$  – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low  $R_{DS(ON)}$  – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- $<1.1$ mm Package Profile – Ideal for Thin Applications (PowerDI<sup>®</sup>)

## Mechanical Data

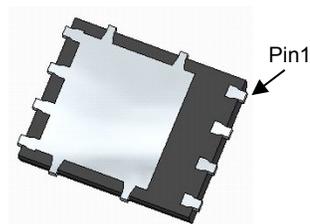
- Case: PowerDI5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish - Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.097 grams (Approximate)

Site 1:

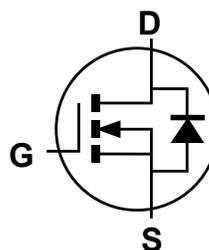
PowerDI5060-8



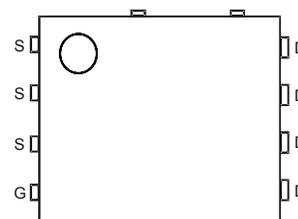
Top View



Bottom View



Internal Schematic



Top View  
Pin Configuration

Site 2:

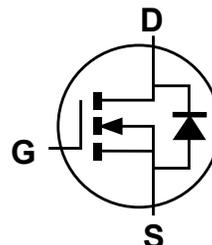
PowerDI5060-8 (SWP) (Type UX)



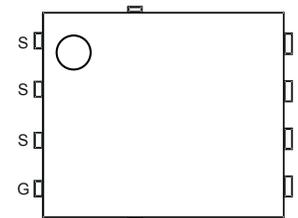
Top View



Bottom View



Internal Schematic



Top View  
Pin Configuration

### Maximum Ratings (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	150	V
Gate-Source Voltage			$V_{GSS}$	$\pm 20$	V
Continuous Drain Current $V_{GS} = 10\text{V}$ (Note 6)	Steady State	$T_A = +25^\circ\text{C}$	$I_D$	11	A
		$T_A = +100^\circ\text{C}$		7	
Continuous Drain Current $V_{GS} = 10\text{V}$ (Note 7)	Steady	$T_C = +25^\circ\text{C}$	$I_D$	61	A
	State	$T_C = +100^\circ\text{C}$		40	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	250	A
Maximum Continuous Body Diode Forward Current			$I_S$	61	A
Pulsed Body Diode Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{SM}$	250	A
Avalanche Current (Note 8), $L = 3\text{mH}$			$I_{AS}$	14.4	A
Avalanche Energy (Note 8), $L = 3\text{mH}$			$E_{AS}$	311	mJ

### Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	$P_D$	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	97	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	$P_D$	3.2	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	47	$^\circ\text{C/W}$
Total Power Dissipation (Note 7)	$T_C = +25^\circ\text{C}$	$P_D$	107	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.4	$^\circ\text{C/W}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  - Thermal resistance from junction to soldering point (on the exposed drain pad).
  - $I_{AS}$  and  $E_{AS}$  ratings are based on low frequency and duty cycles to keep  $T_J = +25^\circ\text{C}$ .

**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 9)						
Drain-Source Breakdown Voltage	$BV_{DSS}$	150	—	—	V	$V_{GS} = 0V, I_D = 10mA$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu A$	$V_{DS} = 120V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS</b> (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	14	19	m $\Omega$	$V_{GS} = 10V, I_D = 20A$
		—	16	22		$V_{GS} = 8V, I_D = 15A$
Diode Forward Voltage	$V_{SD}$	—	0.8	1.2	V	$V_{GS} = 0V, I_S = 20A$
<b>DYNAMIC CHARACTERISTICS</b> (Note 10)						
Input Capacitance	$C_{iss}$	—	2344	—	pF	$V_{DS} = 75V, V_{GS} = 0V$ $f = 1MHz$
Output Capacitance	$C_{oss}$	—	213	—		
Reverse Transfer Capacitance	$C_{rss}$	—	6.9	—		
Gate Resistance	$R_g$	—	1.8	—	$\Omega$	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge	$Q_g$	—	34	—	nC	$V_{DD} = 75V, I_D = 20A,$ $V_{GS} = 10V$
Gate-Source Charge	$Q_{gs}$	—	12	—		
Gate-Drain Charge	$Q_{gd}$	—	9	—		
Turn-On Delay Time	$t_{D(ON)}$	—	13.2	—	ns	$V_{DD} = 75V, V_{GS} = 10V,$ $I_D = 20A, R_g = 6\Omega$
Turn-On Rise Time	$t_R$	—	22.4	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	26.3	—		
Turn-Off Fall Time	$t_F$	—	16.1	—		
Reverse Recovery Time	$t_{RR}$	—	69	—	ns	$I_F = 20A, di/dt = 100A/\mu s$
Reverse Recovery Charge	$Q_{RR}$	—	196	—	nC	

Notes: 9. Short duration pulse test used to minimize self-heating effect.  
 10. Guaranteed by design. Not subject to product testing.

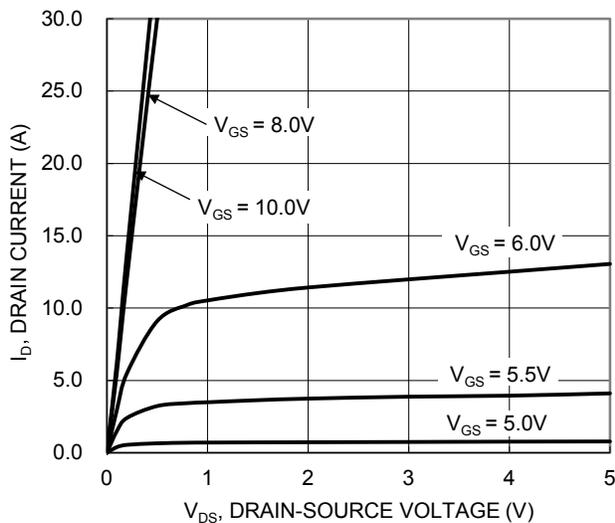


Figure 1. Typical Output Characteristic

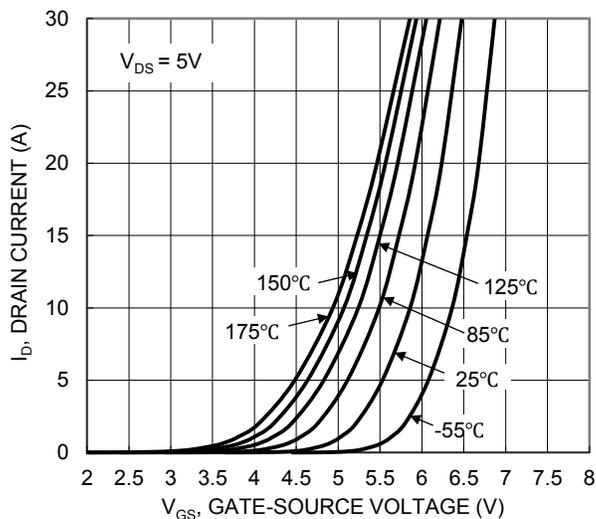


Figure 2. Typical Transfer Characteristic

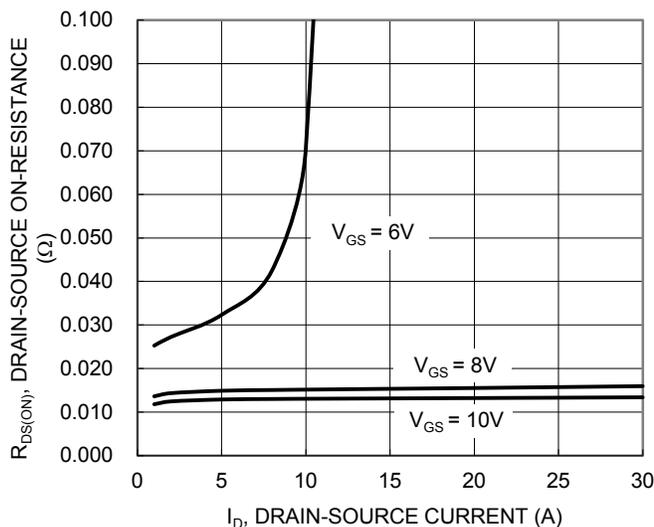


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

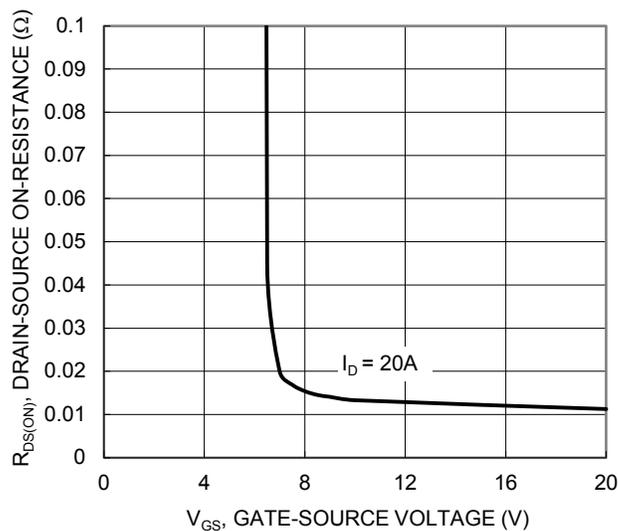


Figure 4. Typical Transfer Characteristic

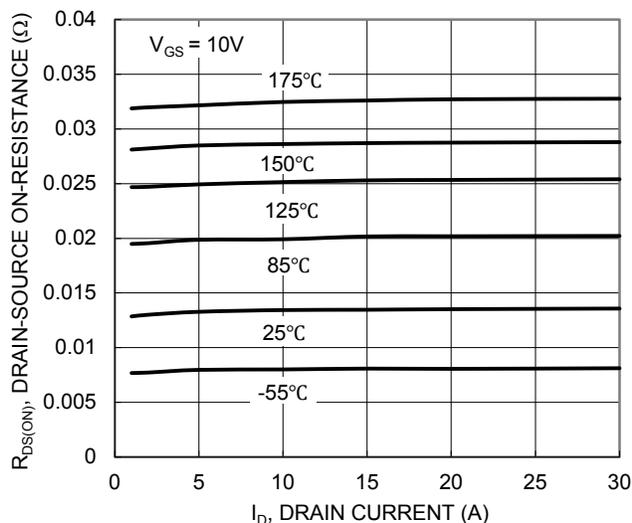


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

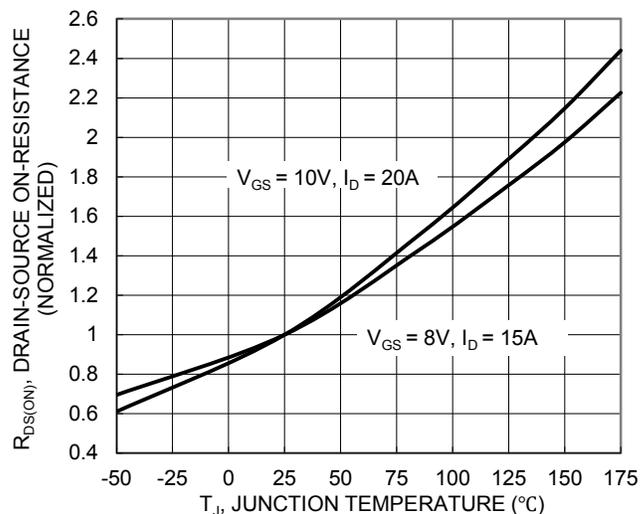


Figure 6. On-Resistance Variation with Temperature

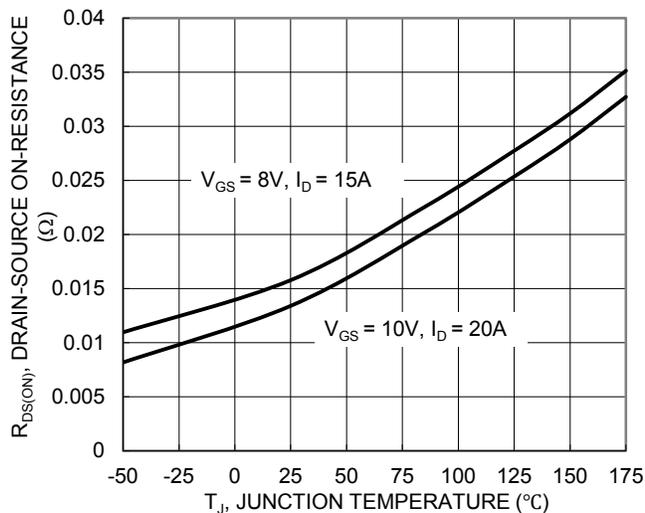


Figure 7. On-Resistance Variation with Temperature

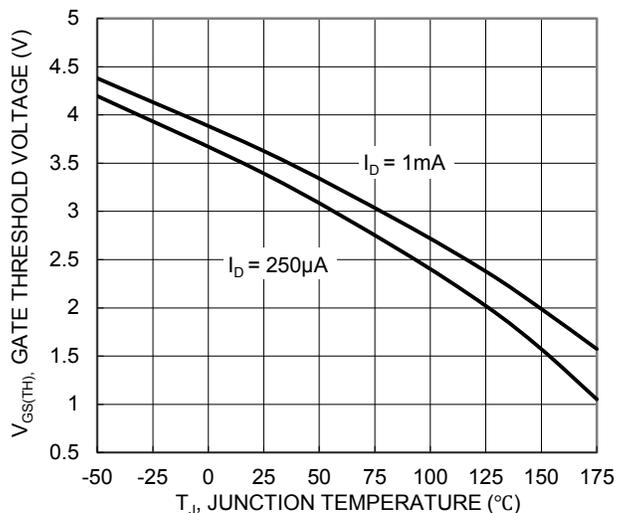


Figure 8. Gate Threshold Variation vs. Junction Temperature

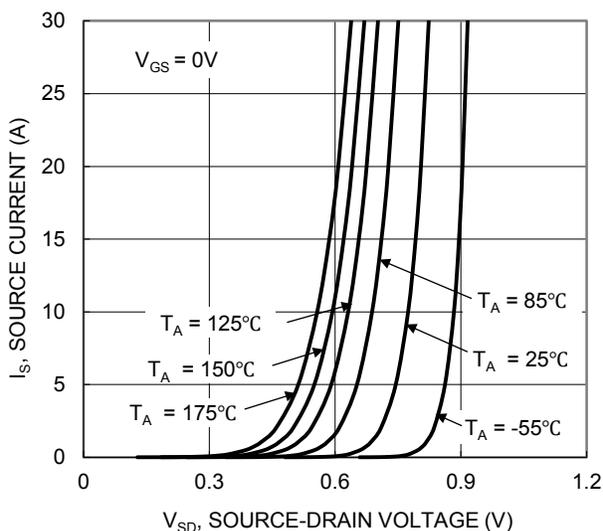


Figure 9. Diode Forward Voltage vs. Current

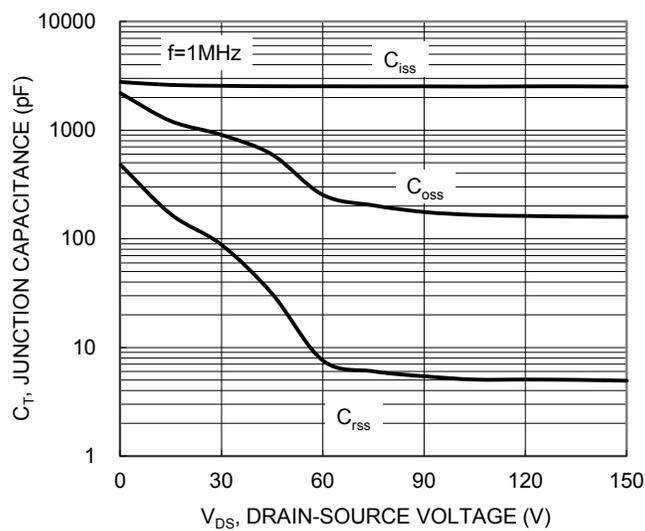


Figure 10. Typical Junction Capacitance

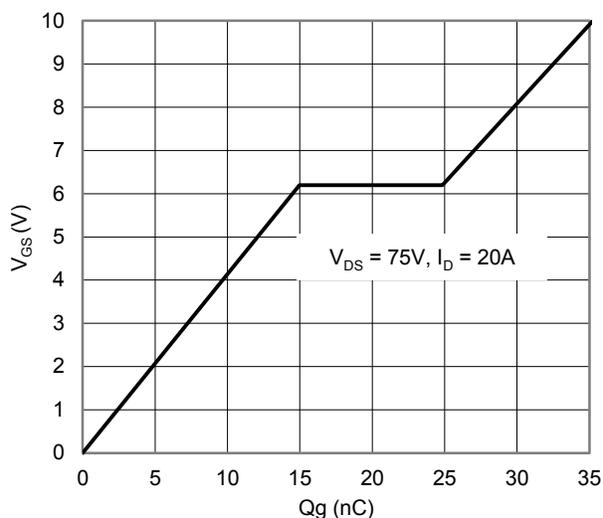


Figure 11. Gate Charge

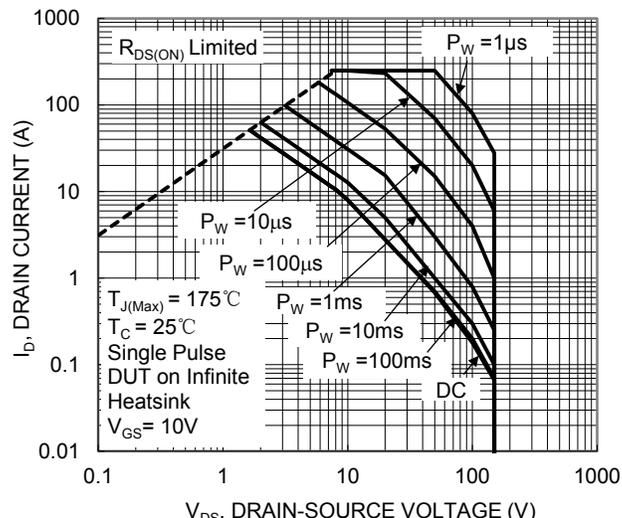


Figure 12. SOA, Safe Operation Area

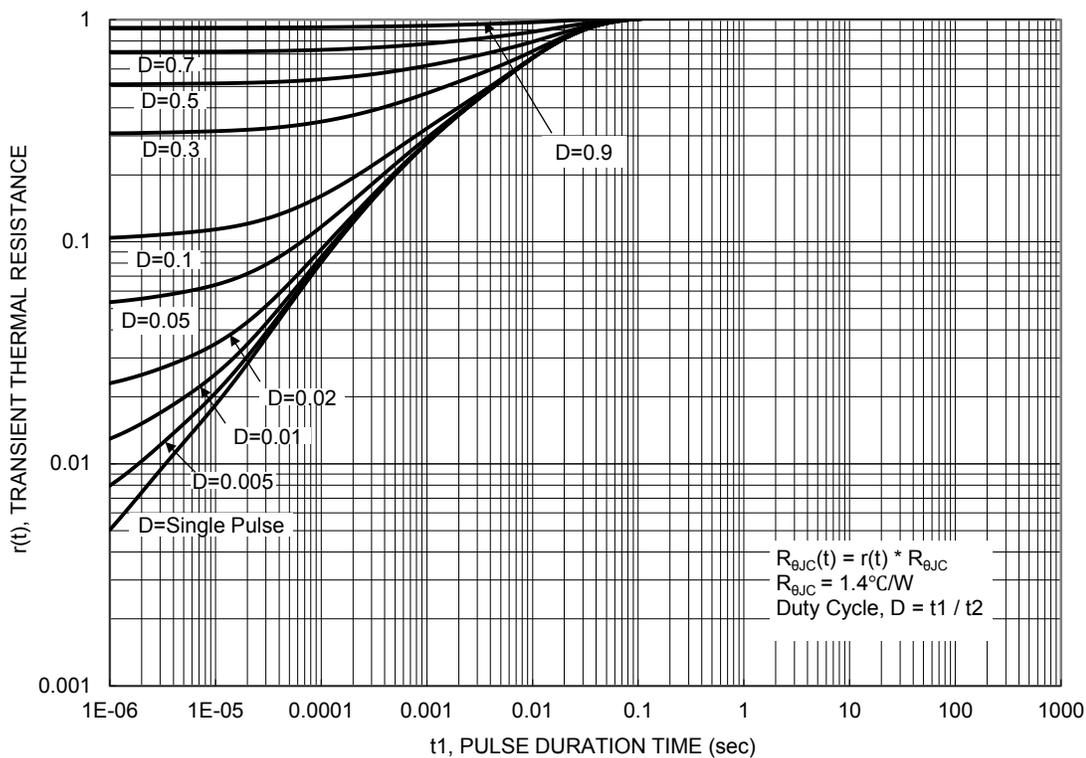
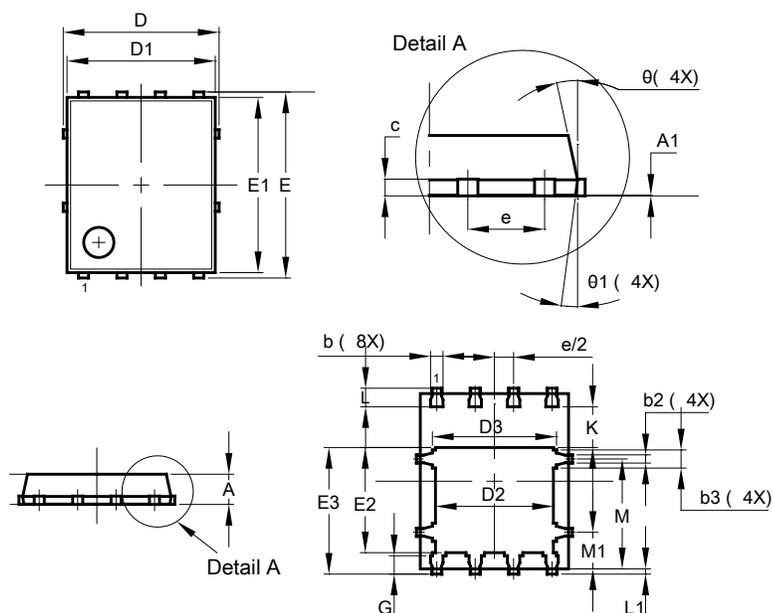


Figure 13. Transient Thermal Resistance

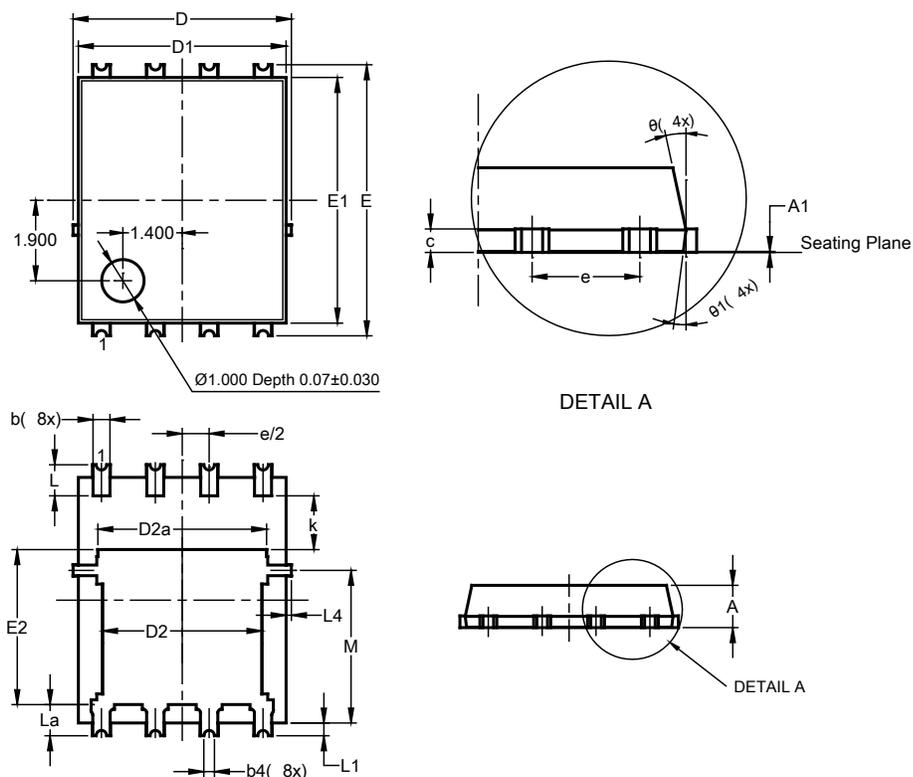
## Package Outline Dimensions

Site 1:

**PowerDI5060-8**


PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
theta	10°	12°	11°
theta1	6°	8°	7°
All Dimensions in mm			

Site 2:

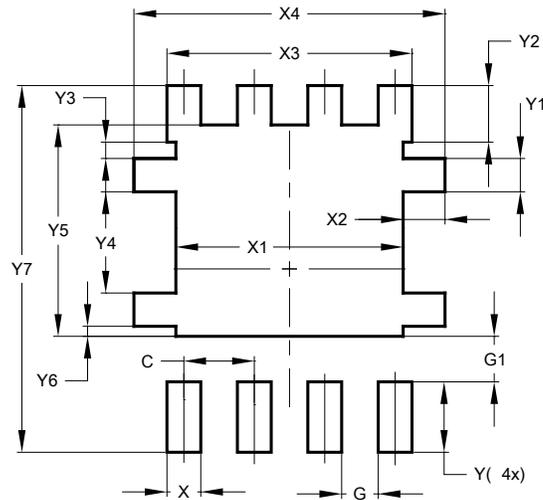
**PowerDI5060-8 (SWP) (Type UX)**


PowerDI5060-8 (SWP) (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	—
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	—	—
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
theta	10°	12°	11°
theta1	6°	8°	7°
All Dimensions in mm			

## Suggested Pad Layout

Site 1:

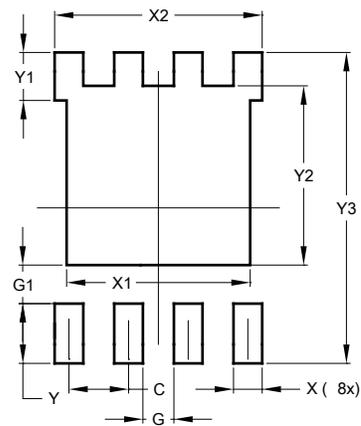
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8 (SWP) (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610