优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

企业微信二维码

企业QQ二维码

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max T_C = +25°C
30V	4mΩ@V_{GS} = 10V	75A
	7mΩ@V_{GS} = 4.5V	75A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

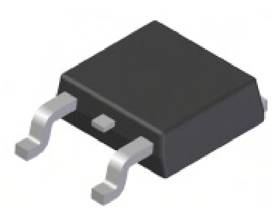
- Power Management Functions
- DC-DC Converters
- Backlighting

Features

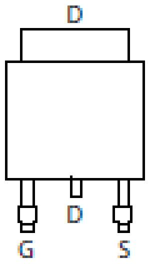
- Low On-Resistance
- Low Input Capacitance

Mechanical Data

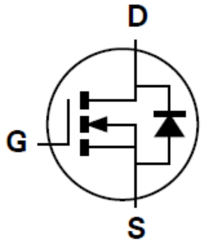
- Case:TO252
- Case Material: Molded Plastic, “Green” Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Matte Tin Finish.
  Solderable per MIL-STD-202, Method 208 ⓔ3
- Weight: 0.315 grams (Approximate)



Top View



Pin Out Top View



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	+20 -16	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_C = +25°C T_C = +70°C	I_D	75 75	A
	Steady State	T_A = +25°C T_A = +70°C	I_D	21 17	A
Pulsed Drain Current (380µs Pulse, Duty Cycle=1%)			I_{DM}	160	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	3	A
Avalanche Current (Note 7) L=5mH			I_{AS}	10.7	A
Avalanche Energy (Note 7) L=5mH			E_{AS}	287	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.9	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	80	°C/W
Total Power Dissipation (Note 6)		P_D	3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction to Case		$R_{\theta JC}$	1.4	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	10	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	100 -100	nA	V_{GS} = +20V, V_{DS} = 0V V_{GS} = -16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	-	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	3.3	4	mΩ	V_{GS} = 10V, I_D = 20A
		-	5.5	7		V_{GS} = 4.5V, I_D = 7A
Diode Forward Voltage	V_{SD}	-	0.75	1	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	-	2370	-	pF	V_{DS} =15V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	-	1360	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	240	-	pF	
Gate Resistance	R_g	-	0.6	-	Ω	V_{DS} =0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	-	20	-	nC	V_{DS} = 15V, I_D =20A
Total Gate Charge (V_{GS} = 10V)	Q_g	-	44	-	nC	
Gate-Source Charge	Q_{gs}	-	7	-	nC	
Gate-Drain Charge	Q_{gd}	-	8	-	nC	
Turn-On Delay Time	$t_{D(ON)}$	-	6.2	-	ns	V_{DD} = 15V, V_{GS} = 10V, R_L = 0.75Ω, R_G = 3Ω, I_D =20A
Turn-On Rise Time	t_R	-	4.3	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	-	21	-	ns	
Turn-Off Fall Time	t_F	-	8	-	ns	
Reverse Recovery Time	t_{RR}	-	25	-	ns	I_F =15A, di/dt=500A/µs
Reverse Recovery Charge	Q_{RR}	-	37	-	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

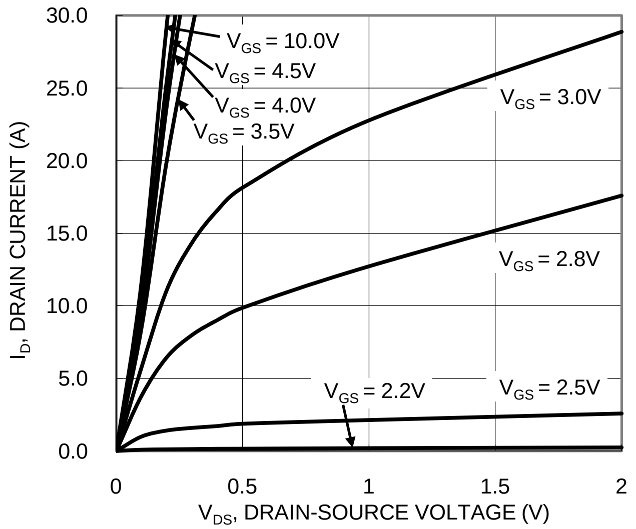


Figure 1. Typical Output Characteristic

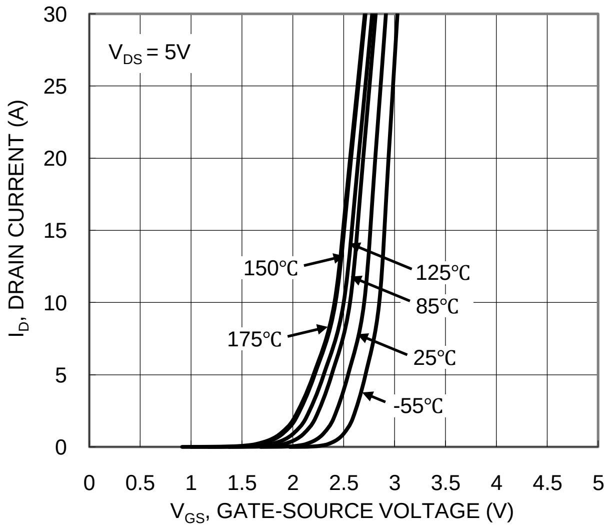


Figure 2. Typical Transfer Characteristic

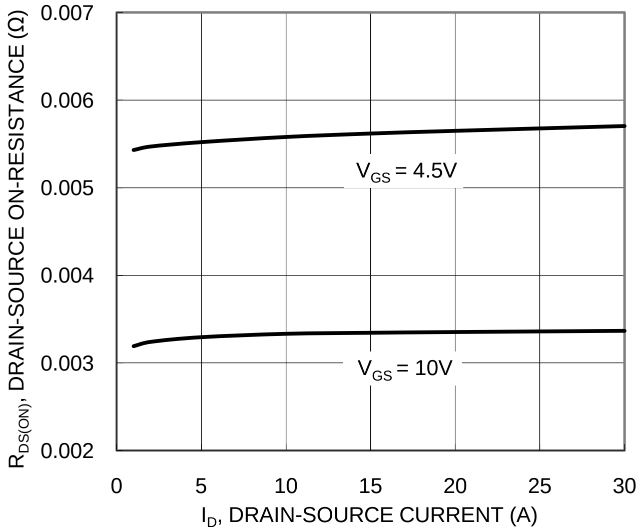


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

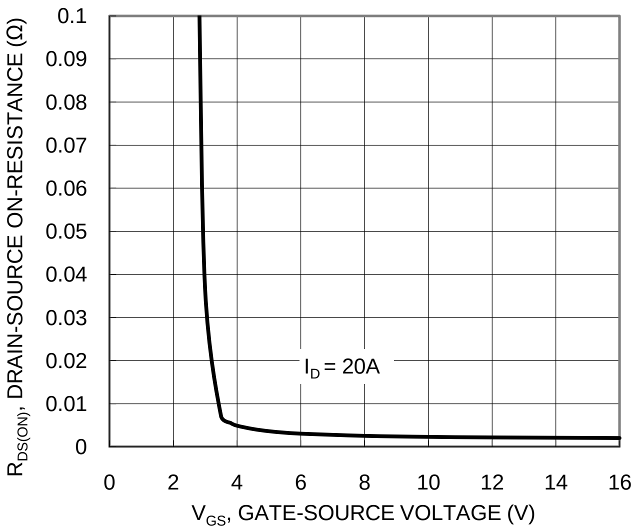


Figure 4. Typical Transfer Characteristic

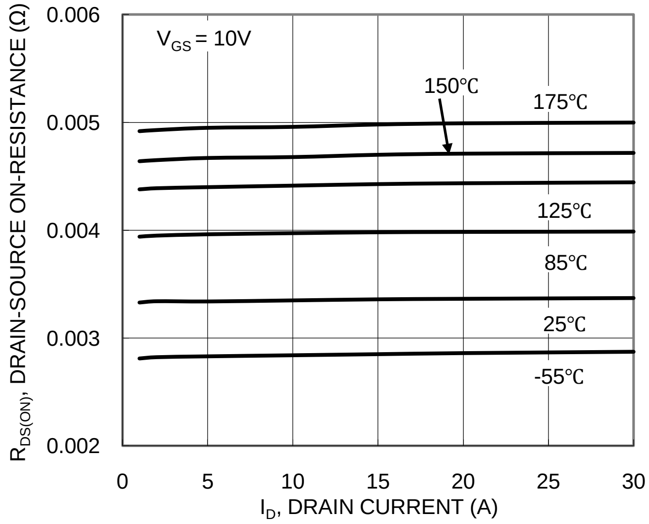


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

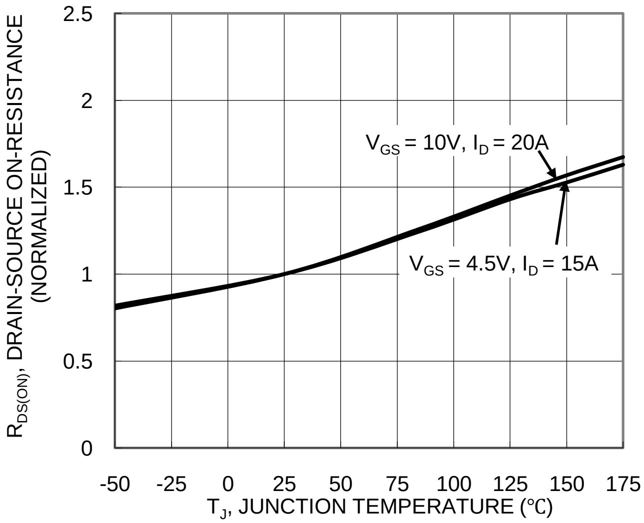


Figure 6. On-Resistance Variation with Junction Temperature

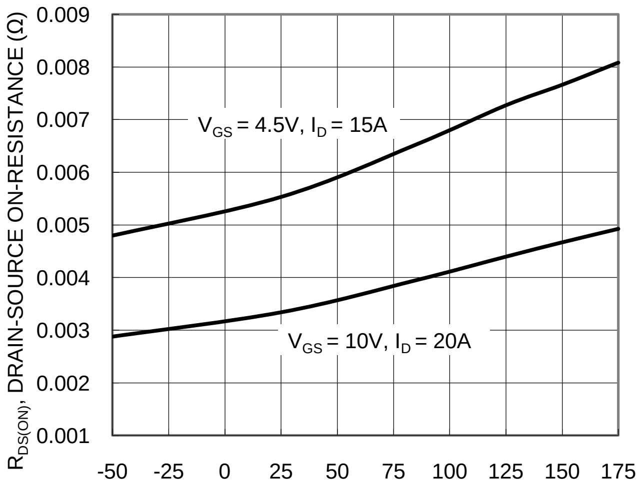


Figure 7. On-Resistance Variation with Junction Temperature

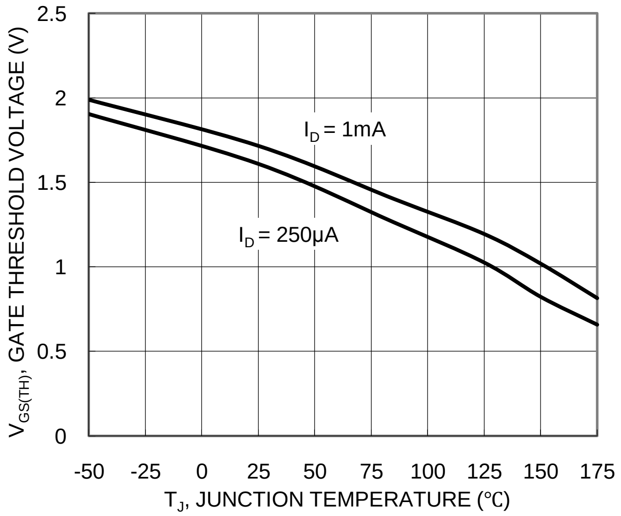


Figure 8. Gate Threshold Variation vs. Junction Temperature

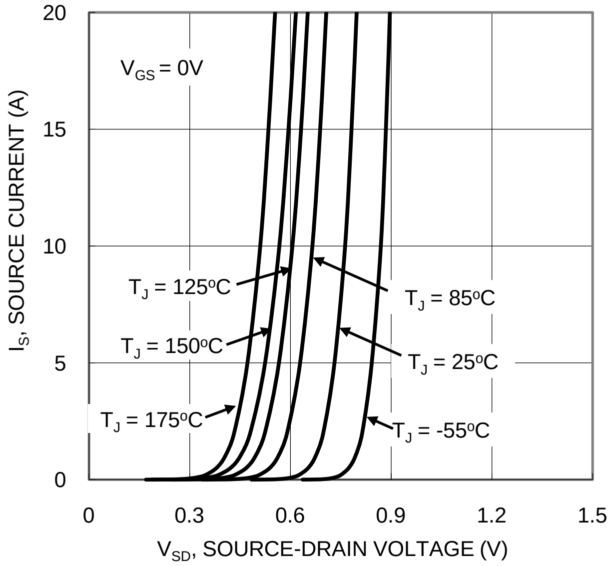


Figure 9. Diode Forward Voltage vs. Current

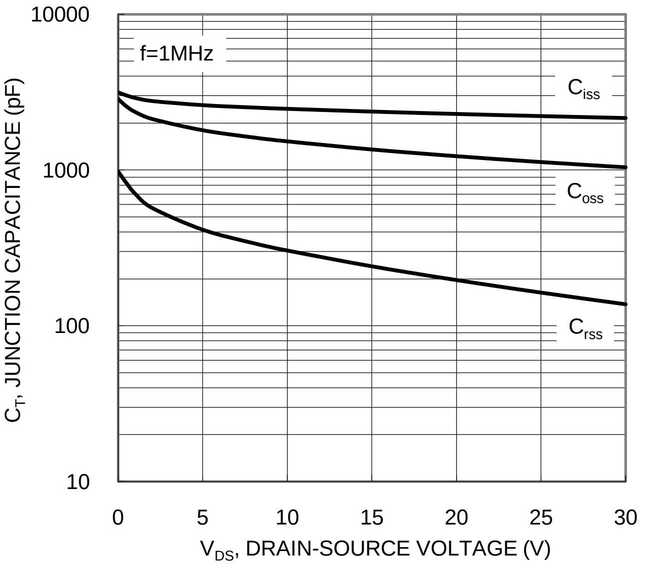


Figure 10. Typical Junction Capacitance

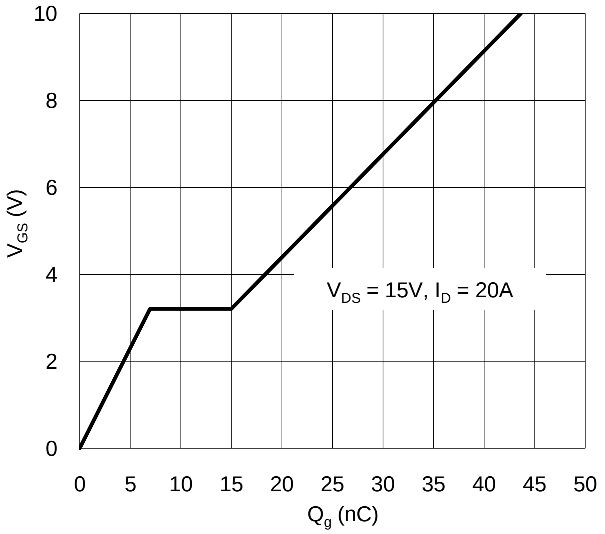


Figure 11. Gate Charge

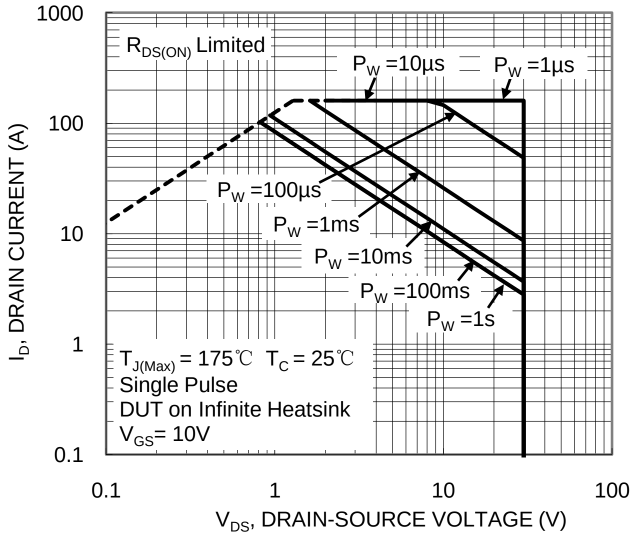


Figure 12. SOA, Safe Operation Area

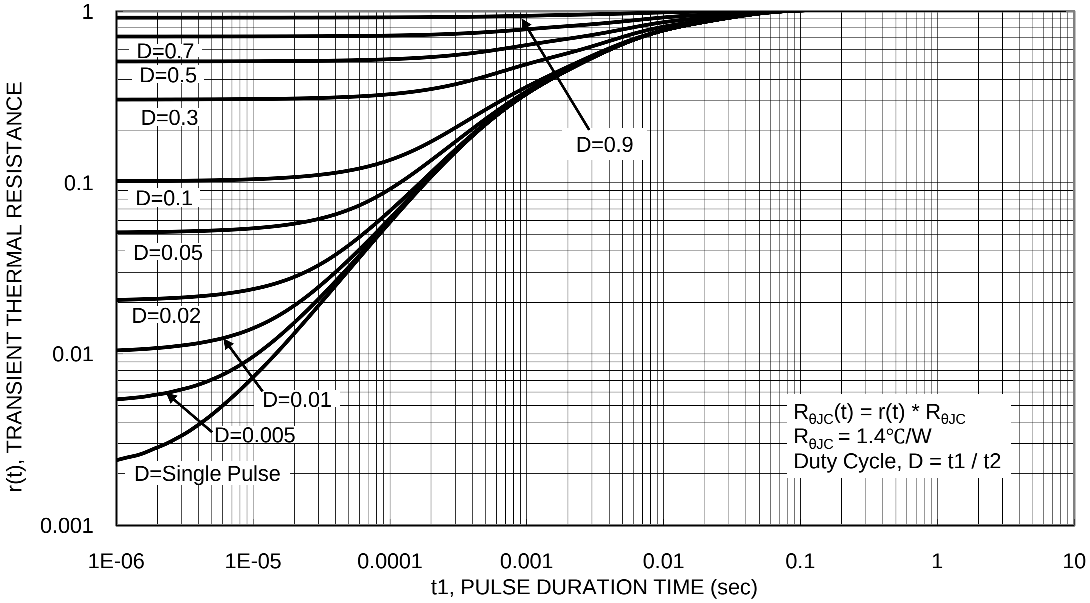
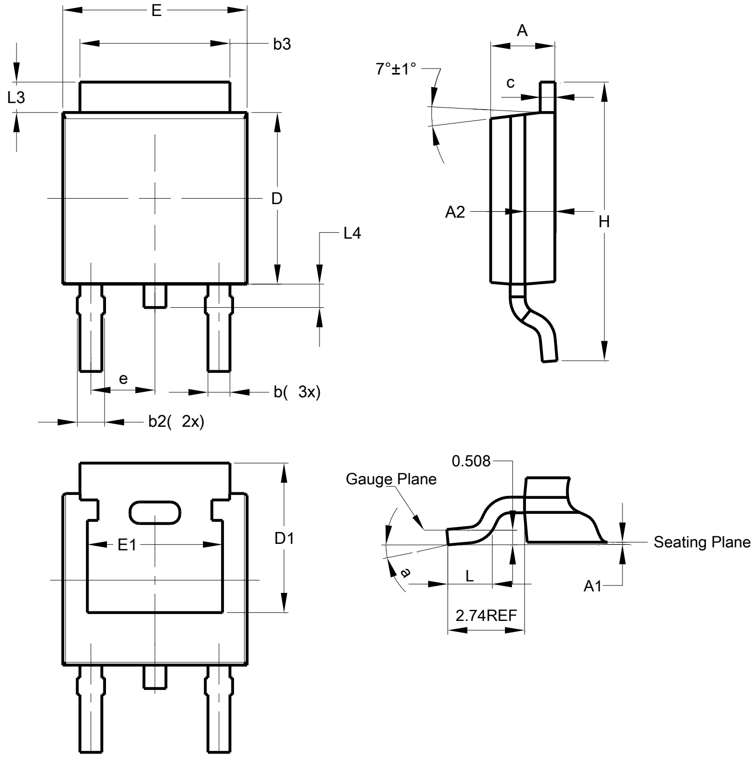


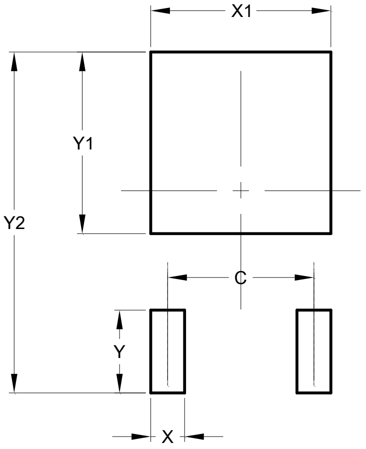
Figure 13. Transient Thermal Resistance

Package Outline Dimensions



TO252 (DPAK)			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700