



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



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Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _C = +25°C (Note 7)
40V	3.3mΩ @ V _{GS} = 10V	100A
	5.0mΩ @ V _{GS} = 5V	95A

Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize R_{DS(ON)} yet maintain superior switching performance.

Applications

- BLDC motors
- DC-DC converters
- Load switches

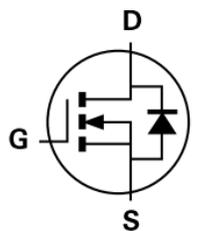
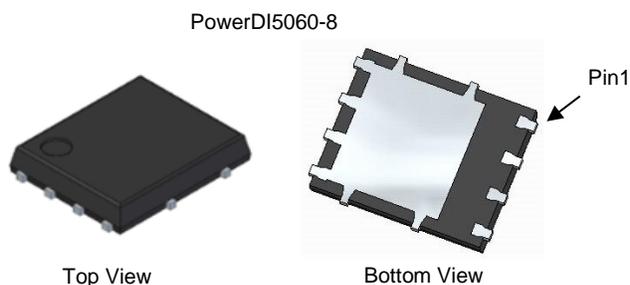
Features

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable And Robust End Application
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed

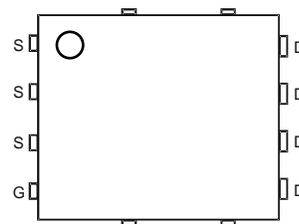
Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.097 grams (Approximate)

Site1:

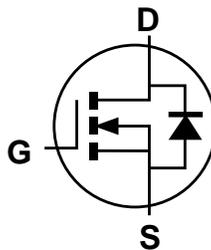
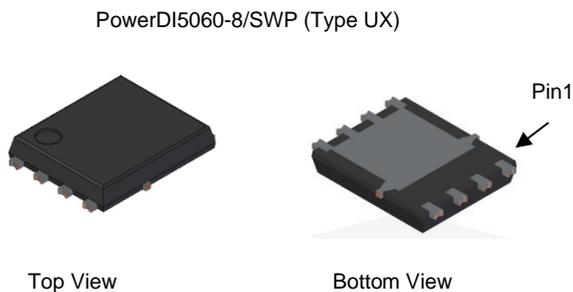


Internal Schematic

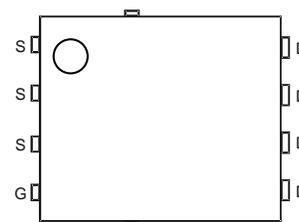


Top View
Pin Configuration

Site 2:



Internal Schematic



Top View
Pin Configuration

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 5)	I_D	$T_A = +25^\circ\text{C}$	22
		$T_A = +100^\circ\text{C}$	15.5
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6) (Note 7)	I_D	$T_C = +25^\circ\text{C}$	100
		$T_C = +100^\circ\text{C}$	82
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	350	A
Maximum Continuous Body Diode Forward Current (Note 6)	I_S	69	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)	I_{SM}	350	A
Avalanche Current, $L = 1\text{mH}$	I_{AS}	13.2	A
Avalanche Energy, $L = 1\text{mH}$	E_{AS}	87	mJ

Thermal Characteristics

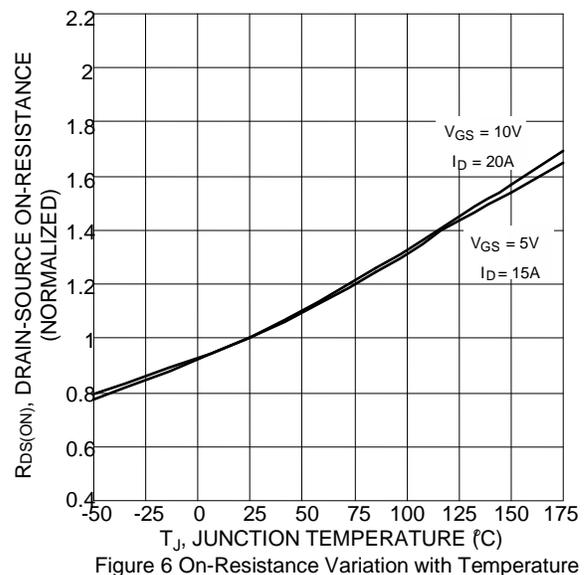
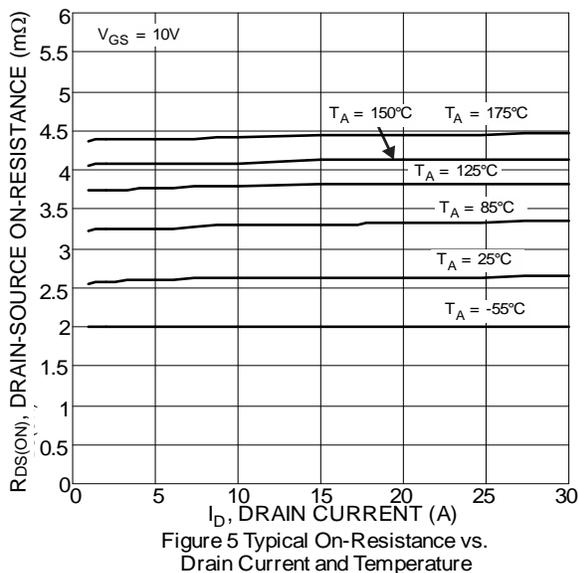
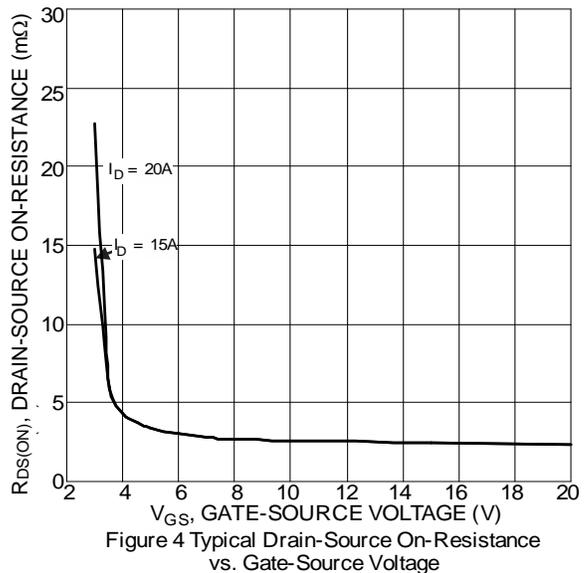
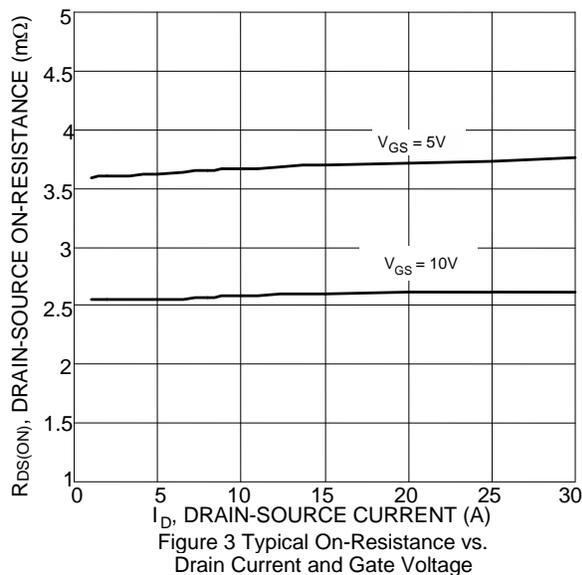
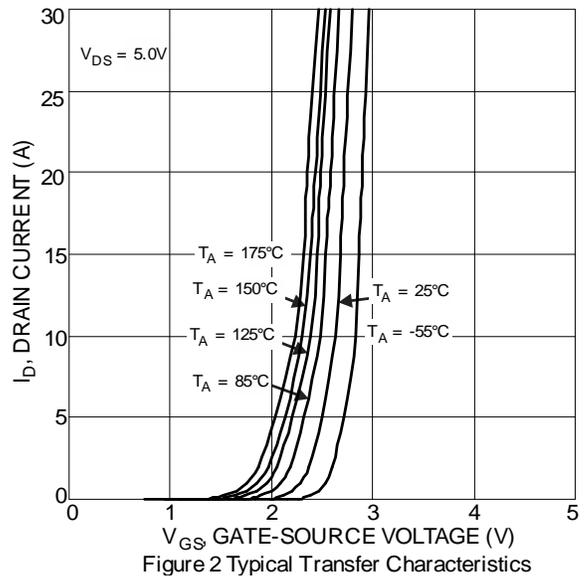
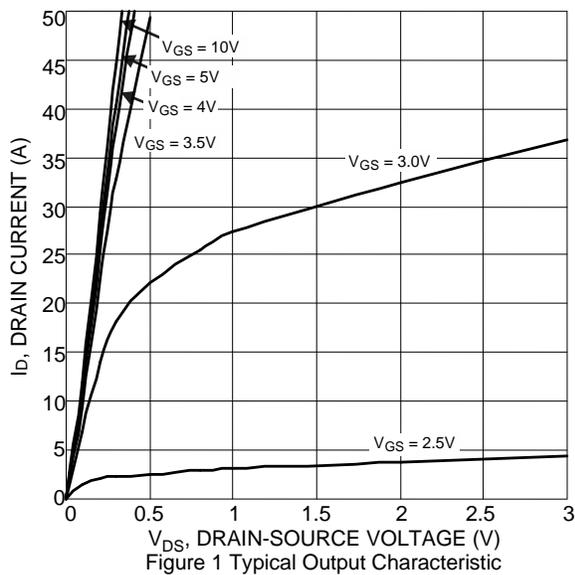
Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.7	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	55	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 6)	P_D	83	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	1.8	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
 6. Thermal resistance from junction to soldering point (on the exposed drain pad).
 7. Package limit.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 32V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	1	—	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	2.7	3.3	mΩ	V _{GS} = 10V, I _D = 20A
		—	3.6	5.0		V _{GS} = 5V, I _D = 15A
Diode Forward Voltage	V _{SD}	—	—	1.2	V	V _{GS} = 0V, I _S = 20A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{ISS}	—	2,693	—	pF	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{OSS}	—	1,172	—		
Reverse Transfer Capacitance	C _{RSS}	—	52	—		
Gate Resistance	R _G	—	2.54	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 10V)	Q _G	—	38.5	—	nC	V _{DS} = 20V, I _D = 20A
Total Gate Charge (V _{GS} = 4.5V)	Q _G	—	17.6	—		
Gate-Source Charge	Q _{GS}	—	6.9	—		
Gate-Drain Charge	Q _{GD}	—	6.9	—		
Turn-On Delay Time	t _{D(ON)}	—	5.2	—	ns	V _{DD} = 20V, V _{GS} = 10V, I _D = 20A, R _G = 3Ω
Turn-On Rise Time	t _R	—	5.7	—		
Turn-Off Delay Time	t _{D(OFF)}	—	23.5	—		
Turn-Off Fall Time	t _F	—	11	—		
Body Diode Reverse Recovery Time	t _{RR}	—	35.4	—	ns	I _F = 20A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{RR}	—	32.9	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.



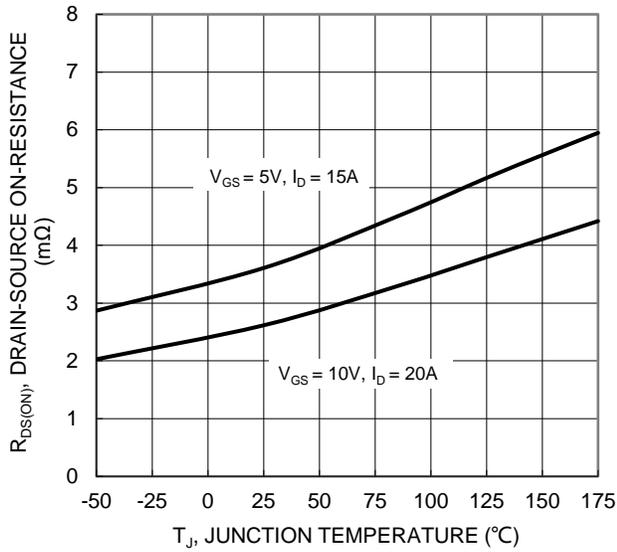


Figure 7. On-Resistance Variation with Temperature

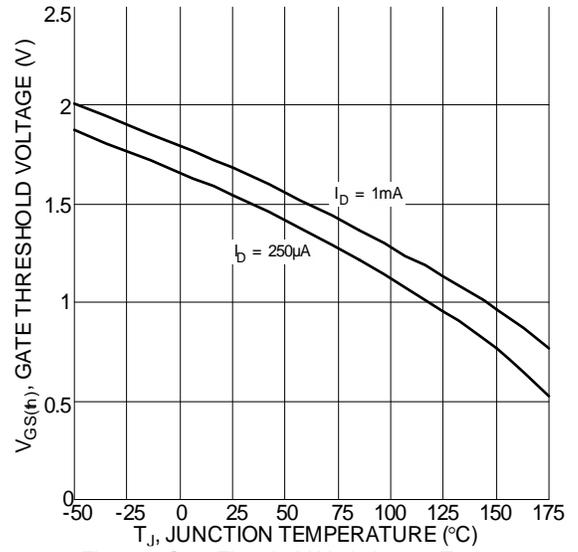


Figure 8 Gate Threshold Variation vs. Temperature

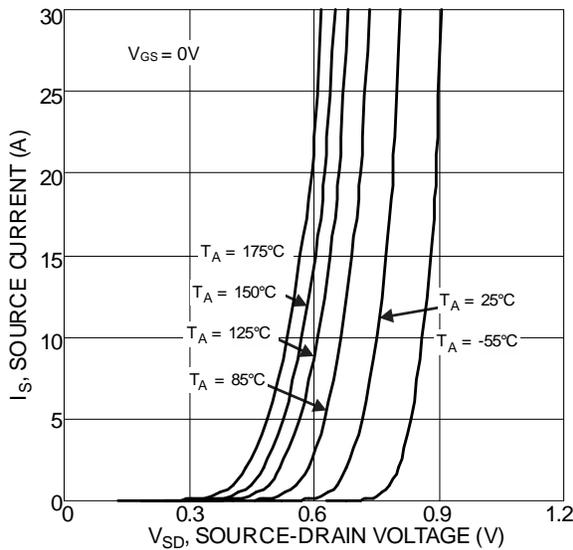


Figure 9 Diode Forward Voltage vs. Current

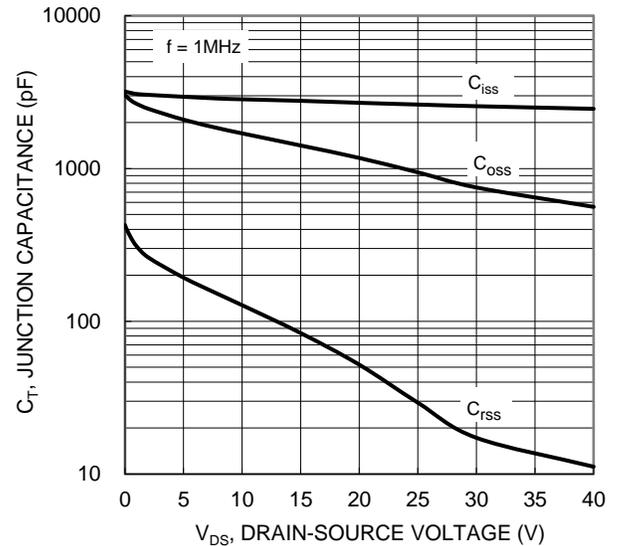


Figure 10. Typical Junction Capacitance

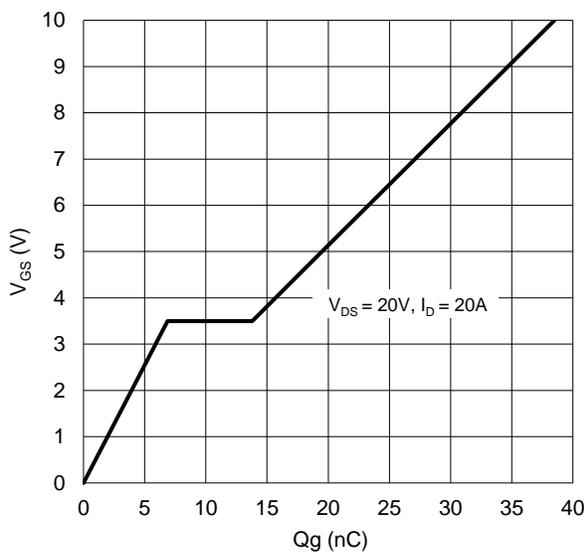


Figure 11. Gate Charge

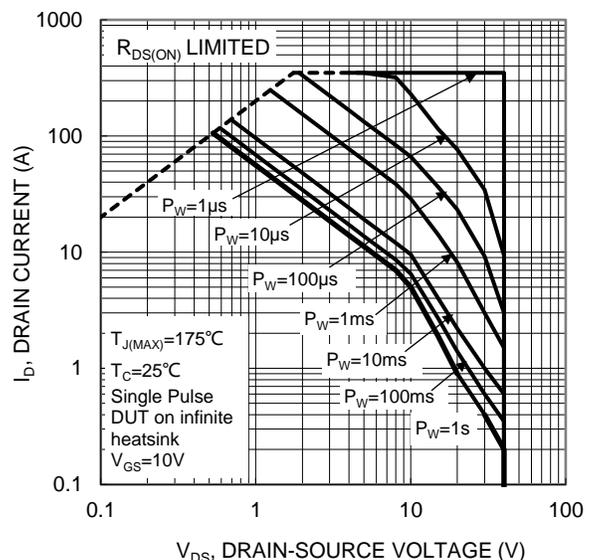
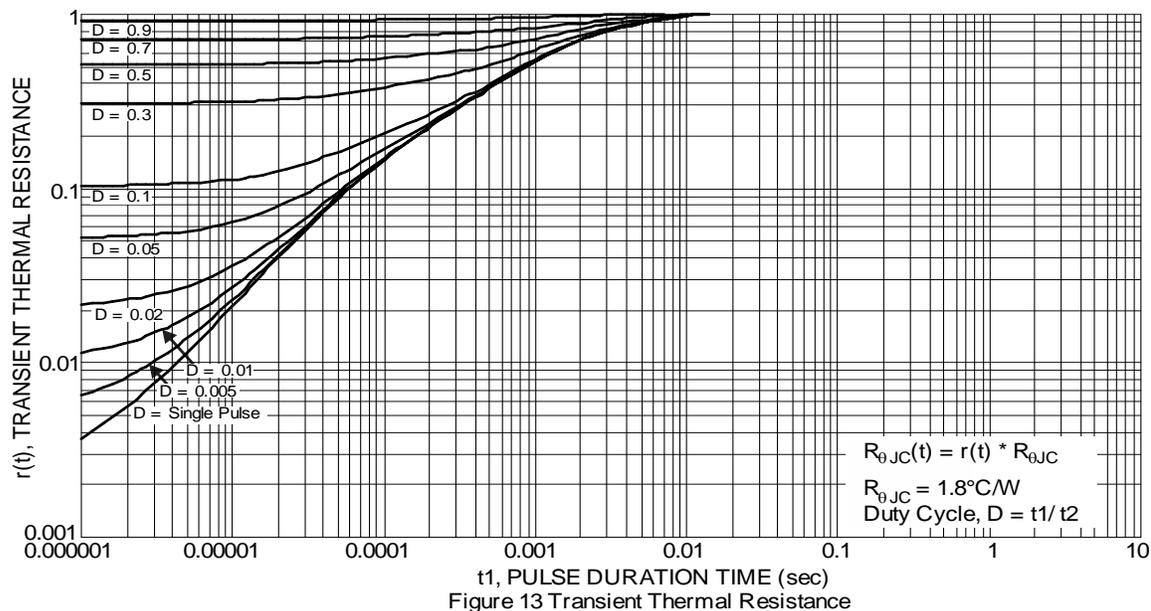


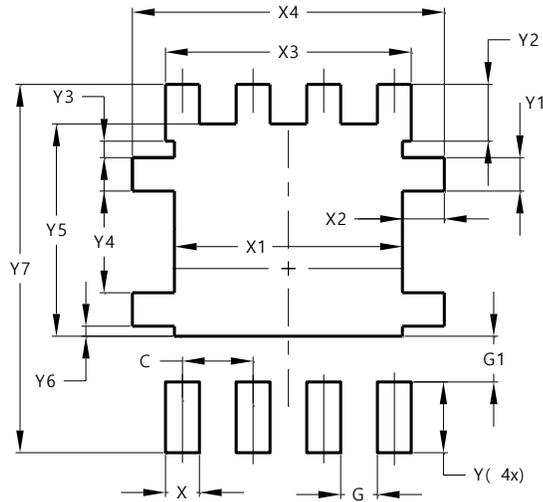
Figure 12. SOA, Safe Operation Area



Suggested Pad Layout

Site 1:

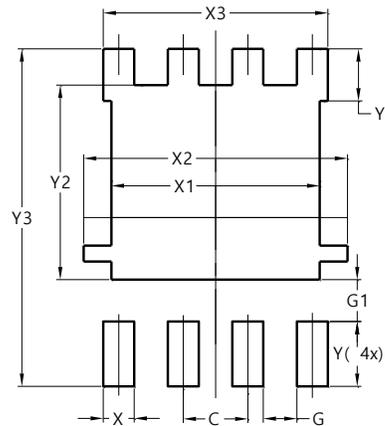
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610