



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max $T_C = +25^\circ C$ (Note 9)
60V	3.8m Ω @ $V_{GS} = 10V$	100A

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

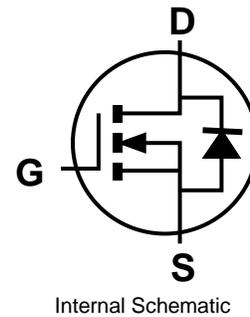
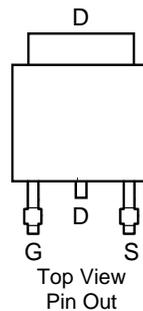
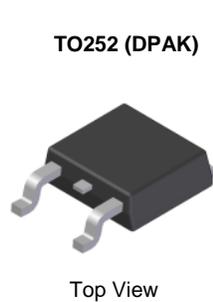
- Engine Management Systems
- Body Control Electronics
- DC-DC Converters
- Motor Control

Features

- Rated to $+175^\circ C$ – Ideal For High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ – Minimizes Power Losses
- Low Q_G – Minimizes Switching Losses

Mechanical Data

- Case: TO252 (DPAK)
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (g3)
- Weight: 0.33 grams (Approximate)



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Note 6)	I_D	$T_C = +25^\circ\text{C}$ (Note 9)	100
		$T_C = +100^\circ\text{C}$	75
Maximum Body Diode Forward Current (Note 6)	I_S	100	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	150	A
Avalanche Current, $L = 0.2\text{mH}$	I_{AS}	45	A
Avalanche Energy, $L = 0.2\text{mH}$	E_{AS}	200	mJ

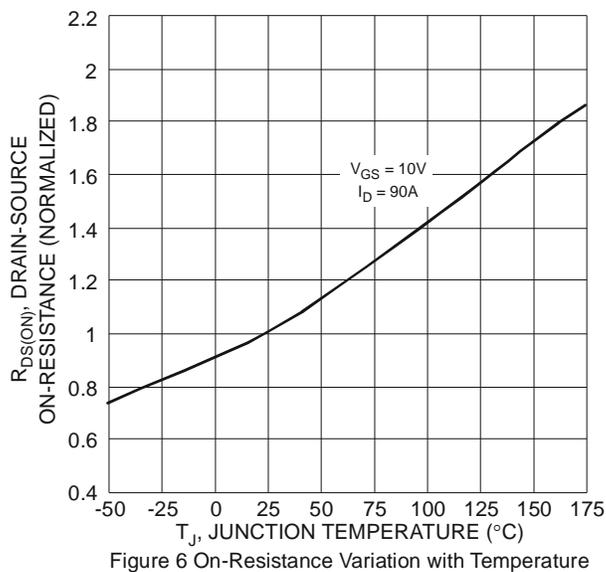
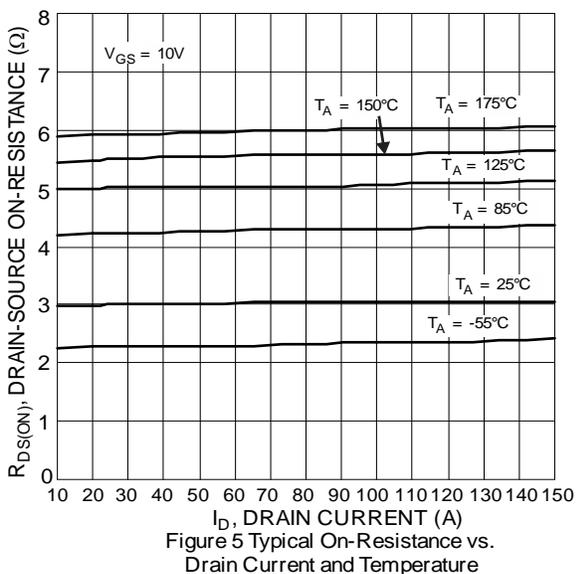
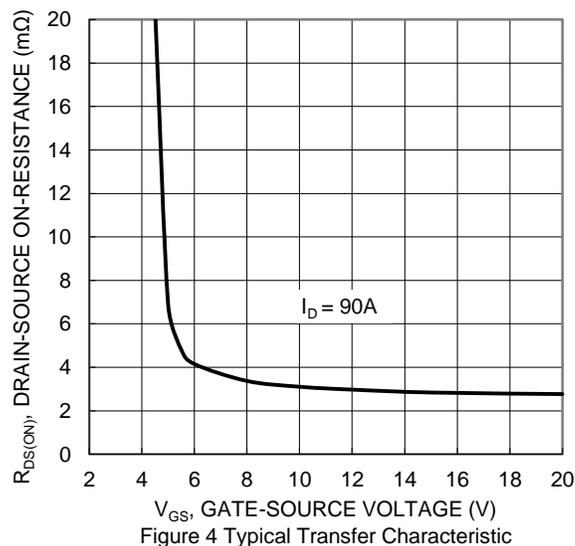
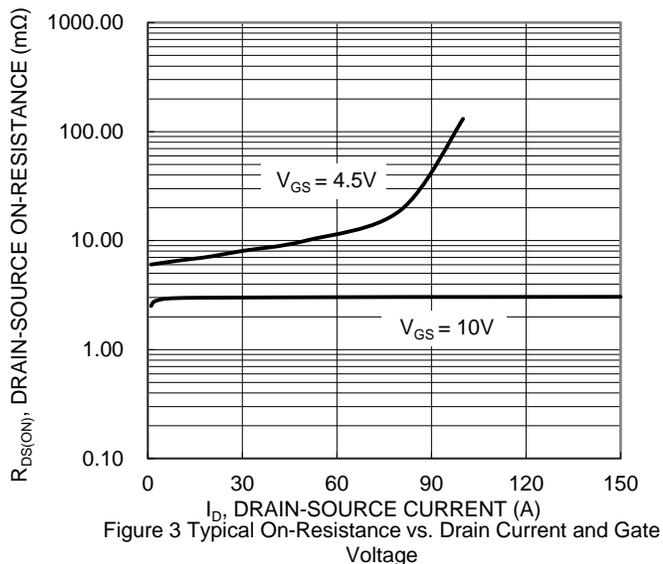
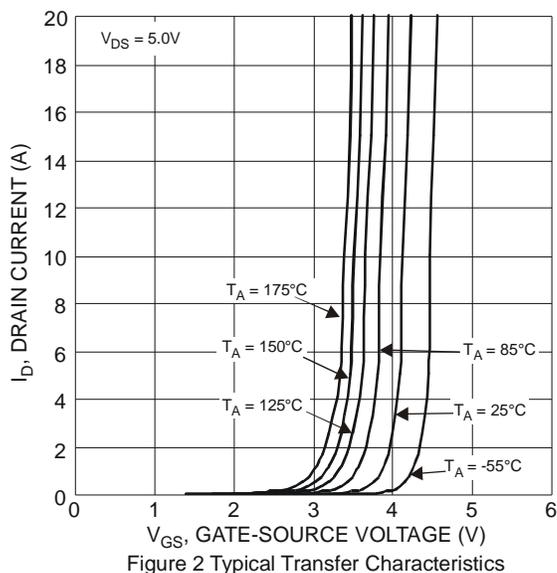
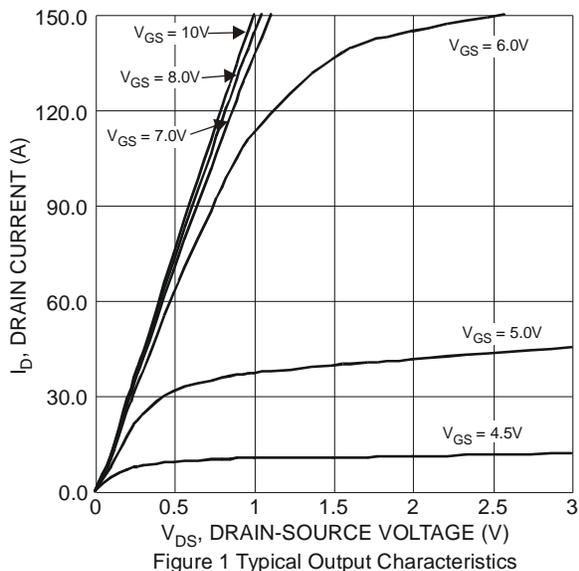
Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	3.9	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	38	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	180	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	0.8	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	3	3.8	m Ω	$V_{GS} = 10\text{V}, I_D = 90\text{A}$
Diode Forward Voltage	V_{SD}	—	0.9	1.2	V	$V_{GS} = 0\text{V}, I_S = 20\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{ISS}	—	4,556	—	pF	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Output Capacitance	C_{OSS}	—	1,383	—		
Reverse Transfer Capacitance	C_{RSS}	—	105.2	—		
Gate Resistance	R_G	—	0.66	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_G	—	95.4	—	nC	$V_{DS} = 30\text{V}, I_D = 90\text{A}, V_{GS} = 10\text{V}$
Gate-Source Charge	Q_{GS}	—	21.6	—		
Gate-Drain Charge	Q_{GD}	—	20.4	—		
Turn-On Delay Time	$t_{D(ON)}$	—	13.2	—	ns	$V_{DD} = 30\text{V}, V_{GS} = 10\text{V}, I_D = 90\text{A}, R_G = 3.5\Omega$
Turn-On Rise Time	t_R	—	11.7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	31	—		
Turn-Off Fall Time	t_F	—	12	—		
Body Diode Reverse Recovery Time	t_{RR}	—	50.5	—	ns	$I_F = 50\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{RR}	—	80.8	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).
 - Short duration pulse test used to minimize self-heating effect
 - Guaranteed by design. Not subject to production testing
 - Package limited.



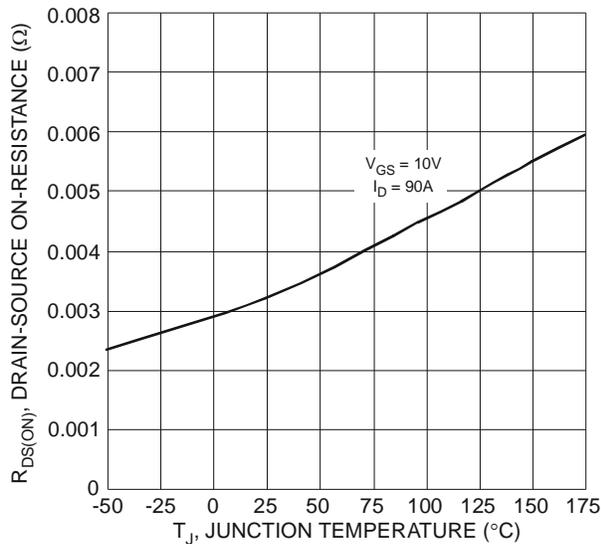


Figure 7 On-Resistance Variation with Temperature

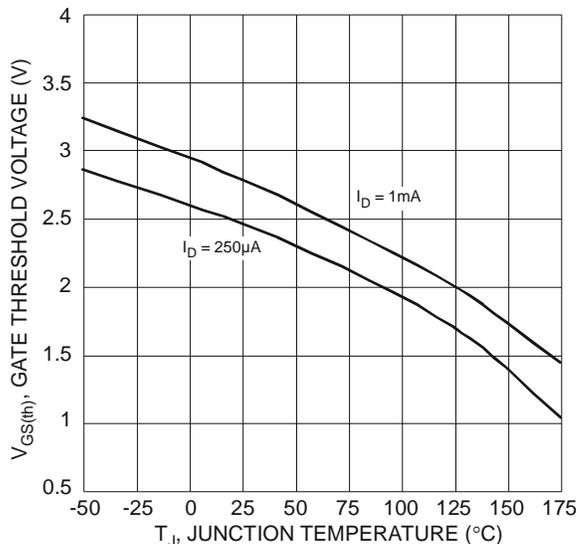


Figure 8 Gate Threshold Variation vs. Ambient Temperature

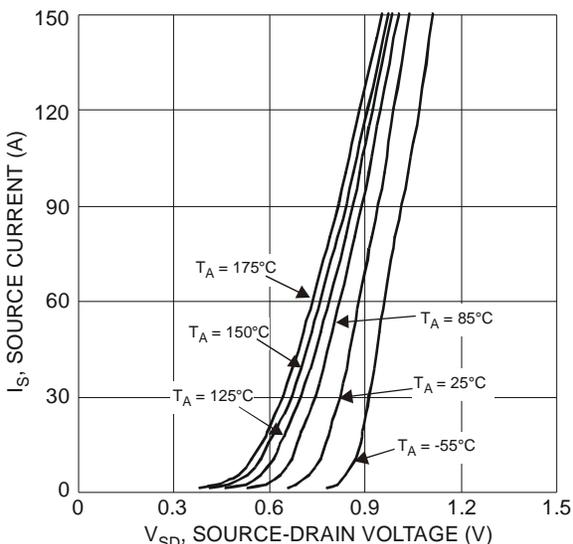


Figure 9 Diode Forward Voltage vs. Current

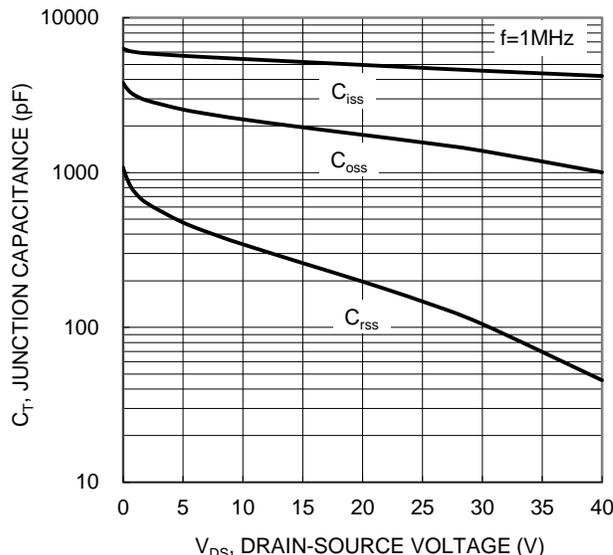


Figure 10 Typical Junction Capacitance

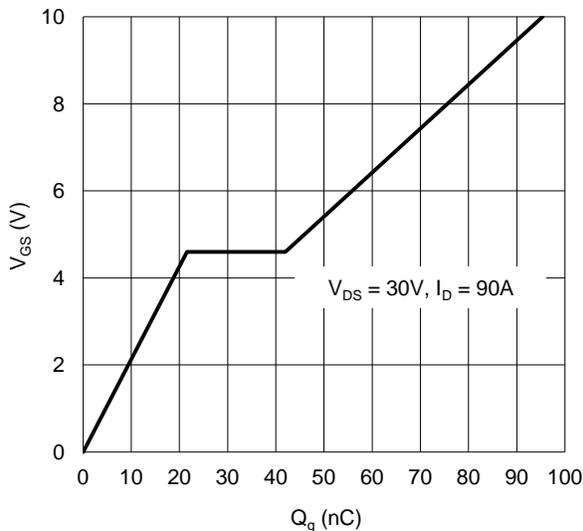


Figure 11 Gate Charge

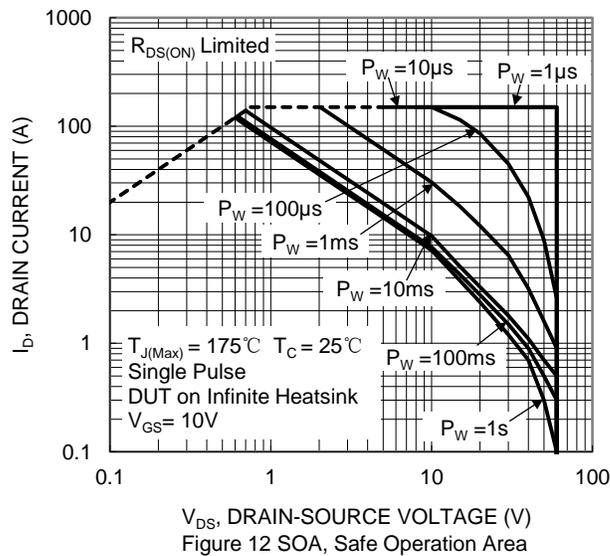


Figure 12 SOA, Safe Operation Area

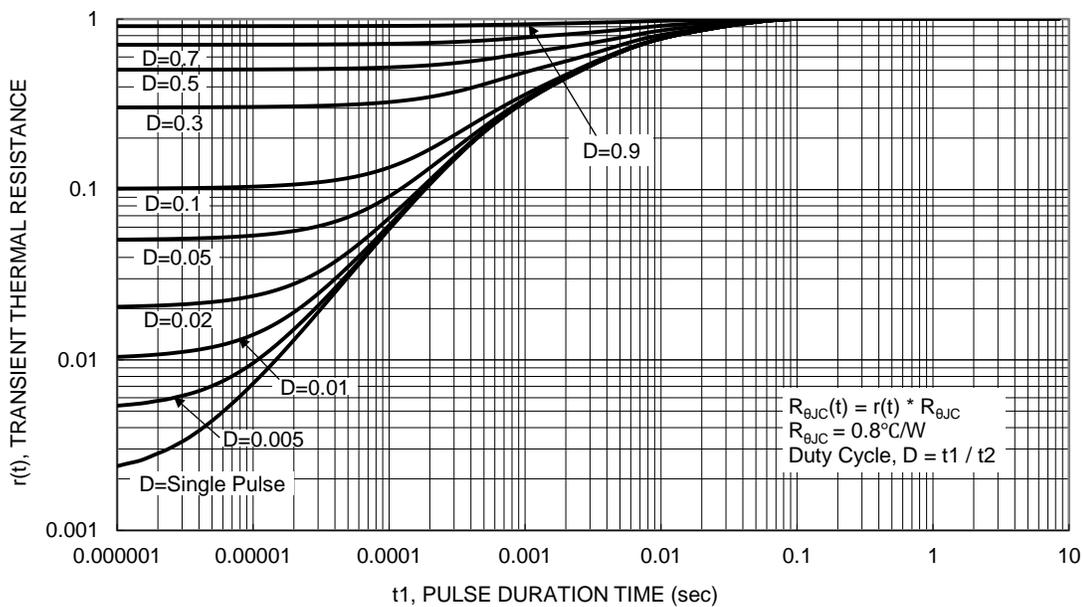
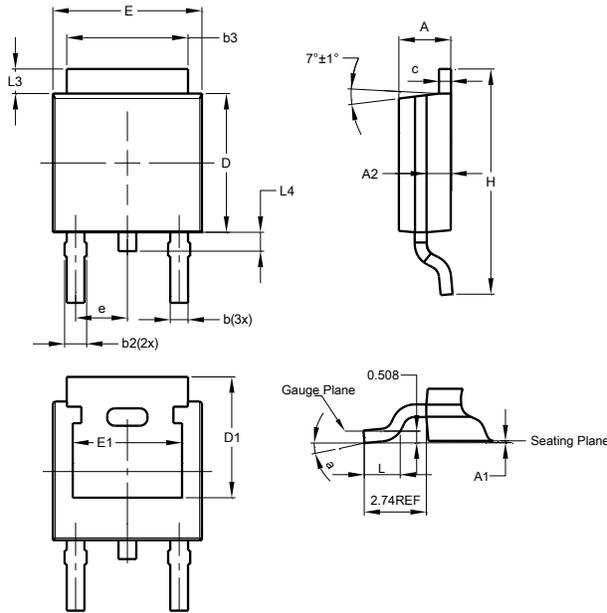


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

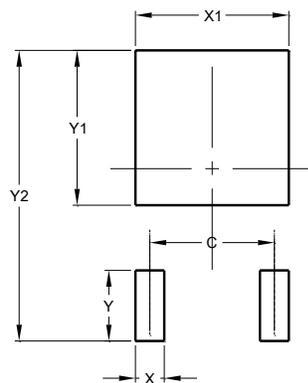
TO252 (DPAK)



TO252 (DPAK)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700