优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max
-200V	80Ω @ V_{GS} = -10V	-65mA

Features and Benefits

- Low Input Capacitance
- Low Input/Output Leakage
- Small Surface Mount Package

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

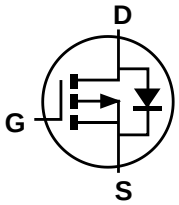
- DC-DC Converters
- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.

Mechanical Data

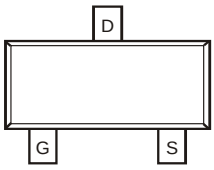
- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Terminals Connections: See Diagram Below
- Weight: 0.008 grams (Approximate)

SOT23

Top View



Equivalent Circuit



Top View
Pin Out Configuration

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-200	V
Gate-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current (Note 6)	I_D	-65	mA
Maximum Body Diode Forward Current (Note 6)	I_S	-65	mA
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)	I_{DM}	-212	mA
Pulsed Source Current (10μs Pulse, Duty Cycle = 1%)	I_{SM}	-212	mA

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Power Dissipation (Note 5)		P_D	0.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	240	°C/W
Power Dissipation (Note 6)		P_D	0.7	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	180	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-200	—	—	V	V_{GS} = 0V, I_D = -1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -200V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.5	—	-3.5	V	V_{DS} = V_{GS}, I_D = -1mA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	51	80	Ω	V_{GS} = -10V, I_D = -30mA
Diode Forward Voltage	V_{SD}	—	-0.7	-1.5	V	V_{GS} = 0V, I_S = -30mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	25	—	pF	V_{DS} = -100V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	9	—		
Reverse Transfer Capacitance	C_{rss}	—	4	—		
Gate Resistance	R_g	—	11.5	—	Ω	f = 1MHz, Level = 50mV, V_{GS} = 5V, V_{DS} = 0V
Total Gate Charge	Q_g	—	1.2	—	nC	V_{GS} = -10V, V_{DS} = -100V I_D = -30mA
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.5	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.7	—	ns	V_{DS} = -100V, I_D = -30mA V_{GS} = -10V, R_g = 1Ω
Turn-On Rise Time	t_R	—	7.5	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	18.5	—		
Turn-Off Fall Time	t_F	—	140	—		
Body Diode Reverse Recovery Time	t_{RR}	—	81	—	ns	I_F = -1A, di/dt = -100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	210	—	nC	

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

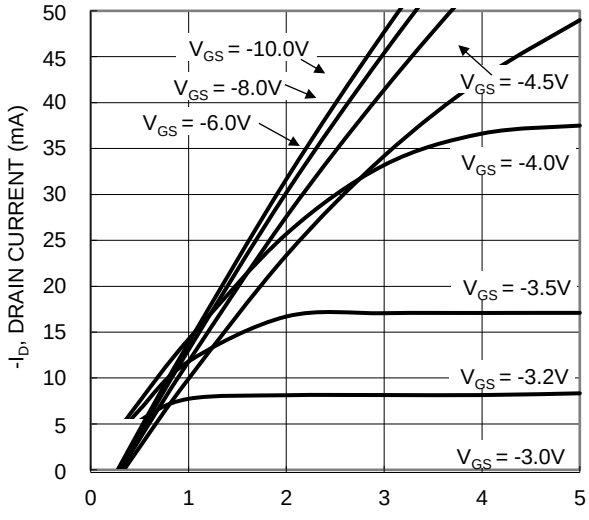


Figure 1. Typical Output Characteristic

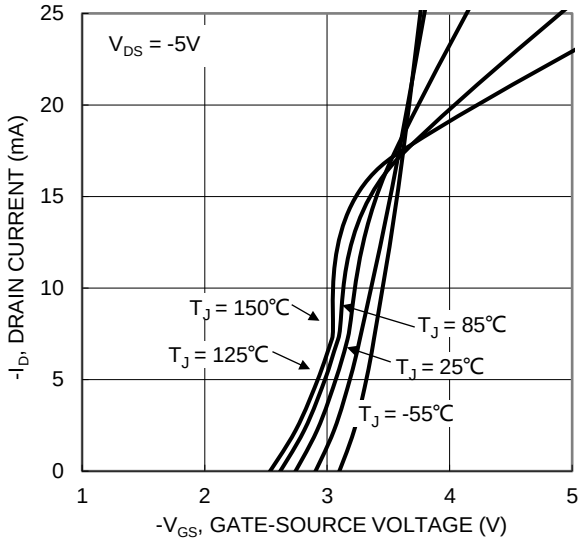


Figure 2. Typical Transfer Characteristic

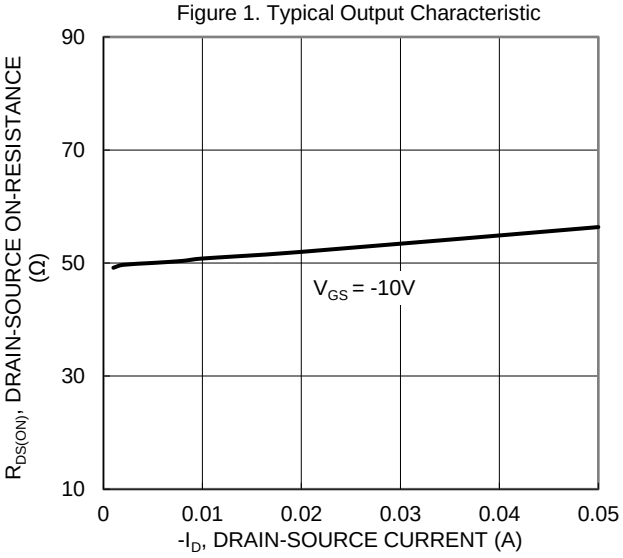


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

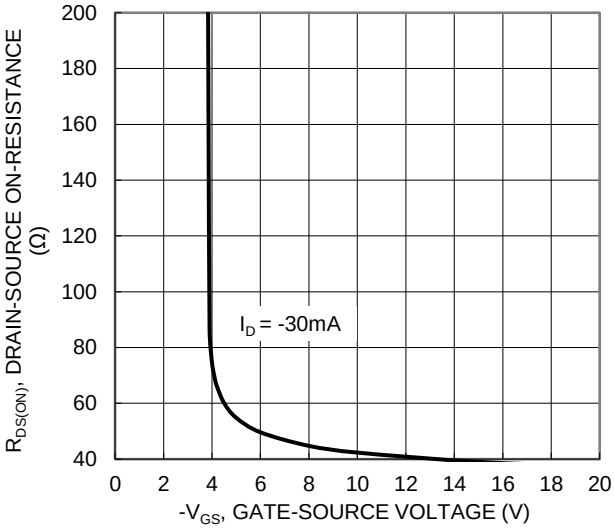


Figure 4. Typical Transfer Characteristic

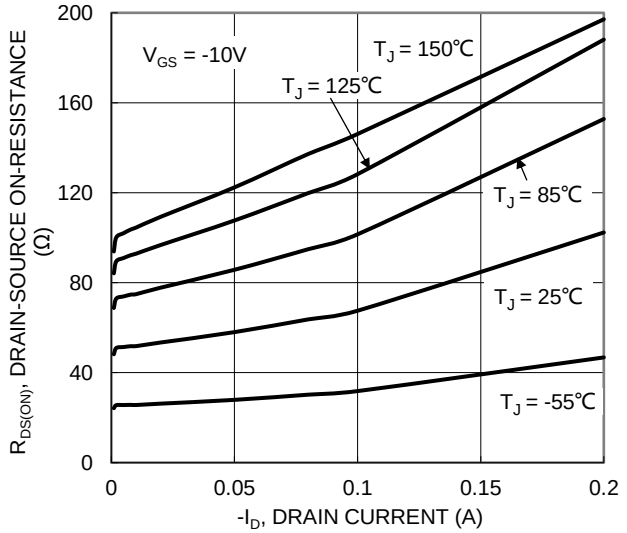


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

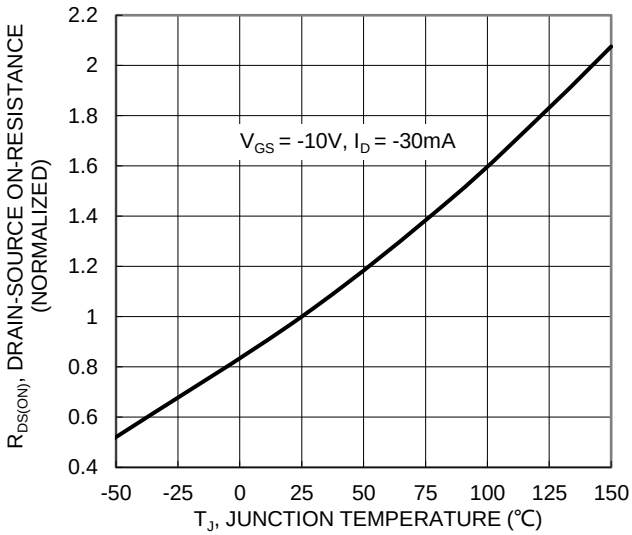


Figure 6. On-Resistance Variation with Junction Temperature

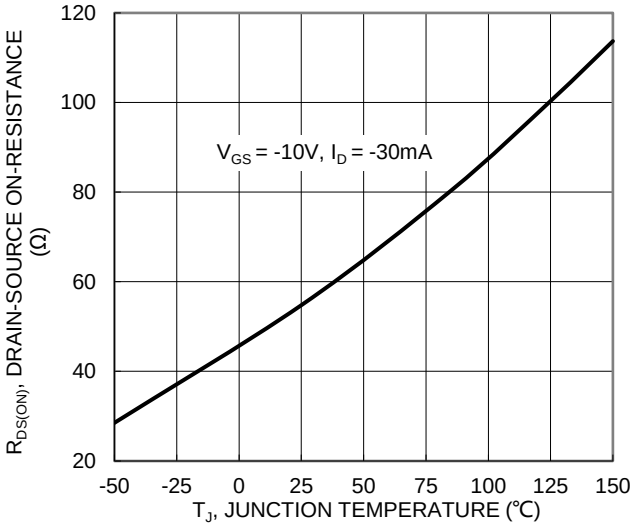


Figure 7. On-Resistance Variation with Temperature

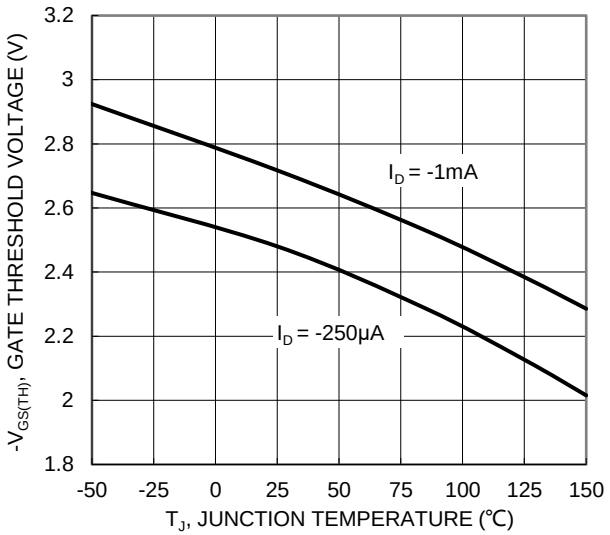


Figure 8. Gate Threshold Variation vs. Junction Temperature

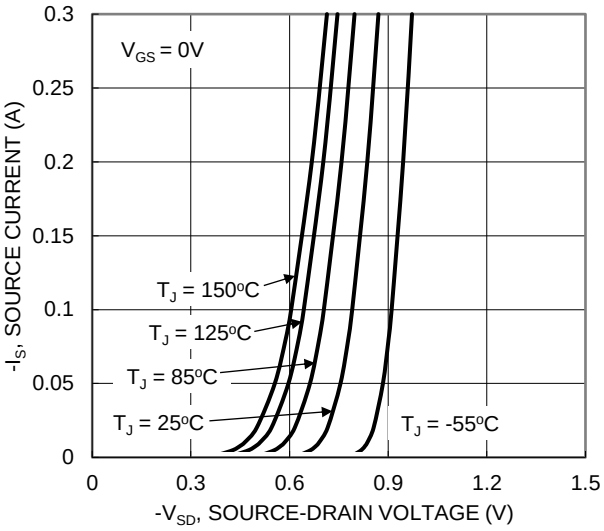


Figure 9. Diode Forward Voltage vs. Current

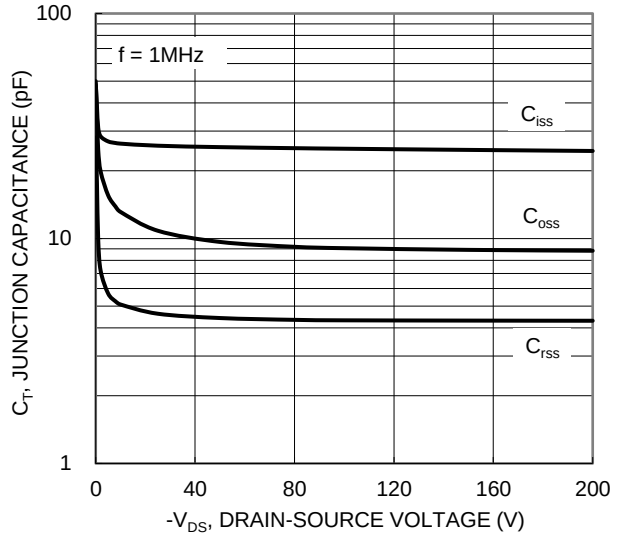


Figure 10. Typical Junction Capacitance

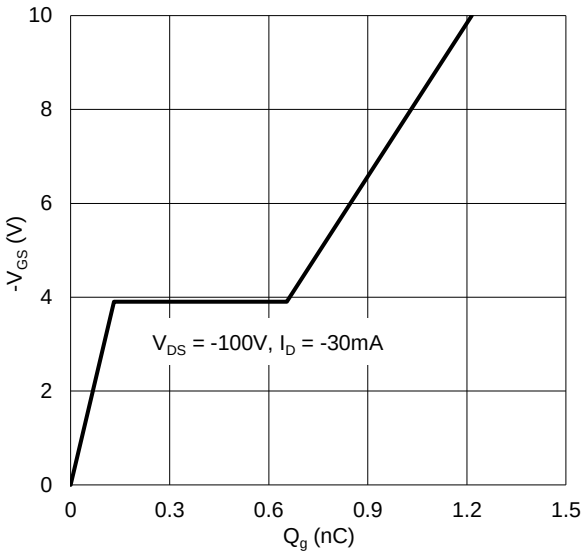


Figure 11. Gate Charge

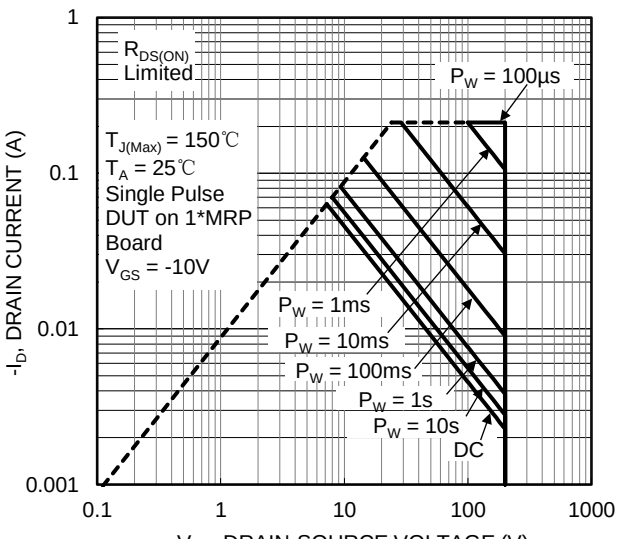


Figure 12. SOA, Safe Operation Area

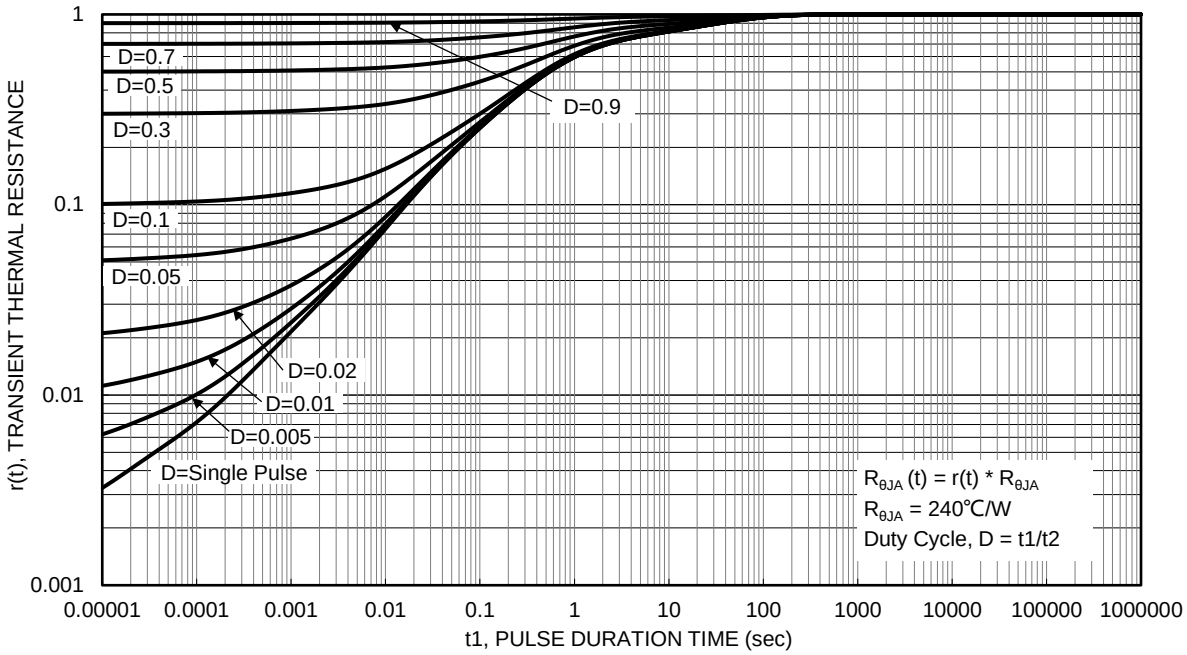
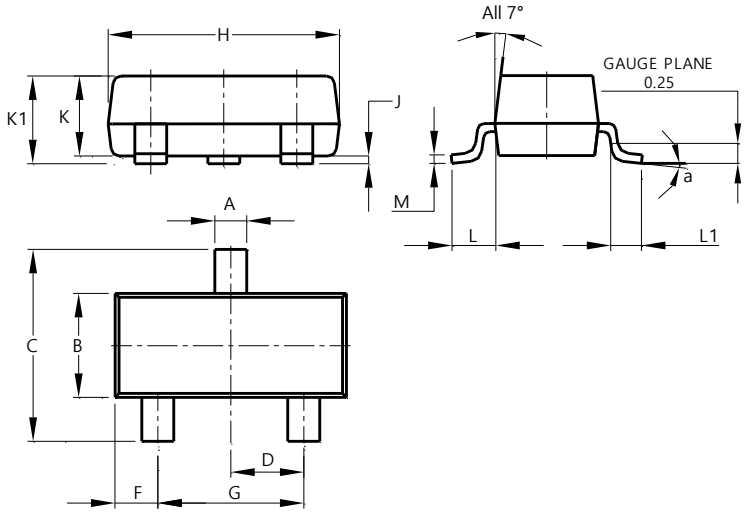


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

SOT23



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT23