



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码

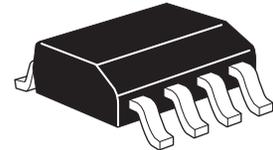


企业QQ二维码

Summary

N-Channel = $V_{(BR)DSS} = 30V$: $R_{DS(on)} = 0.025\Omega$; $I_D = 7.6A$

P-Channel = $V_{(BR)DSS} = -30V$: $R_{DS(on)} = 0.035\Omega$; $I_D = -6.3A$



Description

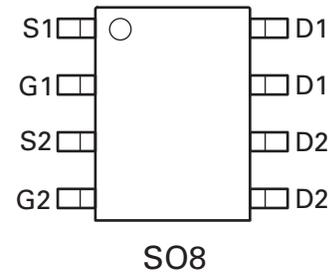
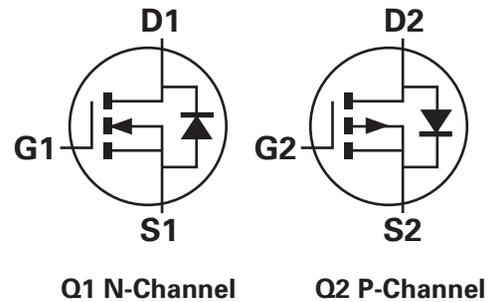
This new generation of trench MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package

Applications

- Motor Drive
- LCD backlighting



Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
NK-ZXMC3A18DN8TC	13	12	2500

Device marking

NK-ZXMC
3A18

Absolute maximum ratings

Parameter	Symbol	N-channel	P-channel	Unit
Drain-source voltage	V_{DSS}	30	-30	V
Gate-source voltage	V_{GS}	± 20	± 20	V
Continuous drain current ($V_{GS}=10V$; $T_{amb}=25^{\circ}C$) ^{(b)(d)} ($V_{GS}=10V$; $T_{amb}=70^{\circ}C$) ^{(b)(d)} ($V_{GS}=10V$; $T_{amb}=25^{\circ}C$) ^{(a)(d)}	I_D	7.6 6.1 5.8	-6.3 -5.0 -4.8	A
Pulsed drain current ^(c)	I_{DM}	37	-30	A
Continuous source current (body diode) ^(b)	I_S	3.6	3.2	A
Pulsed source current (body diode) ^(c)	I_{SM}	37	30	A
Power dissipation at $T_{amb}=25^{\circ}C$ ^{(a)(d)}	P_D	1.25		W
Linear derating factor		10		mW/ $^{\circ}C$
Power dissipation at $T_{amb}=25^{\circ}C$ ^{(a)(e)}	P_D	1.8		W
Linear derating factor		14		mW/ $^{\circ}C$
Power dissipation at $T_{amb}=25^{\circ}C$ ^{(b)(d)}	P_D	2.1		W
Linear derating factor		17		mW/ $^{\circ}C$
Operating and storage temperature range	T_j, T_{stg}	-55 to +150		$^{\circ}C$

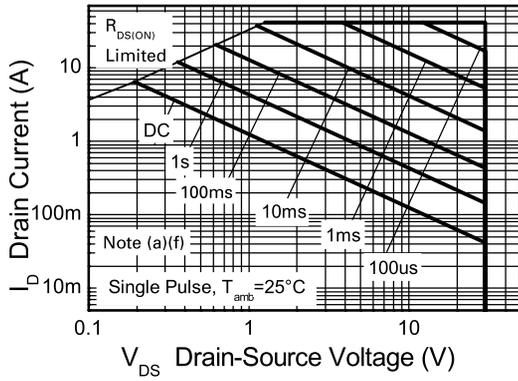
Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient ^{(a)(d)}	$R_{\theta JA}$	100	$^{\circ}C/W$
Junction to ambient ^{(a)(e)}	$R_{\theta JA}$	70	$^{\circ}C/W$
Junction to ambient ^{(b)(d)}	$R_{\theta JA}$	60	$^{\circ}C/W$

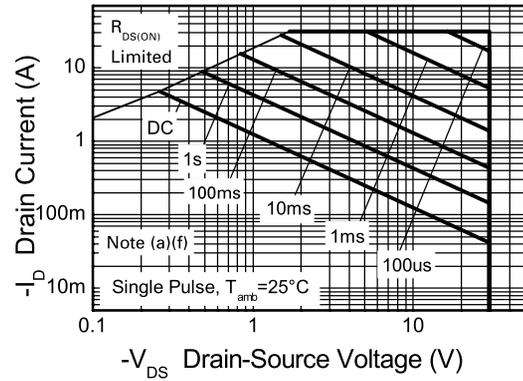
NOTES:

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating - pulse width limited by maximum junction temperature. Pulse width 300 μ s, $d \leq 0.02$. Refer to transient thermal impedance graph.
- (d) For device with one active die.
- (e) For device with two active die running at equal power.

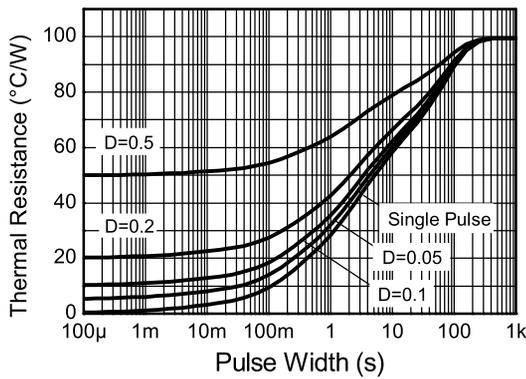
Characteristics



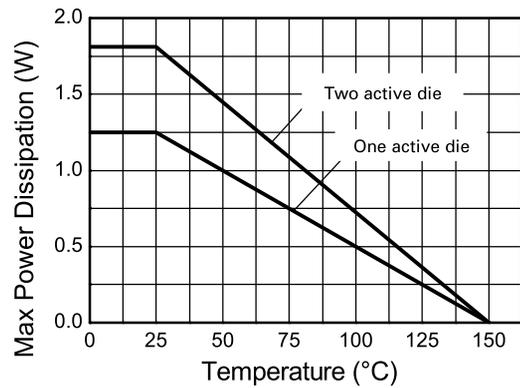
N-channel Safe Operating Area



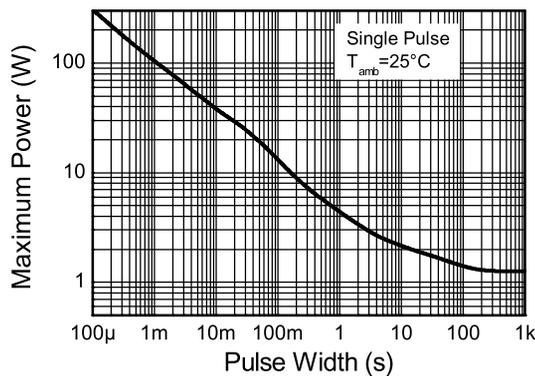
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

N-channel
Electrical characteristics (at $T_{amb} = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	30			V	$I_D = 250\mu A, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}			0.5	μA	$V_{DS} = 30V, V_{GS} = 0V$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	1.0			V	$I_D = 250\mu A, V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.025 0.030	Ω	$V_{GS} = 10V, I_D = 5.8A$ $V_{GS} = 4.5V, I_D = 5.3A$
Forward transconductance ^{(*)(‡)}	g_{fs}		17.5		S	$V_{DS} = 15V, I_D = 5.8A$
Dynamic^(‡)						
Input capacitance	C_{iss}		1800		pF	$V_{DS} = 25V, V_{GS} = 0V$ $f = 1MHz$
Output capacitance	C_{oss}		289		pF	
Reverse transfer capacitance	C_{rss}		178		pF	
Switching^{(†) (‡)}						
Turn-on-delay time	$t_{d(on)}$		5.5		ns	$V_{DD} = 15V, I_D = 6A$ $R_G \cong 6.0\Omega, V_{GS} = 10V$
Rise time	t_r		8.7		ns	
Turn-off delay time	$t_{d(off)}$		33		ns	
Fall time	t_f		8.5		ns	
Gate charge	Q_g		19.4		nC	$V_{DS} = 15V, V_{GS} = 5V$ $I_D = 3.5A$
Total gate charge	Q_g		36		nC	$V_{DS} = 15V, V_{GS} = 10V$ $I_D = 3.5A$
Gate-source charge	Q_{gs}		5.5		nC	
Gate drain charge	Q_{gd}		7.0		nC	
Source-drain diode						
Diode forward voltage ^(*)	V_{SD}			0.95	V	$T_j = 25^{\circ}C, I_S = 6A, V_{GS} = 0V$
Reverse recovery time ^(‡)	t_{rr}		20.5		ns	$T_j = 25^{\circ}C, I_S = 6A,$ $di/dt = 100A/\mu s$
Reverse recovery charge ^(‡)	Q_{rr}		41.5		nC	

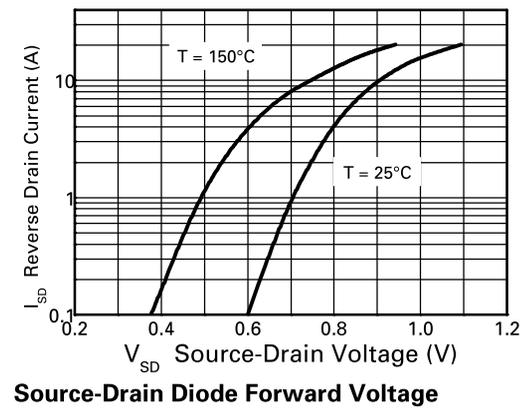
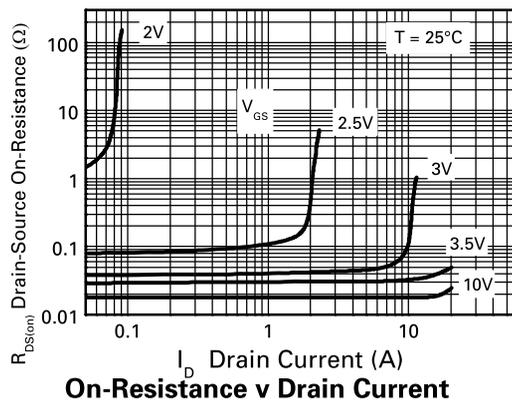
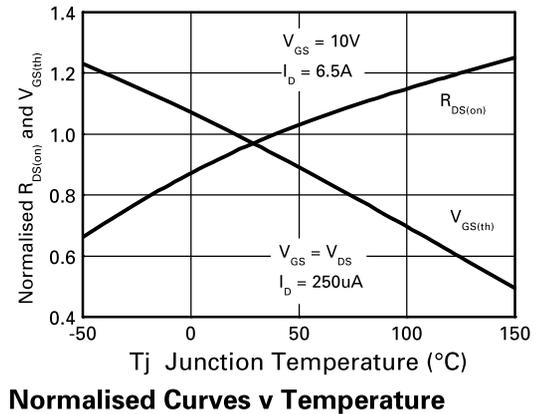
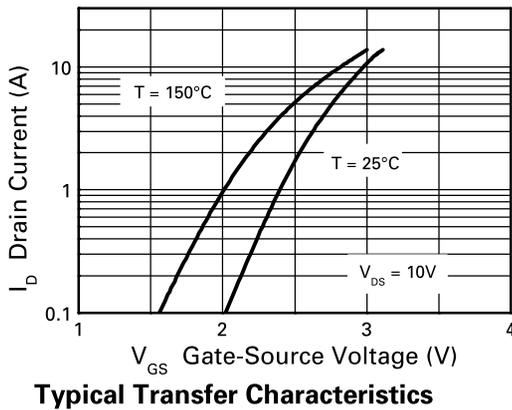
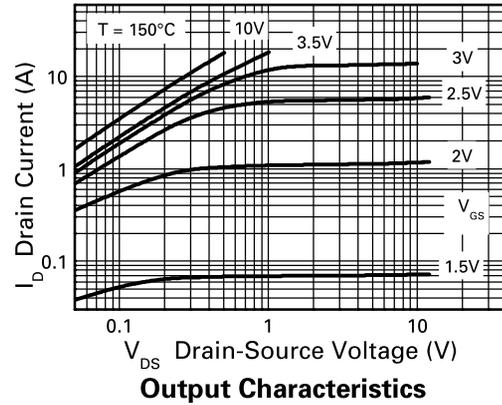
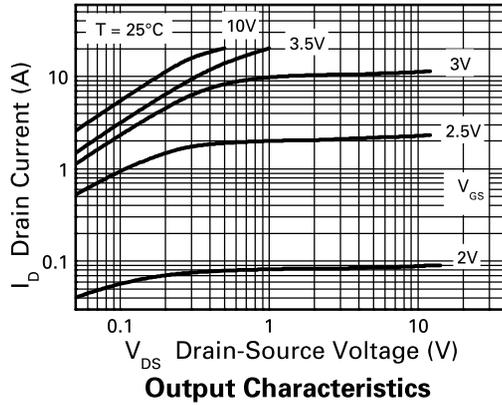
NOTES:

 (*) Measured under pulsed conditions. Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

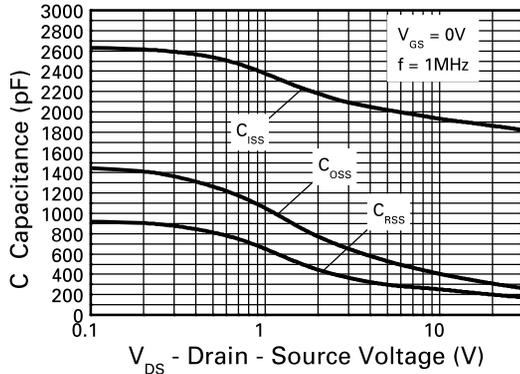
(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing.

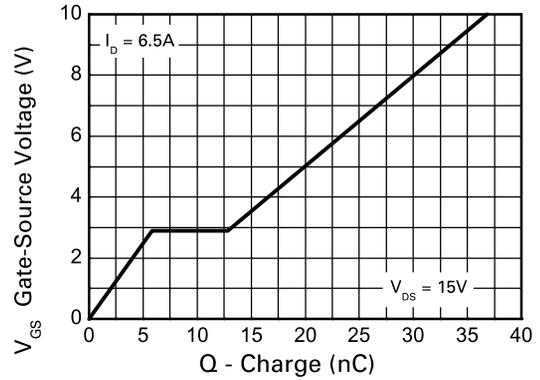
Typical characteristics



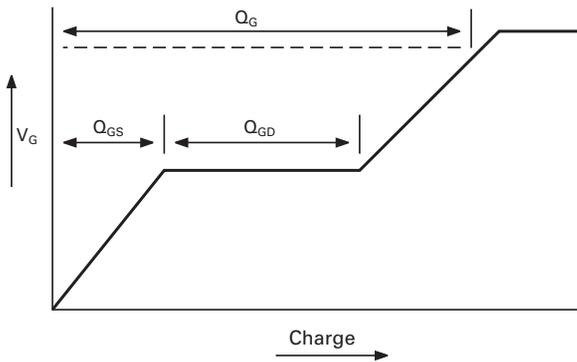
Typical characteristics



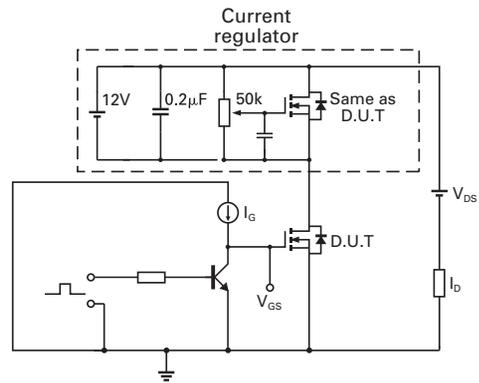
Capacitance v Drain-Source Voltage



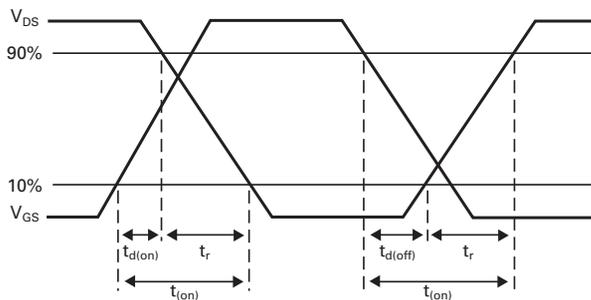
Gate-Source Voltage v Gate Charge



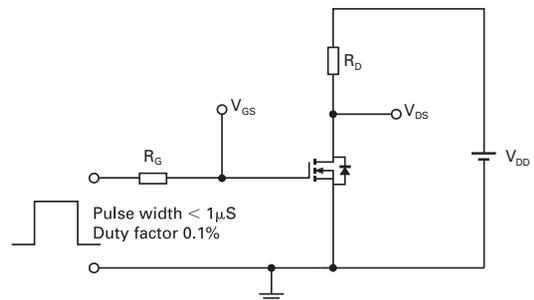
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

P-channel
Electrical characteristics (at $T_{amb} = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30			V	$I_D = -250\mu A, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}			-1.0	μA	$V_{DS} = -30V, V_{GS} = 0V$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	-1.0			V	$I_D = -250\mu A, V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.035 0.050	W	$V_{GS} = -10V, I_D = -4.8A$ $V_{GS} = -4.5V, I_D = -4.0A$
Forward transconductance ^{(*)(‡)}	g_{fs}		8.6		S	$V_{DS} = -15V, I_D = -4.8A$
Dynamic^(‡)						
Input capacitance	C_{iss}		1603		pF	$V_{DS} = -15V, V_{GS} = 0V$ $f = 1MHz$
Output capacitance	C_{oss}		434		pF	
Reverse transfer capacitance	C_{rss}		388		pF	
Switching^{(†)(‡)}						
Turn-on-delay time	$t_{d(on)}$		4.8		ns	$V_{DD} = -15V, I_D = -1A$ $R_G @ 6.0\Omega, V_{GS} = 10V$
Rise time	t_r		9.5		ns	
Turn-off delay time	$t_{d(off)}$		60		ns	
Fall time	t_f		38		ns	
Gate charge	Q_g		25		nC	$V_{DS} = -15V, V_{GS} = -5V$ $I_D = -4.8A$
Total gate charge	Q_g		45		nC	$V_{DS} = -15V, V_{GS} = -10V$ $I_D = -4.8A$
Gate-source charge	Q_{gs}		5.1		nC	
Gate drain charge	Q_{gd}		11.5		nC	
Source-drain diode						
Diode forward voltage ^(*)	V_{SD}		0.82	-0.95	V	$T_j = 25^{\circ}C, I_S = -3.7$ $V_{GS} = 0V$
Reverse recovery time ^(‡)	t_{rr}		32.5		ns	$T_j = 25^{\circ}C, I_S = -2.2,$ $di/dt = 100A/\mu s$
Reverse recovery charge ^(‡)	Q_{rr}		18.4		nC	

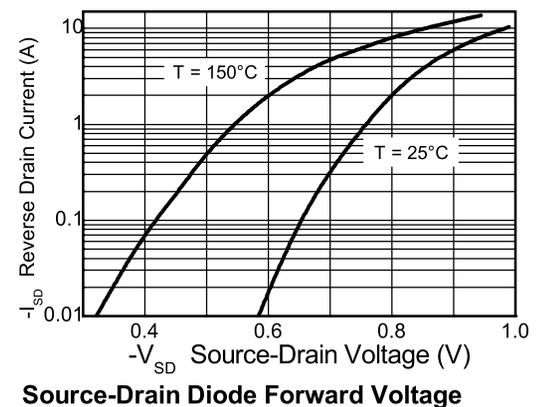
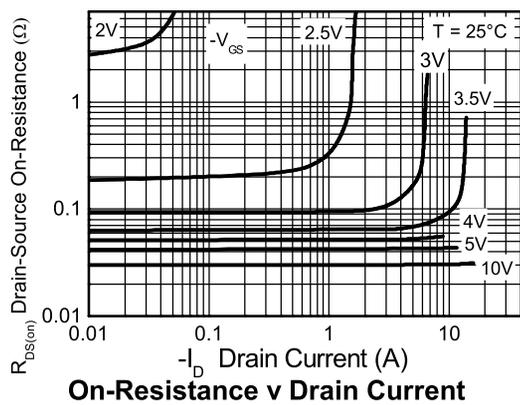
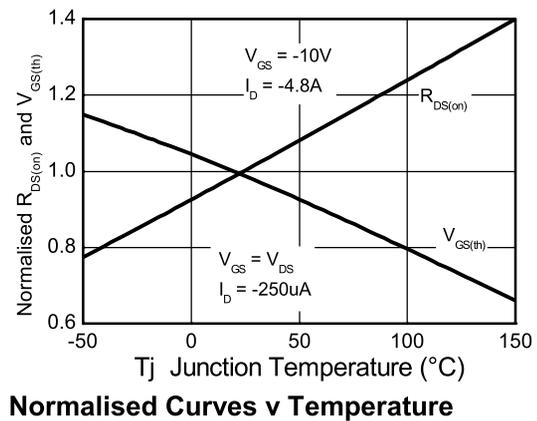
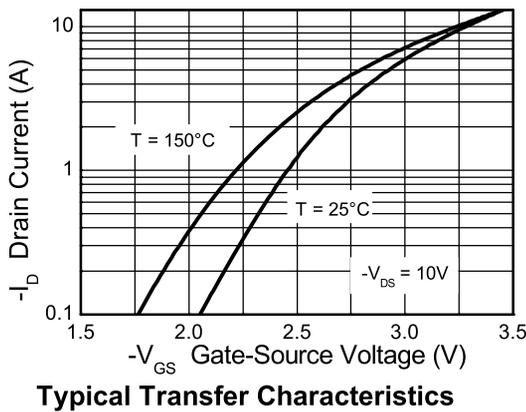
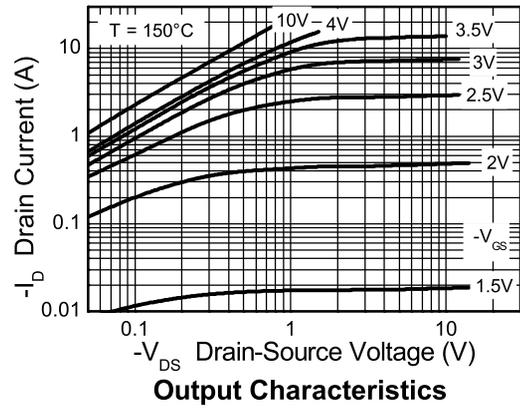
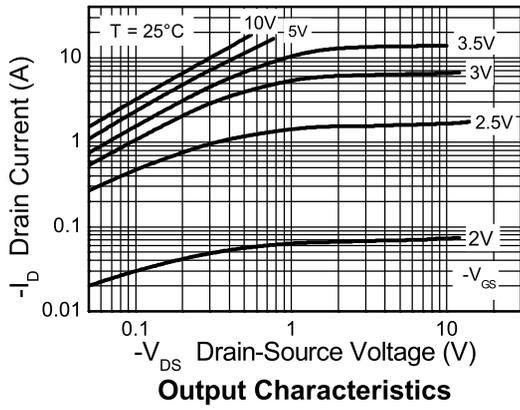
NOTES:

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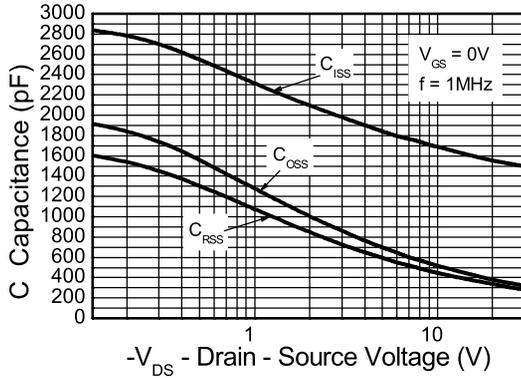
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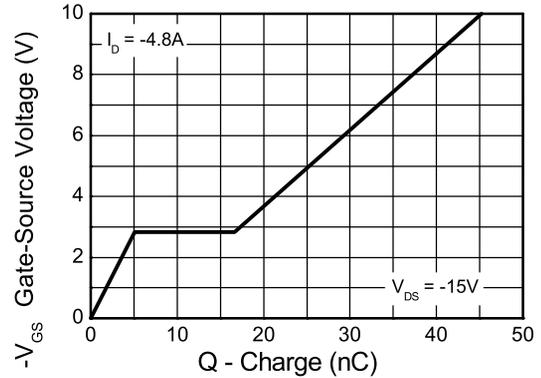
Typical characteristics



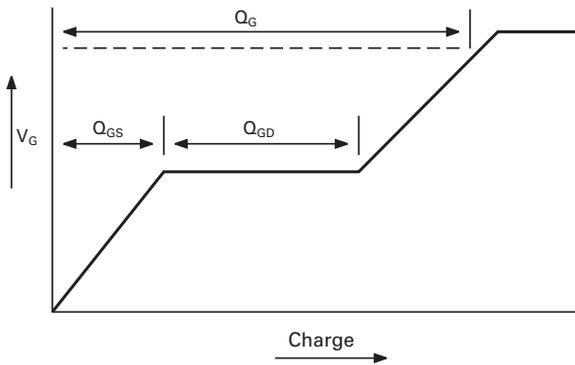
Typical characteristics



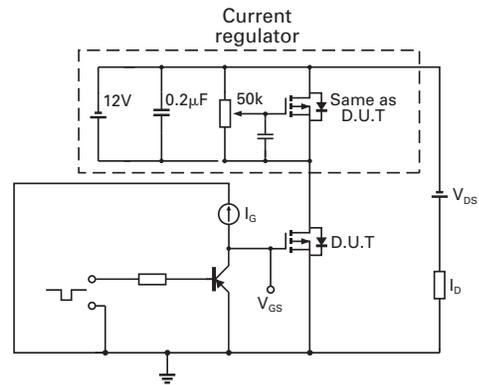
Capacitance v Drain-Source Voltage



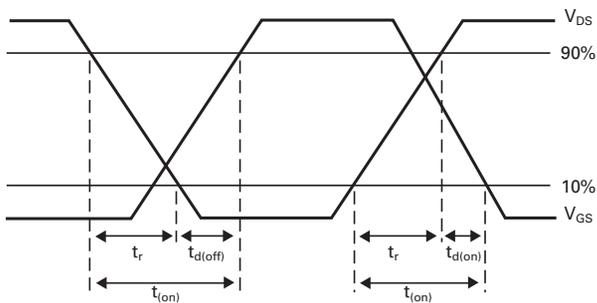
Gate-Source Voltage v Gate Charge



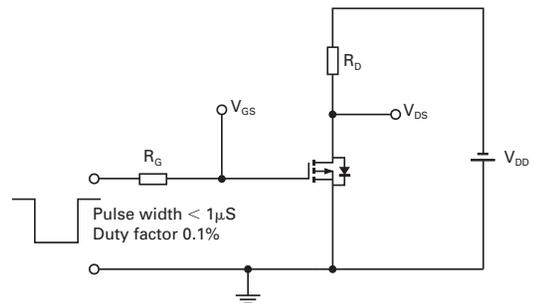
Basic gate charge waveform



Gate charge test circuit

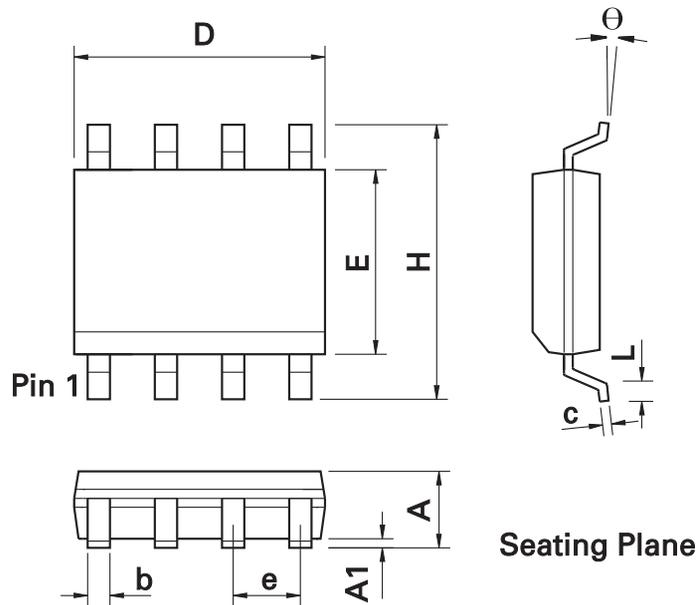


Switching time waveforms



Switching time test circuit

Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	theta	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters