优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

企业微信二维码

企业QQ二维码

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
100V	0.25Ω	2.1A

Features

- Low On-Resistance
- Fast Switching Speed
- Low Threshold
- Low Gate Drive
- Low Profile SOIC Package

Description

This new generation of trench MOSFETs utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high-efficiency, low-voltage, power-management applications.

Applications

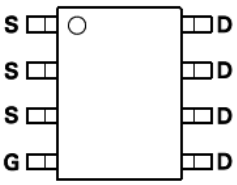
- DC-DC converters
- Power-management functions
- Disconnect switches
- Motor controls

Mechanical Data

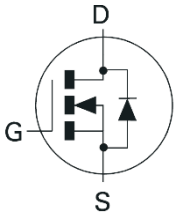
- Package: SO-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.076 grams (Approximate)

SO-8

Top View



Top View
Pin Configuration



Equivalent Circuit

Absolute Maximum Ratings

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate Source Voltage		V_{GS}	±20	V
Continuous Drain Current	V_{GS} = 10V, T_A = +25°C (Note 5)	I_D	2.1	A
	V_{GS} = 10V, T_A = +70°C (Note 5)		1.7	
	V_{GS} = 10V, T_A = +25°C (Note 6)		1.6	
Pulsed Drain Current (Note 7)		I_{DM}	9	A
Continuous Source Current (Body Diode) (Note 5)		I_S	2.6	A
Pulsed Source Current (Body Diode) (Note 7)		I_{SM}	9	A
Power Dissipation at T_A = +25°C (Note 6) Linear Derating Factor		P_D	1.25 10	W mW/°C
Power Dissipation at T_A = +25°C (Note 5) Linear Derating Factor		P_D	1.8 14.5	W mW/°C
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 6)	$R_{\theta JA}$	100	°C/W
Junction to Ambient (Note 5)	$R_{\theta JA}$	69	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	I_D = 250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.5	μA	V_{DS} = 100V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	2.0	—	—	V	I_D = 250μA, V_{DS} = V_{GS}
Static Drain-Source On-State Resistance (Note 8)	$R_{DS(on)}$	— —	— —	0.25 0.30	Ω	V_{GS} = 10V, I_D = 3.2A V_{GS} = 6V, I_D = 2.6A
Forward Transconductance (Notes 8 & 9)	g_{fs}	—	5.0	—	S	V_{DS} = 15V, I_D = 3.2A
DYNAMIC (Note 9)						
Input Capacitance	C_{iss}	—	405	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	28.2	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	14.2	—	pF	
SWITCHING (Notes 9 & 10)						
Turn-On Delay Time	$t_{d(on)}$	—	3.4	—	ns	V_{DD} = 30V, I_D = 1.2A $R_G \cong$ 6.0Ω, V_{GS} = 10V
Rise Time	t_r	—	2.2	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	—	8	—	ns	
Fall Time	t_f	—	3.2	—	ns	
Gate Charge	Q_g	—	4.2	—	nC	V_{DS} = 50V, V_{GS} = 5V I_D = 1.2A
Total Gate Charge	Q_g	—	7.7	—	nC	V_{DS} = 50V, V_{GS} = 10V I_D = 1.2A
Gate-Source Charge	Q_{gs}	—	1.8	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.1	—	nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (Note 8)	V_{SD}	—	0.87	0.95	V	T_J = +25°C, I_S = 3.2A V_{GS} = 0V
Reverse Recovery Time (Note 9)	t_{rr}	—	27	—	ns	T_J = +25°C, I_F = 1.2A dI/dt = 100A/μs
Reverse Recovery Charge (Note 9)	Q_{rr}	—	32	—	nC	

Notes:
5. For a device surface-mounted on FR4 PCB measured at t ≤ 5 secs.
6. For a device surface-mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
7. Repetitive rating 25mm x 25mm FR4 PCB, D = 0.02, pulse width 300μs – pulse width limited by maximum junction temperature.
8. Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
9. For design aid only, not subject to production testing.
10. Switching characteristics are independent of operating junction temperature.

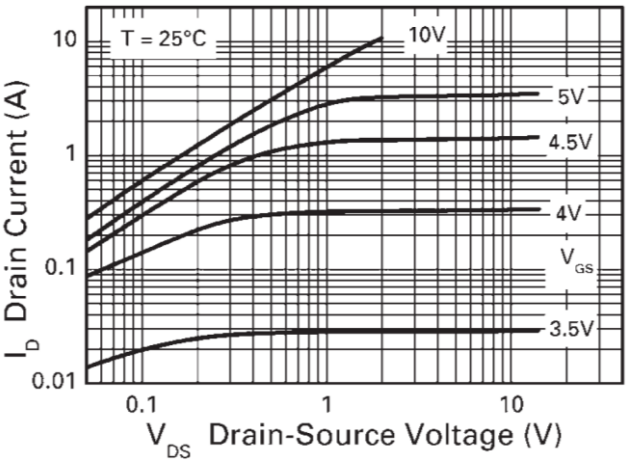


Figure 1. Output Characteristics

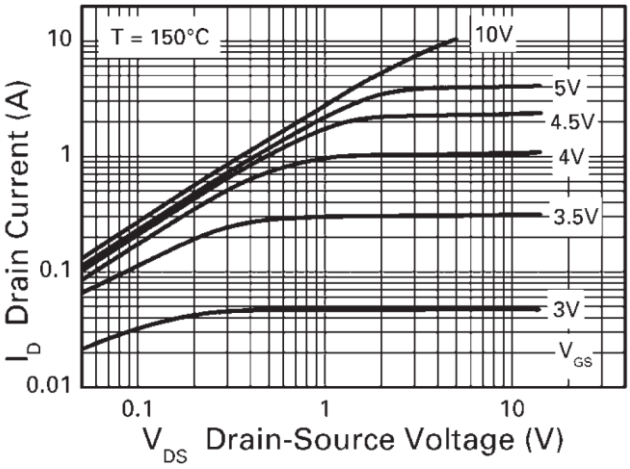


Figure 2. Output Characteristics

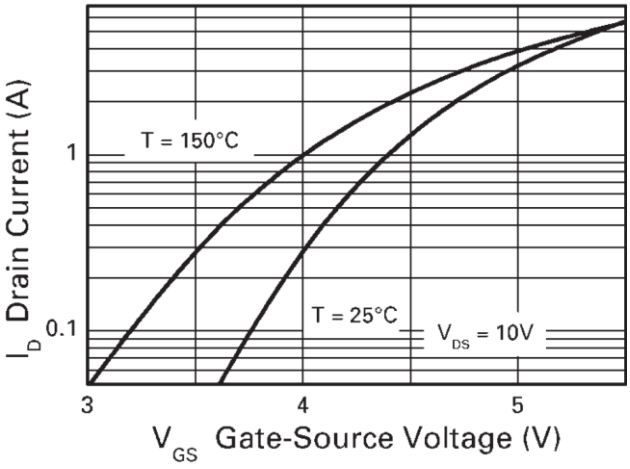


Figure 3. Typical Transfer Characteristics

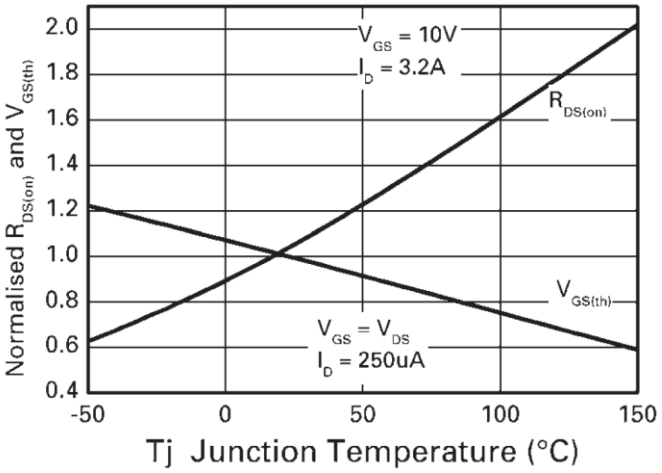


Figure 4. Normalized Curves vs. Temperature

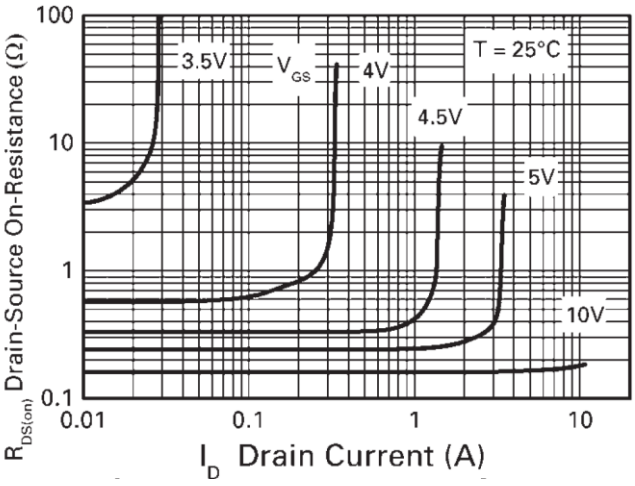


Figure 5. On-Resistance vs. Drain Current

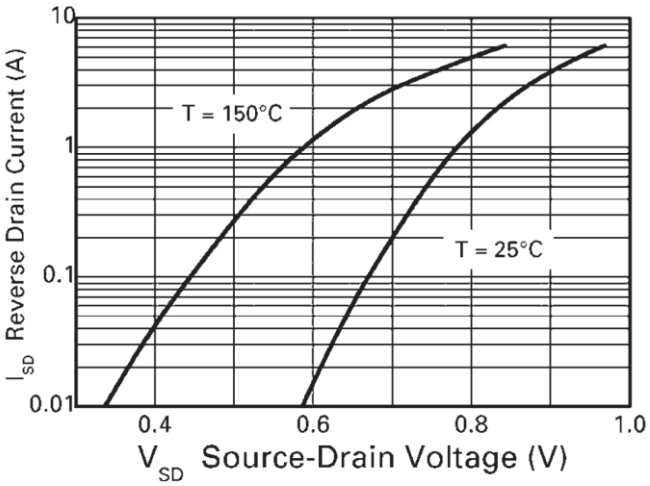


Figure 6. Source-Drain Diode Forward Voltage

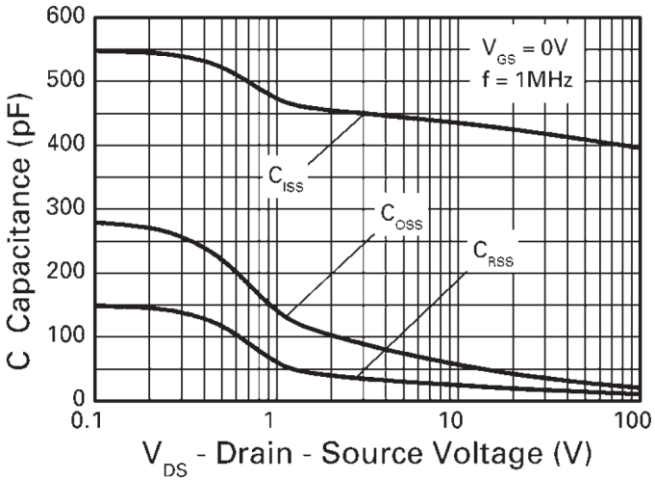


Figure 7. Capacitance vs. Drain-Source Voltage

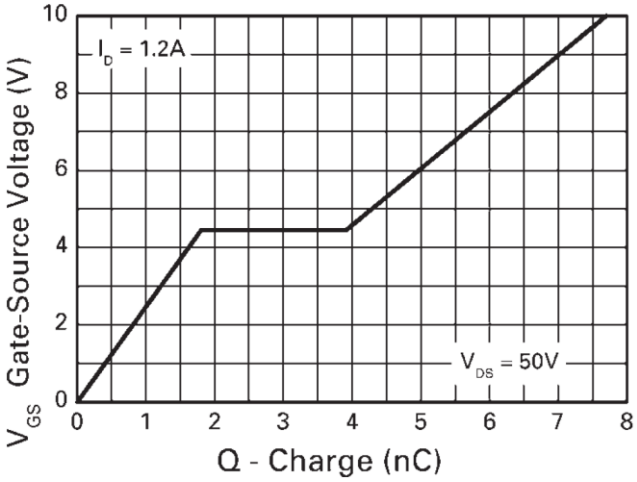


Figure 8. Gate-Source Voltage vs. Gate Charge

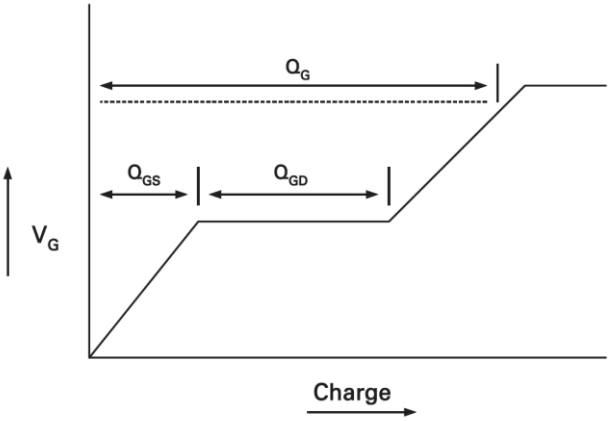


Figure 9. Basic Gate Charge Waveform

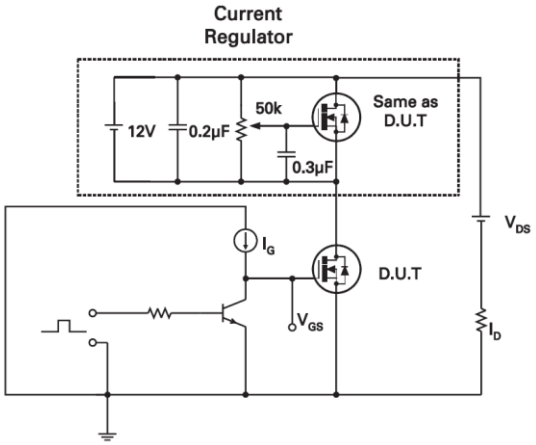


Figure 10. Gate Charge Test Circuit

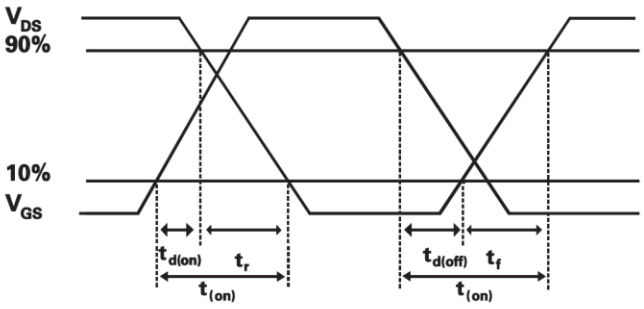


Figure 11. Switching Time Waveforms

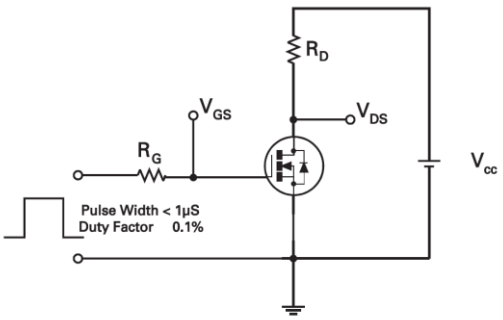
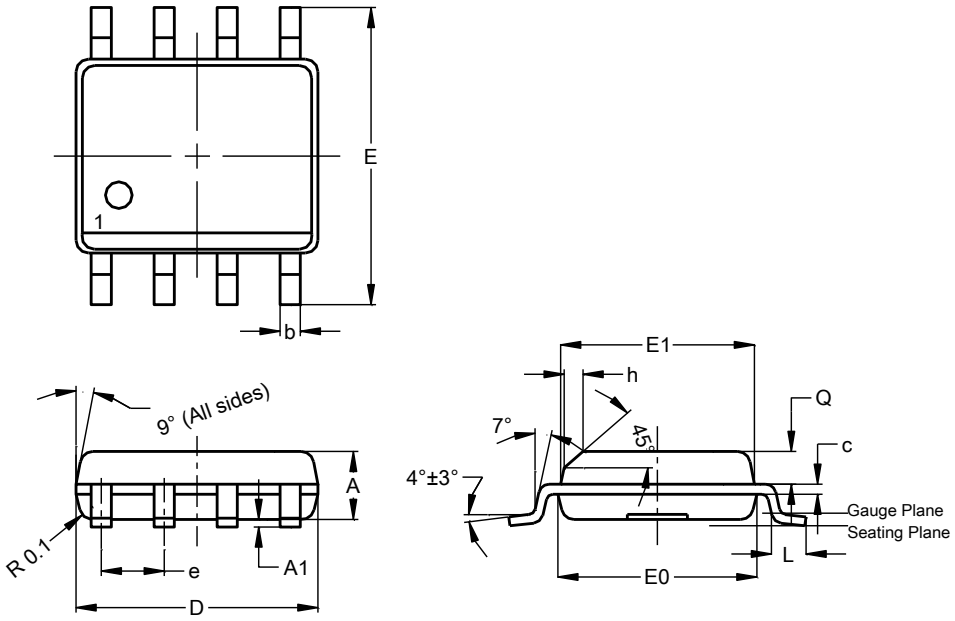


Figure 12. Switching Time Test Circuit

Package Outline Dimensions

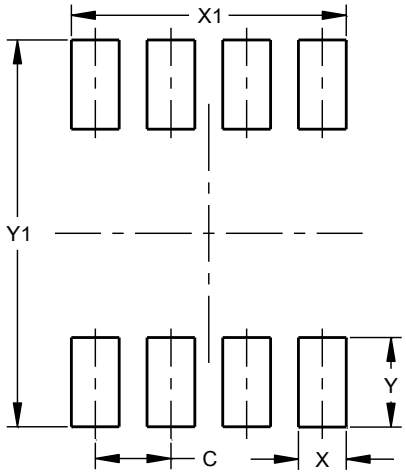
SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50