优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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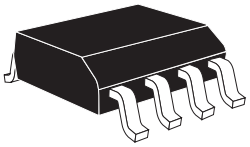
SUMMARY

$V_{(BR)DSS}$= 20V; $R_{DS(ON)}$= 0.025Ω ; I_D= 7.7A

DESCRIPTION

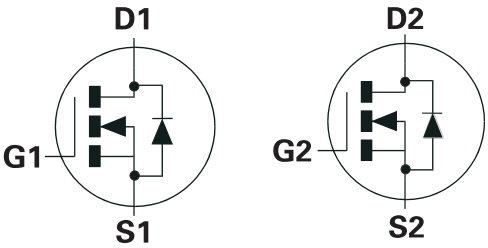
This new generation of TRENCH MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.



SO8

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package



APPLICATIONS

- DC - DC converters
- Power management functions
- Disconnect switches
- Motor control

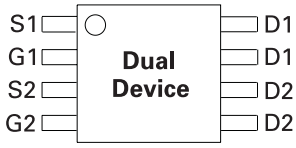
ORDERING INFORMATION

DEVICE	REEL	TAPE WIDTH	QUANTITY PER REEL
NK-ZXMN2A04DN8TA	7''	12mm	500 units
NK-ZXMN2A04DN8TC	13''	12mm	2500 units

DEVICE MARKING

NK-ZXMN
2A04D

PINOUT



Top view

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	20	V
Gate Source Voltage	V_{GS}	±12	V
Continuous Drain Current (V_{GS}=10V; T_A=25°C) [b] [d]	I_D	7.7	A
(V_{GS}=10V; T_A=70°C) [b] [d]		6.2	A
(V_{GS}=10V; T_A=25°C) [a] [d]		5.9	A
Pulsed Drain Current [c]	I_{DM}	38	A
Continuous Source Current (Body Diode) [b]	I_S	2.9	A
Pulsed Source Current (Body Diode) [c]	I_{SM}	38	A
Power Dissipation at T_A=25°C [a] [d]	P_D	1.25	W
Linear Derating Factor		10	mW/°C
Power Dissipation at T_A=25°C [a] [e]	P_D	1.8	W
Linear Derating Factor		14	mW/°C
Power Dissipation at T_A=25°C [b] [d]	P_D	2.1	W
Linear Derating Factor		17	mW/°C
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient [a] [d]	$R_{\Theta JA}$	100	°C/W
Junction to Ambient [b] [e]	$R_{\Theta JA}$	70	°C/W
Junction to Ambient [b] [d]	$R_{\Theta JA}$	60	°C/W

NOTES:

(a) For a dual device surface mounted on 25mm x 25mm FR4 PCB with coverage of single sided 1oz copper in still air conditions.

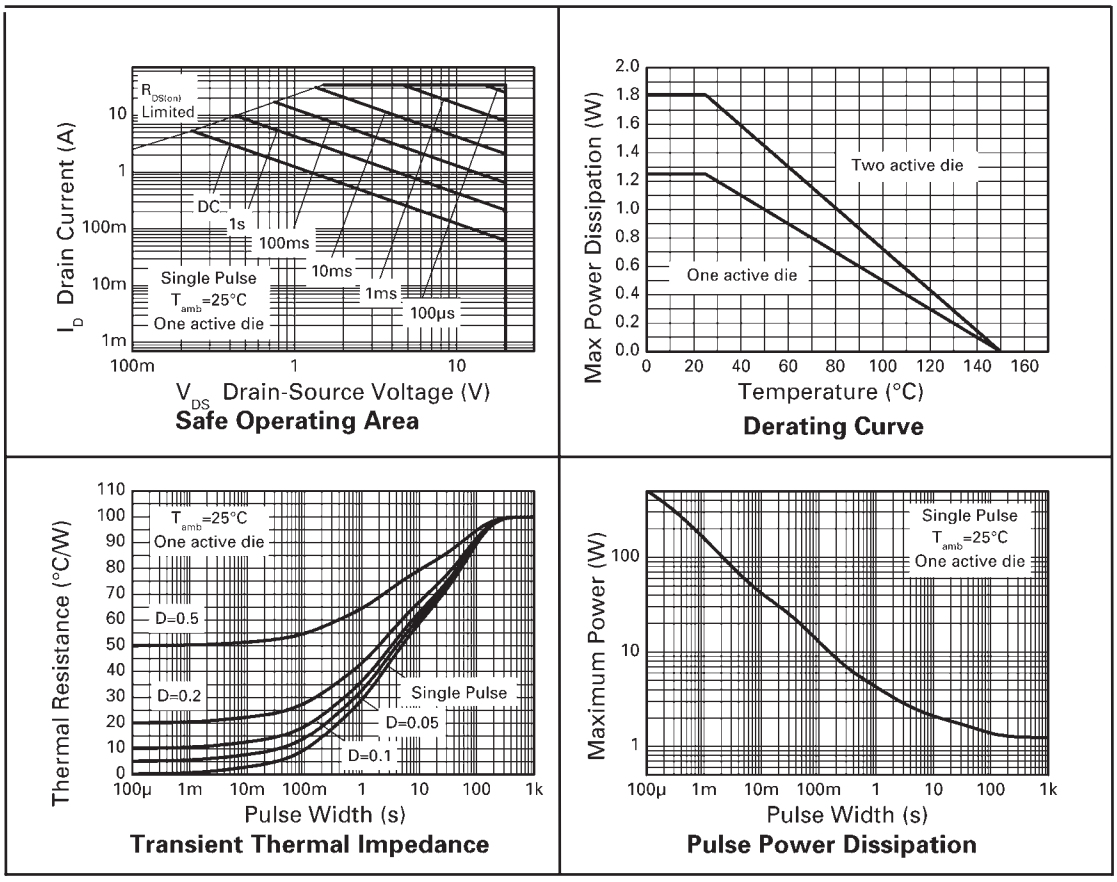
(b) For a dual device surface mounted on FR4 PCB measured at t ≤10 sec.

(c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.02 pulse width=300μs - pulse width limited by maximum junction temperature. Refer to Trnsient Thermal Impedance Graph.

(d) For a dual device with one active die.

(e) For dual device with 2 active die running at equal power.

CHARACTERISTICS



ELECTRICAL CHARACTERISTICS (at T_A = 25°C unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	20			V	I_D=250μA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			0.5	μA	V_{DS}=20V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±12V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.7			V	I_D=250μA, V_{DS} = V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.025 0.035	Ω Ω	V_{GS}=4.5V, I_D=5.9A V_{GS}=2.5V, I_D=5A
Forward Transconductance (3)	g_{fs}		40		S	V_{DS}=10V,I_D=5.9A
DYNAMIC (3)						
Input Capacitance	C_{iss}		1880		pF	V_{DS}=10V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{oss}		506		pF	
Reverse Transfer Capacitance	C_{rss}		386		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		7.9		ns	V_{DD} =10V, I_D=1A R_G≅6Ω, V_{GS}=5V
Rise Time	t_r		14.8		ns	
Turn-Off Delay Time	$t_{d(off)}$		50.5		ns	
Fall Time	t_f		30.6		ns	
Gate Charge	Q_g		22.1		nC	V_{DS}=15V,V_{GS}=5V, I_D=3.5A
Total Gate Charge	Q_g		40.5		nC	V_{DS}=10V,V_{GS}=4.5V, I_D=5.9A
Gate-Source Charge	Q_{gs}		5.6		nC	
Gate-Drain Charge	Q_{gd}		8.0		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}		0.85	0.95	V	T_J=25°C, I_S=5.1A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		18.0		ns	T_J=25°C, I_F=1.9A, di/dt= 100A/μs
Reverse Recovery Charge (3)	Q_{rr}		8.9		nC	

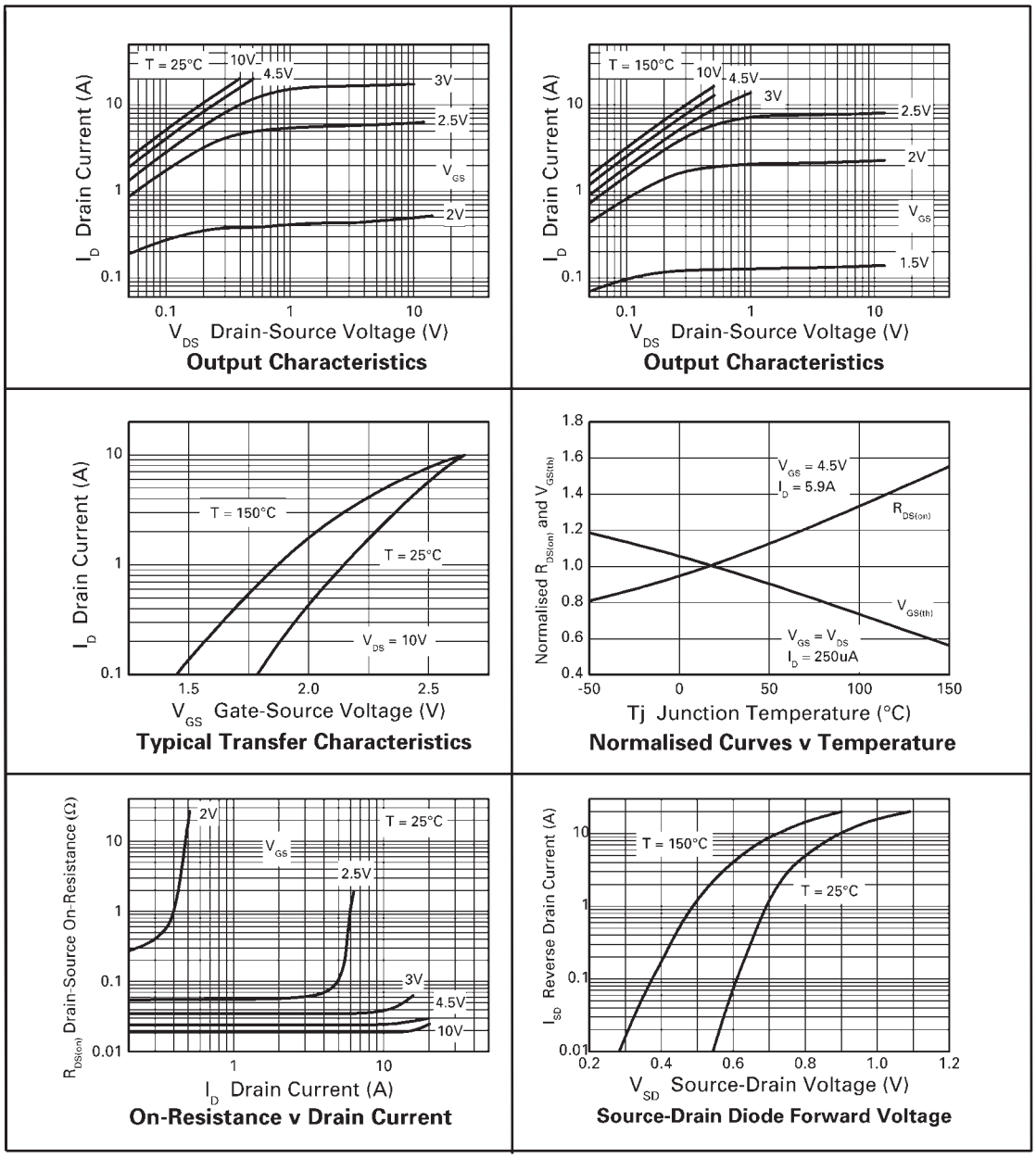
NOTES:

(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤ 2% .

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

TYPICAL CHARACTERISTICS



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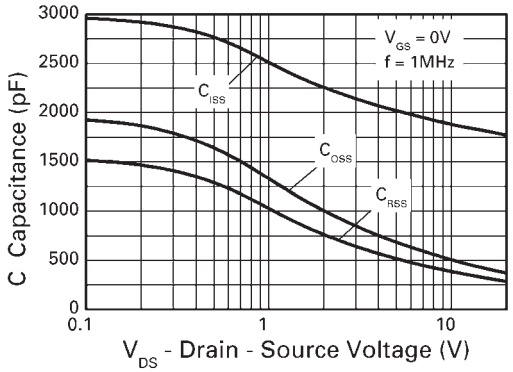
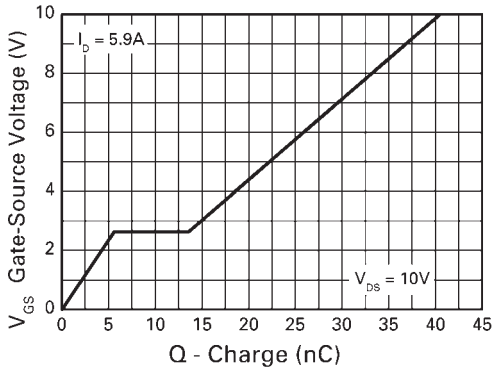
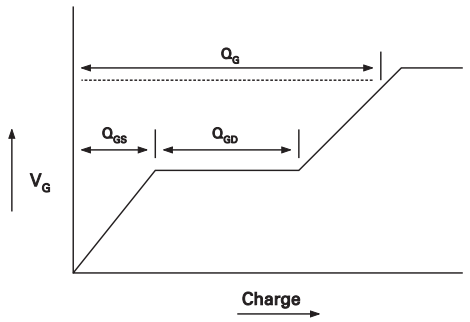


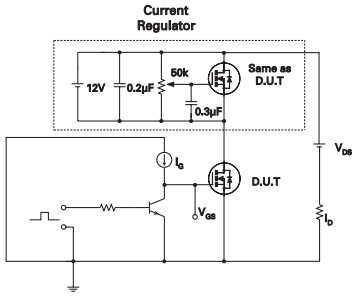
Capacitance v Drain-Source Voltage



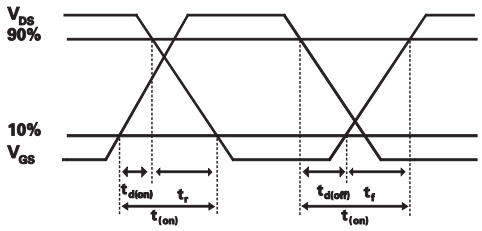
Gate-Source Voltage v Gate Charge



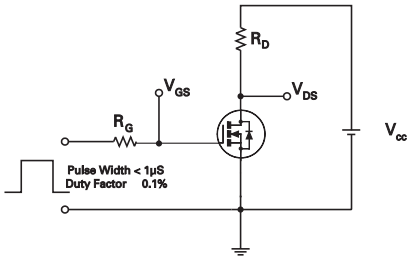
Basic Gate Charge Waveform



Gate Charge Test Circuit

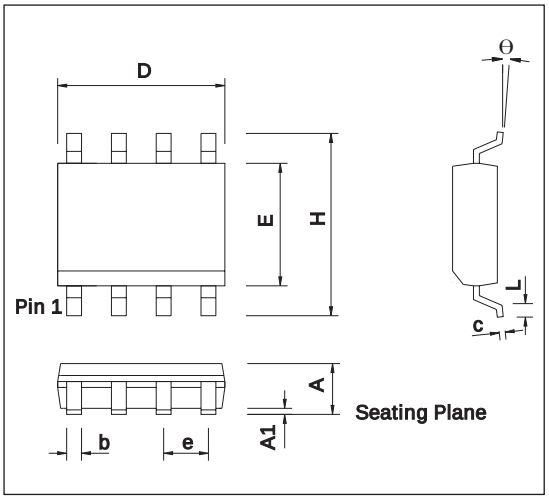


Switching Time Waveforms



Switching Time Test Circuit

PACKAGE OUTLINE



CONTROLLING DIMENSIONS ARE IN INCHES
APPROX IN MILLIMETRES

PACKAGE DIMENSIONS

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
D	0.189	0.197	4.80	5.00
H	0.228	0.244	5.80	6.20
E	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27
e	0.050 BSC		1.27 BSC	
b	0.013	0.020	0.33	0.51
c	0.008	0.010	0.19	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50