优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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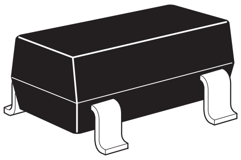
SUMMARY

$V_{(BR)DSS}$=30V : $R_{DS(on)}$=0.08Ω; I_D=3.5A

DESCRIPTION

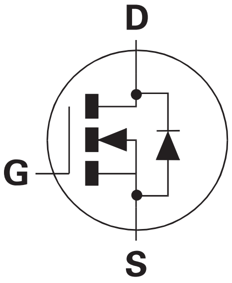
This new generation of Trench MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.



PACKAGE

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- SOT23 package



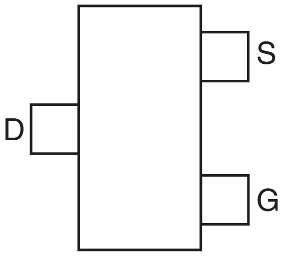
APPLICATIONS

- DC-DC converters
- Power management functions
- Disconnect switches
- Motor control

ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
NK-ZXMN3B14FTA	7″	8mm	3,000 units
NK-ZXMN3B14FTC	13″	8mm	10,000 units

PINOUT



DEVICE MARKING

- 3B4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current @ V_{GS}= 4.5V; T_A=25°C (b) @ V_{GS}= 4.5V; T_A=70°C (b) @ V_{GS}= 4.5V; T_A=25°C (a)	I_D	3.5 2.9 2.9	A A A
Pulsed Drain Current (c)	I_{DM}	16	A
Continuous Source Current (Body Diode) (b)	I_S	2.4	A
Pulsed Source Current (Body Diode) (c)	I_{SM}	16	A
Power Dissipation at T_A =25°C (a) Linear Derating Factor	P_D	1 8	W mW/°C
Power Dissipation at T_A =25°C (b) Linear Derating Factor	P_D	1.5 12	W mW/°C
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)	$R_{\Theta JA}$	125	°C/W
Junction to Ambient (b)	$R_{\Theta JA}$	83	°C/W

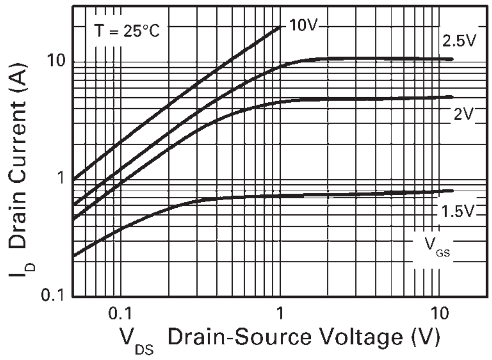
NOTES

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

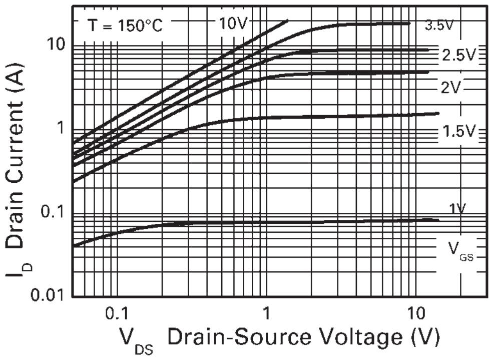
(b) For a device surface mounted on FR4 PCB measured at t ≤ 5 sec.

(c) Repetitive rating - 25mm x 25mm FR4 PCB, D=0.02, pulse width 300µs - pulse width limited by maximum junction temperature.

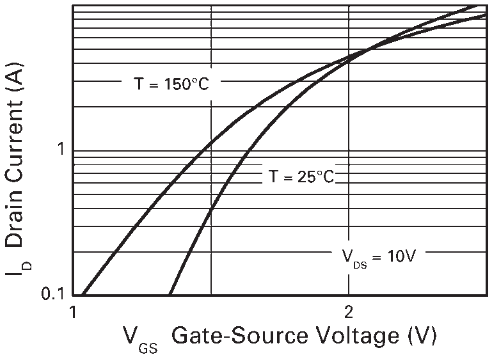
TYPICAL CHARACTERISTICS



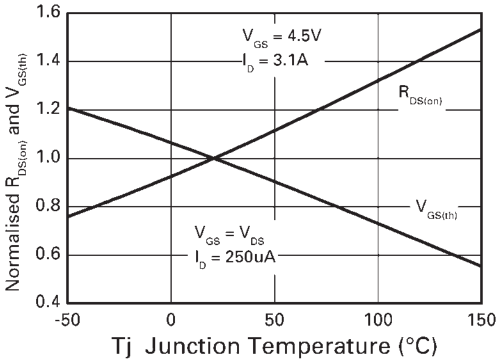
Output Characteristics



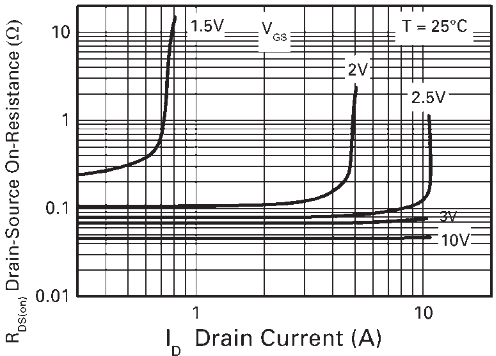
Output Characteristics



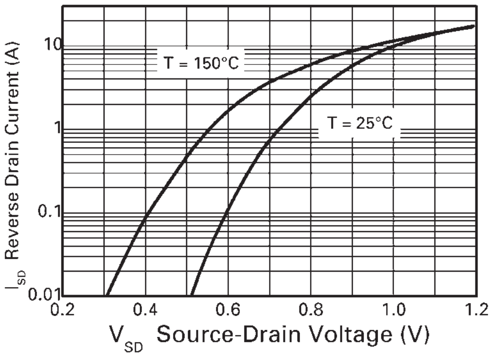
Typical Transfer Characteristics



Normalised Curves v Temperature



On-Resistance v Drain Current



Source-Drain Diode Forward Voltage

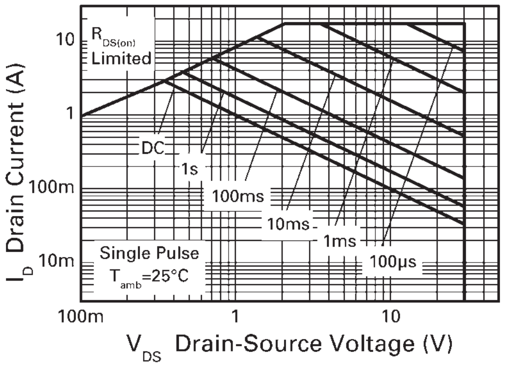
ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	30			V	I_D= 250µA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			1	µA	V_{DS}= 30V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±12V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.7			V	I_D= 250µA, V_{DS}=V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.080 0.140	Ω Ω	V_{GS}= 4.5V, I_D= 3.1A V_{GS}= 2.5V, I_D= 2.2A
Forward Transconductance (1) (3)	g_{fs}		8.5		S	V_{DS}= 15V, I_D= 3.1A
DYNAMIC (3)						
Input Capacitance	C_{iss}		568		pF	V_{DS}= 15V, V_{GS}=0V f=1MHz
Output Capacitance	C_{oss}		101		pF	
Reverse Transfer Capacitance	C_{rss}		66		pF	
SWITCHING(2) (3)						
Turn-On-Delay Time	$t_{d(on)}$		3.6		ns	V_{DD}= 15V, V_{GS}= 4.5V I_D= 1A R_G ≅ 6.0Ω
Rise Time	t_r		4.9		ns	
Turn-Off Delay Time	$t_{d(off)}$		17.3		ns	
Fall Time	t_f		9.8		ns	
Total Gate Charge	Q_g		6.7		nC	V_{DS}= 15V, V_{GS}= 4.5V I_D= 3.1A
Gate-Source Charge	Q_{gs}		1.4		nC	
Gate Drain Charge	Q_{gd}		1.8		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}		0.82	0.95	V	T_j=25°C, I_S= 3.1A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		10.8		ns	T_j=25°C, I_F= 1.6A, di/dt=100A/µs
Reverse Recovery Charge (3)	Q_{rr}		4.54		nC	

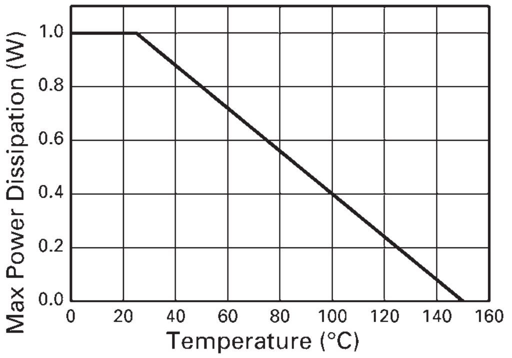
NOTES

(1) Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

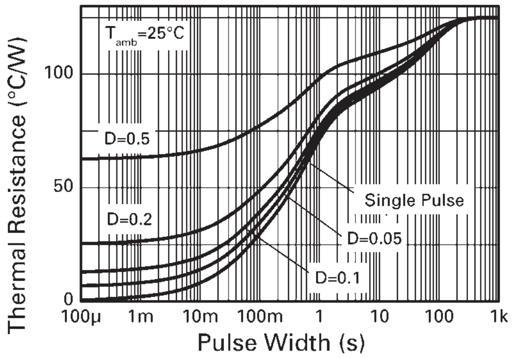
N-CHANNEL TYPICAL CHARACTERISTICS



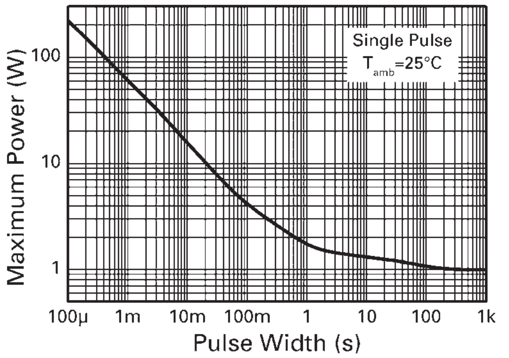
Safe Operating Area



Derating Curve

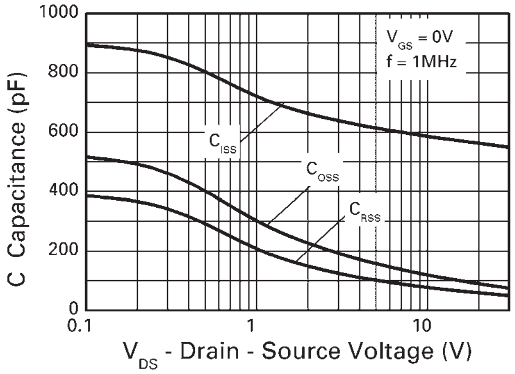


Transient Thermal Impedance

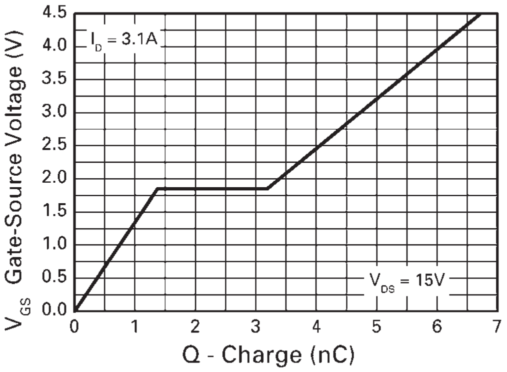


Pulse Power Dissipation

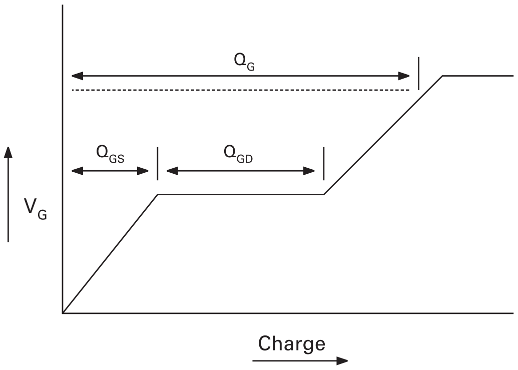
N-CHANNEL TYPICAL CHARACTERISTICS



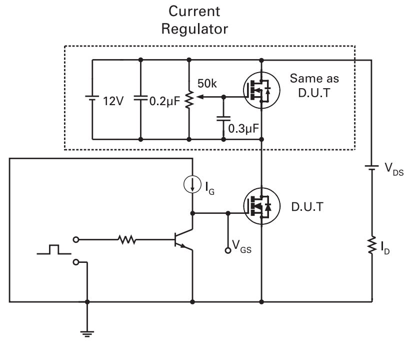
Capacitance v Drain-Source Voltage



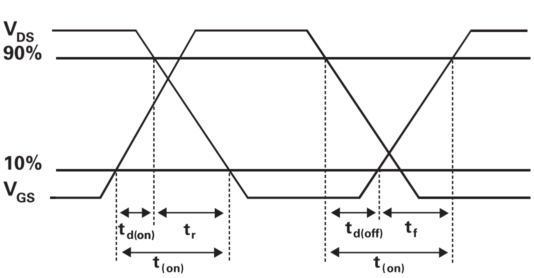
Gate-Source Voltage v Gate Charge



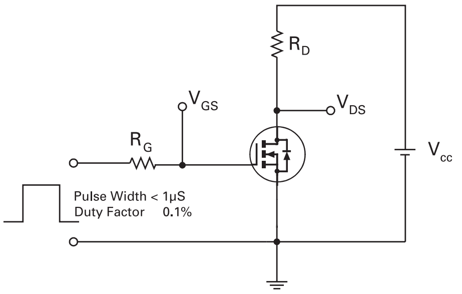
Basic Gate Charge Waveform



Gate Charge Test Circuit

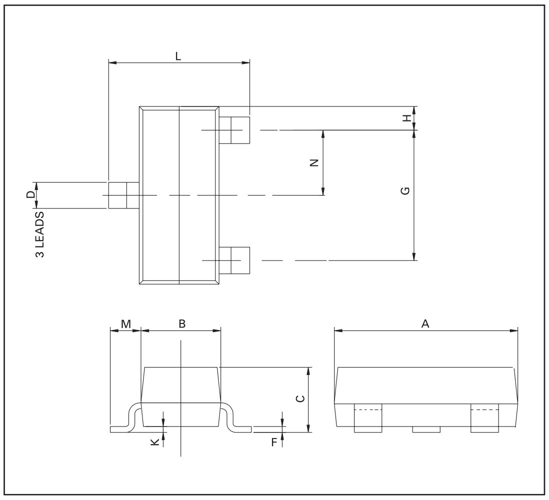


Switching Time Waveforms

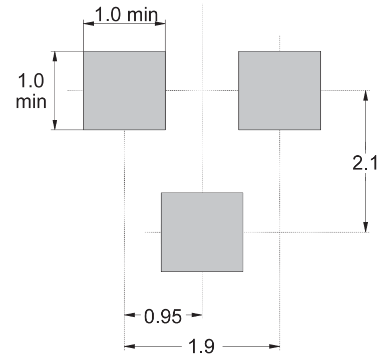


Switching Time Test Circuit

PACKAGE OUTLINE



PAD LAYOUT



SOT23 pattern.
Minimum Pad Size (dimensions in mm)

Controlling dimensions are in millimetres. Approximate conversions are given in inches

PACKAGE DIMENSIONS

DIM	MILLIMETRES		INCHES		DIM	MILLIMETRES		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	2.67	3.05	0.105	0.120	H	0.33	0.51	0.013	0.020
B	1.20	1.40	0.047	0.055	K	0.01	0.10	0.0004	0.004
C	—	1.10	—	0.043	L	2.10	2.50	0.083	0.0985
D	0.37	0.53	0.015	0.021	M	0.45	0.64	0.018	0.025
F	0.085	0.15	0.0034	0.0059	N	0.95 NOM		0.0375 NOM	
G	1.90 NOM		0.075 NOM		Θ	10° TYP		10° TYP	