优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Summary

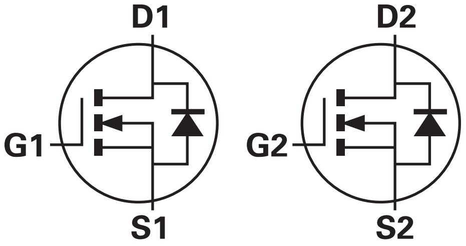
$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.024 @ V_{GS}= 10V	7.3
	0.039 @ V_{GS}= 4.5V	5.7

Description

This new generation Trench MOSFET from Zetex features low on-resistance achievable with 4.5V gate drive.

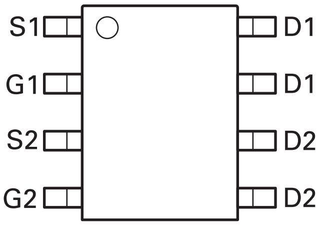
Features

- Low on-resistance
- 4.5V gate drive capability



Applications

- DC-DC Converters
- Power management functions
- Load switching
- Motor control
- Back lighting



Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
NK-ZXMN3F31DN8TA	7	12	500

Device marking

NK-ZXMN

3F31D

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	30	V
Gate source voltage	V_{GS}	±20	V
Continous Drain Current @ V_{GS}=10; T_A=25°C(b) @ V_{GS}=10; T_A=70°C(b) @ V_{GS}=10; T_A=25°C(a)	I_D	7.3 5.9 5.7	A A A
Pulsed drain current(c)	I_{DM}	33	A
Continuous source current (body diode)(b)	I_S	3.5	A
Pulsed source current (body diode)(c)	I_{SM}	33	A
Power dissipation at T_A =25°C(a)(d) Linear derating factor	P_D	1.25 10	W mW/°C
Power dissipation at T_A =25°C(a)(e) Linear derating factor	P_D	1.8 14	W mW/°C
Power dissipation at T_A =25°C(b)(d) Linear derating factor	P_D	2.1 17	W mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	°C

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient(a)(d)	$R_{\Theta JA}$	100	°C/W
Junction to ambient(a)(e)	$R_{\Theta JA}$	70	°C/W
Junction to ambient(b)(d)	$R_{\Theta JA}$	60	°C/W
Junction to lead(f)	$R_{\Theta JL}$	53	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

(b) For a device surface mounted on FR4 PCB measured at t ≤ 10 sec.

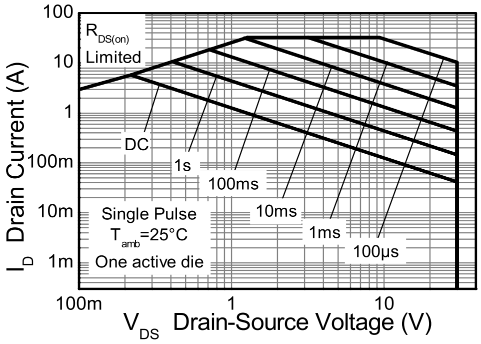
(c) Repetitive rating - 25mm x 25mm FR4 PCB, D=0.02, pulse width 300µs - pulse width limited by maximum junction temperature.

(d) For a dual device with one active die.

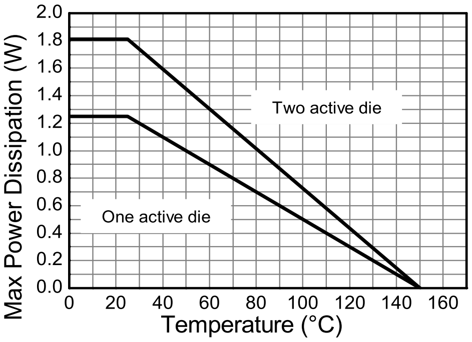
(e) For a device with two active die running at equal power.

(f) Thermal resistance from junction to solder-point (at end of drain lead).

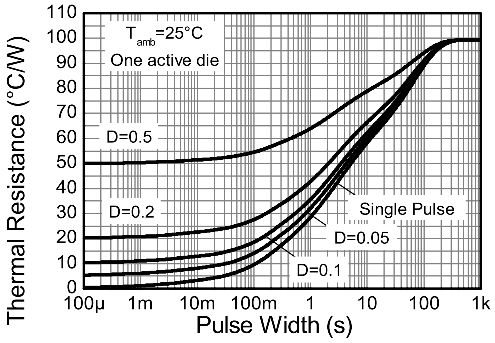
Thermal characteristics



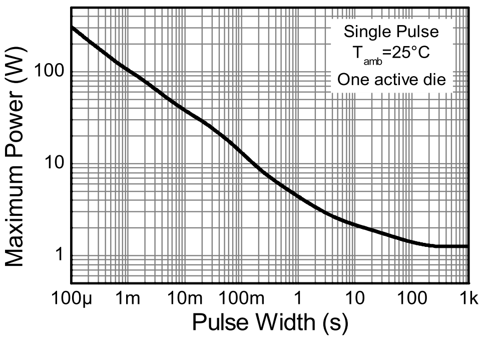
Safe Operating Area



Derating Curve



Transient Thermal Impedance



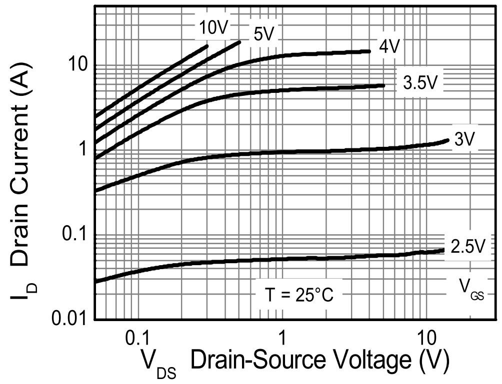
Pulse Power Dissipation

Electrical characteristics (at T_{amb} = 25°C unless otherwise stated)

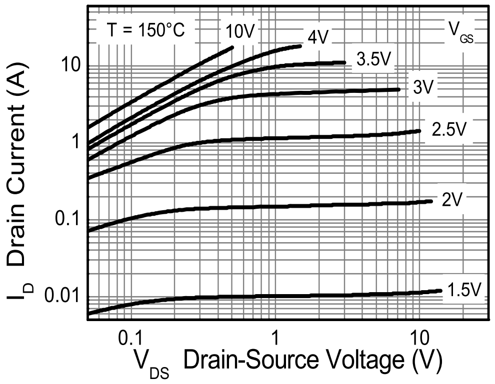
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	30			V	I_D= 250μA, V_{GS}=0V
Zero Gate voltage drain current	I_{DSS}			0.5	μA	V_{DS}= 30V, V_{GS}=0V
Gate-Body leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	I_D= 250μA, V_{DS}=V_{GS}
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.024 0.039	Ω Ω	V_{GS}= 10V, I_D= 7.0A V_{GS}= 4.5V, I_D= 6.0A
Forward transconductance(*)(†)	g_{fs}		16.5		S	V_{DS}= 15V, I_D= 7A
Dynamic (†)						
Input capacitance	C_{iss}		608		pF	V_{DS}= 15V, V_{GS}=0V f=1MHz
Output capacitance	C_{oss}		132		pF	
Reverse transfer capacitance	C_{rss}		71		pF	
Switching (‡)(†)						
Turn-on-delay time	$t_{d(on)}$		2.9		ns	V_{DD}= 15V, I_D= 1A R_G ≅ 6.0Ω, V_{GS}=10V
Rise time	t_r		3.3		ns	
Turn-off delay time	$t_{d(off)}$		16		ns	
Fall time	t_f		8		ns	
Total gate charge	Q_g		12.9		nC	V_{DS}= 15V, V_{GS}= 10V I_D= 7A
Gate-source charge	Q_{gs}		2.5		nC	
Gate drain charge	Q_{gd}		2.52		nC	
Source-drain diode						
Diode Forward Voltage(*)	V_{SD}		0.82	1.2	V	T_j=25°C, I_S= 1.7A, V_{GS}=0V
Reverse recovery time(†)	t_{rr}		12		ns	T_j=25°C, I_S=2.2A di/dt=100A/μs
Reverse recovery charge(†)	Q_{rr}		4.8		nC	

NOTES:
(*) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤2%.
(†) For design aid only, not subject to production testing
(‡) Switching characteristics are independent of operating junction temperature.

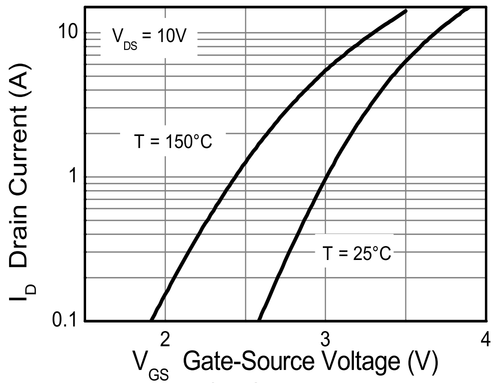
Typical characteristics



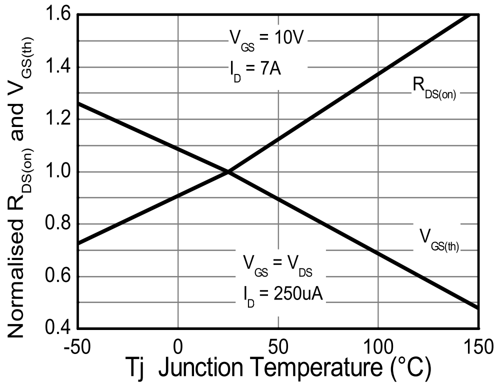
Output Characteristics



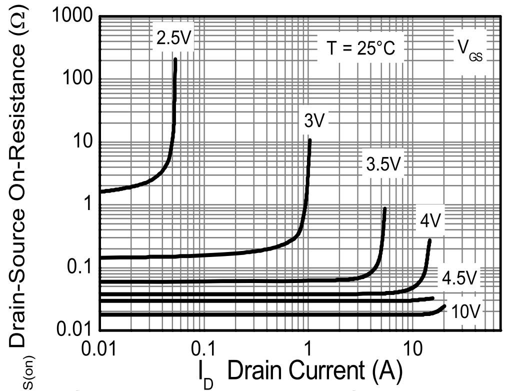
Output Characteristics



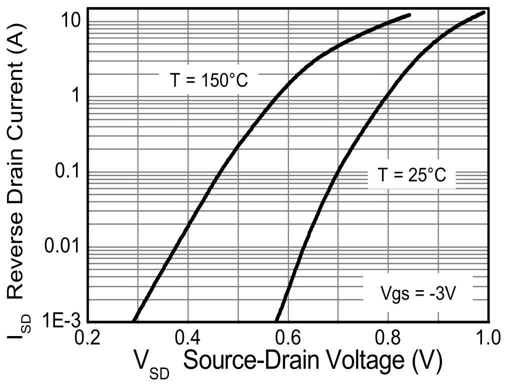
Typical Transfer Characteristics



Normalised Curves v Temperature

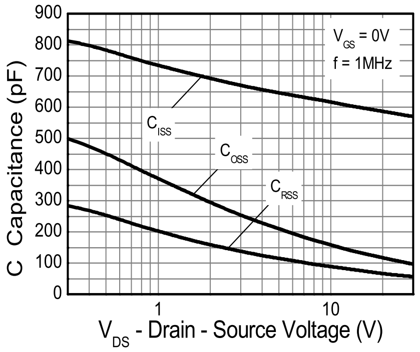


On-Resistance v Drain Current

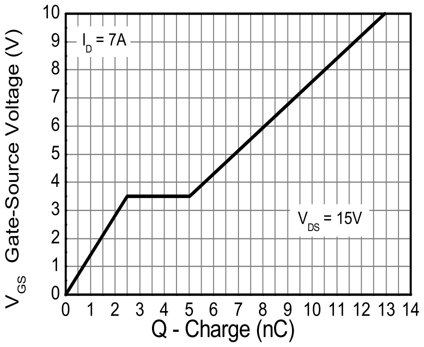


Source-Drain Diode Forward Voltage

Typical characteristics

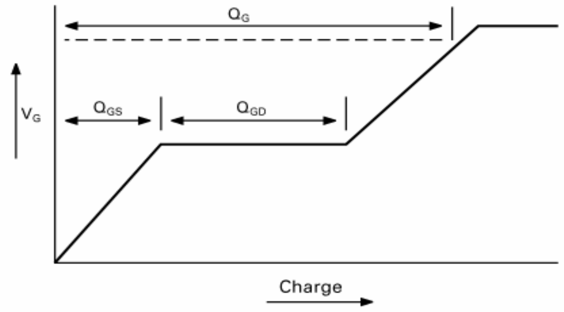


Capacitance v Drain-Source Voltage

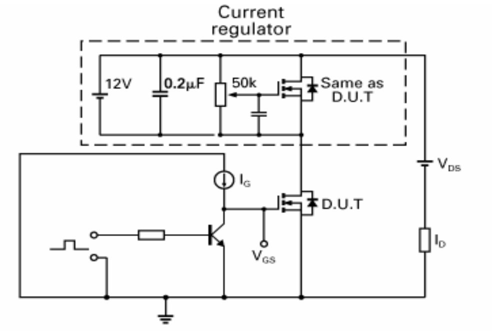


Gate-Source Voltage v Gate Charge

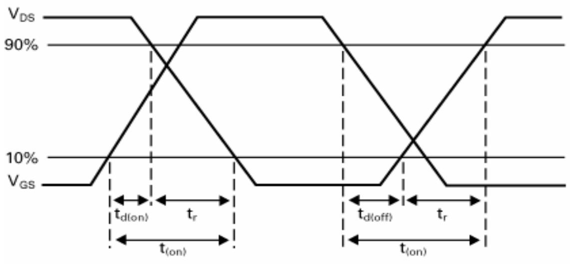
Test circuits



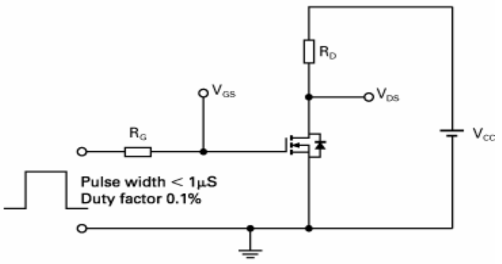
Basic gate charge waveform



Gate charge test circuit

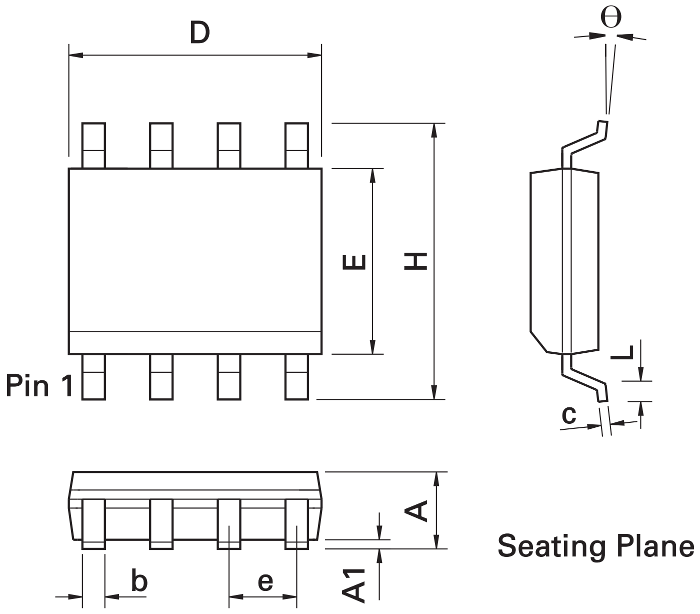


Switching time waveforms



Switching time test circuit

Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	Θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters