



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638

ysbdt@szyoushang.cn

www.szyoushang.cn



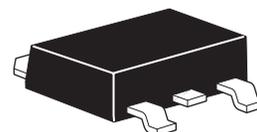
企业微信二维码



企业QQ二维码

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.050 @ $V_{GS}= 10V$	10.7
	0.070 @ $V_{GS}= 4.5V$	9



Description

This new generation trench MOSFET from Zetex features a unique structure combining the benefits of low on-resistance and fast switching, making it ideal for high efficiency power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low gate drive
- DPAK package

Applications

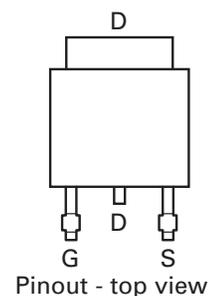
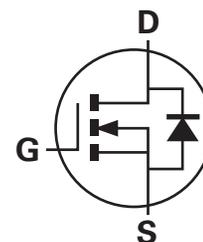
- DC-DC converters
- Power management functions
- Disconnect switches
- Motor control

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
NK-ZXMN6A25KTC	13	16	2,500

Device marking

NK-ZXMN
6A25



Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS} = 10V$; $T_{amb} = 25^{\circ}C^{(b)}$	I_D	10.7	A
@ $V_{GS} = 10V$; $T_{amb} = 70^{\circ}C^{(b)}$		8.6	A
@ $V_{GS} = 10V$; $T_{amb} = 25^{\circ}C^{(a)}$		7	A
Pulsed drain current ^(c)	I_{DM}	36	A
Continuous source current (body diode) ^(b)	I_S	11.8	A
Pulsed source current (body diode) ^(c)	I_{SM}	36	A
Power dissipation at $T_{amb} = 25^{\circ}C^{(a)}$	P_D	4.25	W
Linear derating factor		34	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(b)}$	P_D	9.85	W
Linear derating factor		78.7	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(d)}$	P_D	2.11	W
Linear derating factor		16.8	mW/ $^{\circ}C$
Operating and storage temperature range	T_{j}, T_{stg}	-55 to +150	$^{\circ}C$

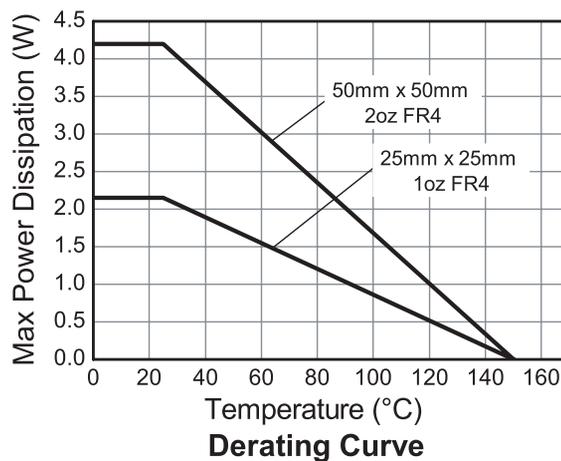
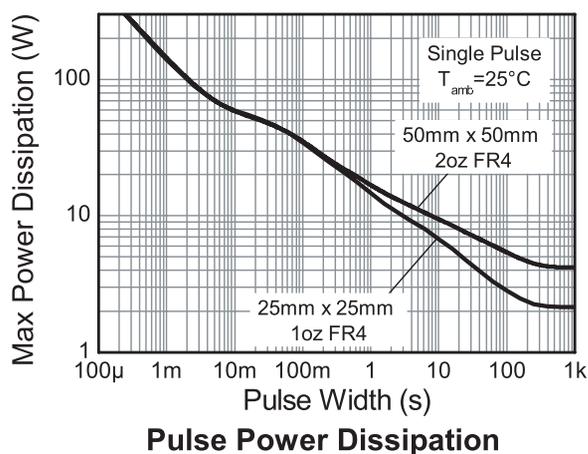
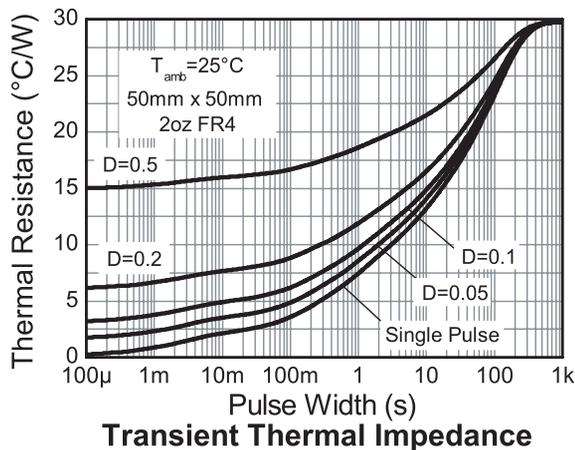
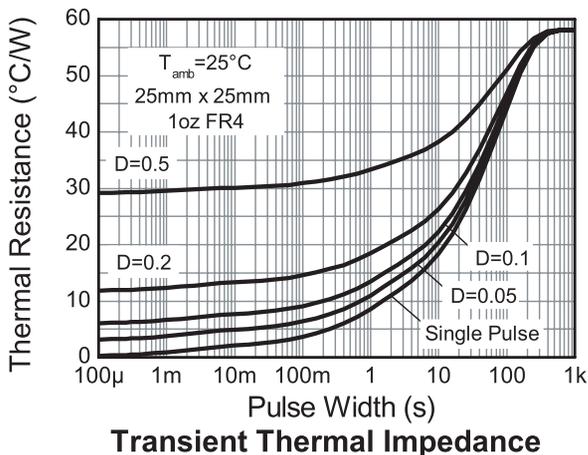
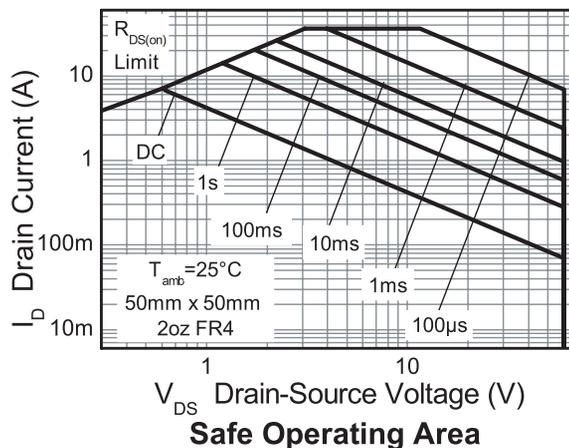
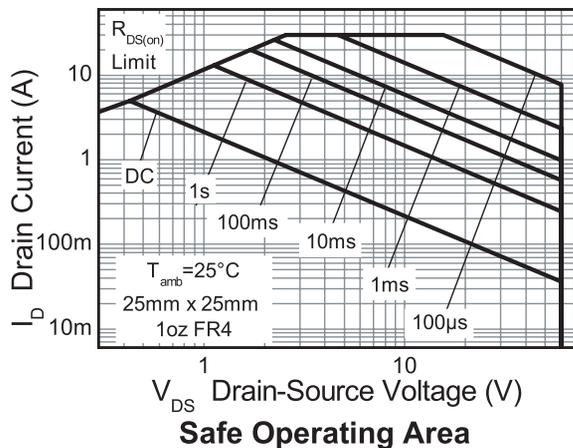
Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	29.4	$^{\circ}C/W$
Junction to ambient ^(b)	$R_{\theta JA}$	12.7	$^{\circ}C/W$
Junction to ambient ^(d)	$R_{\theta JA}$	59.1	$^{\circ}C/W$

NOTES:

- (a) For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating 50mm x 50mm x 1.6mm FR4 PCB, $D=0.02$ pulse width=300 μs - pulse width limited by maximum junction temperature.
- (d) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz. copper, in still air conditions.

Thermal characteristics



Electrical characteristics (at $T_{amb} = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	60			V	$I_D = 250\mu A, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}			1.0	μA	$V_{DS} = 60V, V_{GS} = 0V$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Gate-source threshold voltage	$V_{GS(th)}$	1		3	V	$I_D = 250\mu A, V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.050	Ω	$V_{GS} = 10V, I_D = 3.6A$
				0.070	Ω	$V_{GS} = 4.5V, I_D = 3.0A$
Forward transconductance ^{(*)(‡)}	g_{fs}		10.2		S	$V_{DS} = 15V, I_D = 4.5A$
Dynamic^(‡)						
Input capacitance	C_{iss}		1063		pF	$V_{DS} = 30V, V_{GS} = 0V$ $f = 1MHz$
Output capacitance	C_{oss}		104		pF	
Reverse transfer capacitance	C_{rss}		64		pF	
Switching^{(†) (‡)}						
Turn-on-delay time	$t_{d(on)}$		3.8		ns	$V_{DD} = 30V, I_D = 1A$ $R_G = 6.0\Omega, V_{GS} = 10V$
Rise time	t_r		4.0		ns	
Turn-off delay time	$t_{d(off)}$		26.2		ns	
Fall time	t_f		10.6		ns	
Gate charge	Q_g		11.0		nC	$V_{DS} = 30V, V_{GS} = 5V$ $I_D = 1.4A$
Total gate charge	Q_g		20.4		nC	$V_{DS} = 30V, V_{GS} = 10V$ $I_D = 1.4A$
Gate-source charge	Q_{gs}		4.1		nC	
Gate drain charge	Q_{gd}		5.1		nC	
Source-drain diode						
Diode forward voltage ^(*)	V_{SD}		0.85	0.95	V	$T_j = 25^{\circ}C, I_S = 5.5A,$ $V_{GS} = 0V$
Reverse recovery time ^(‡)	t_{rr}		22.0		ns	$T_j = 25^{\circ}C, I_S = 2.2A,$ $di/dt = 100A/\mu s$
Reverse recovery charge ^(‡)	Q_{rr}		21.4		nC	

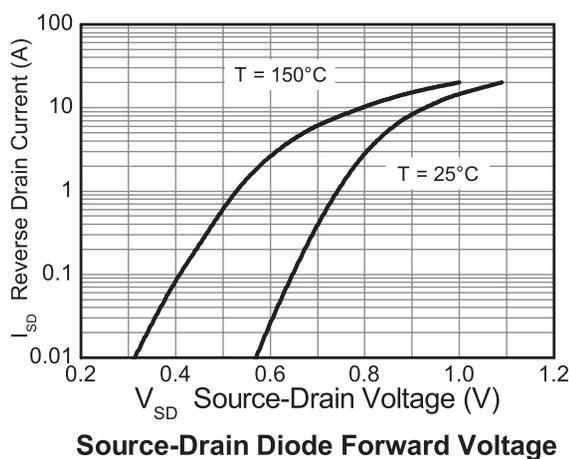
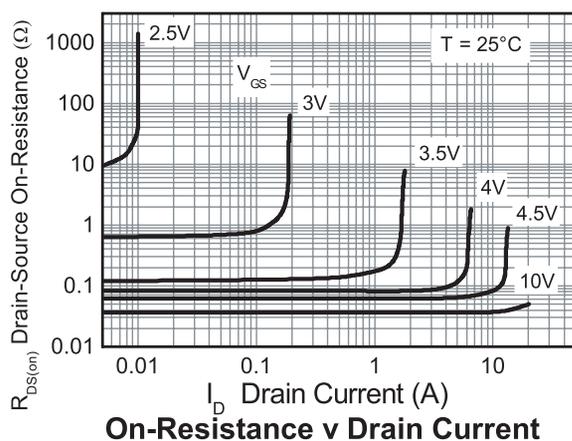
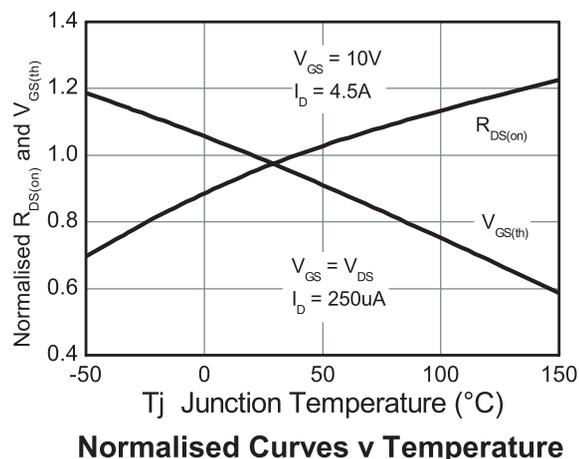
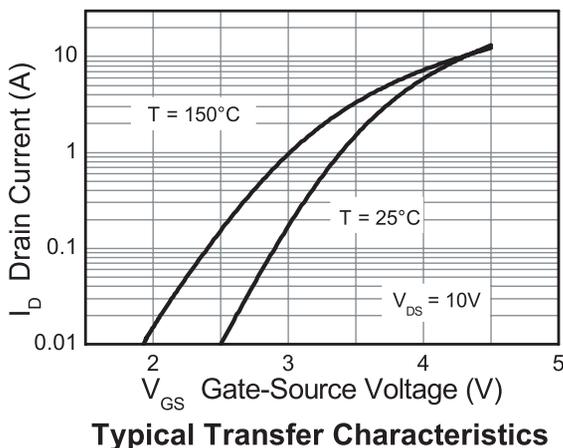
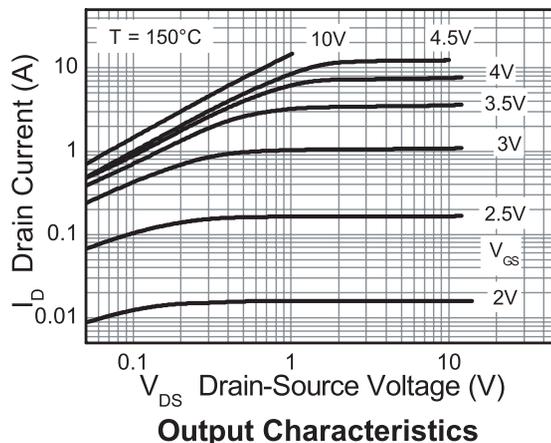
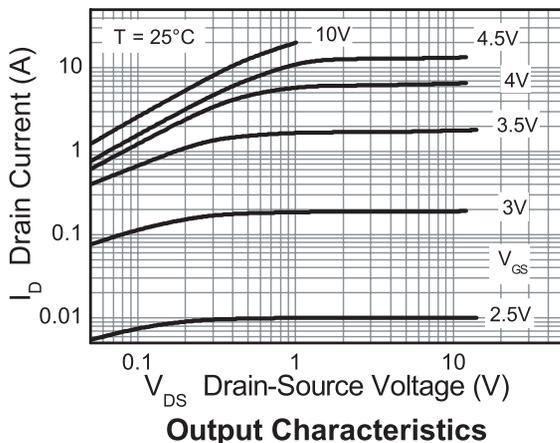
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

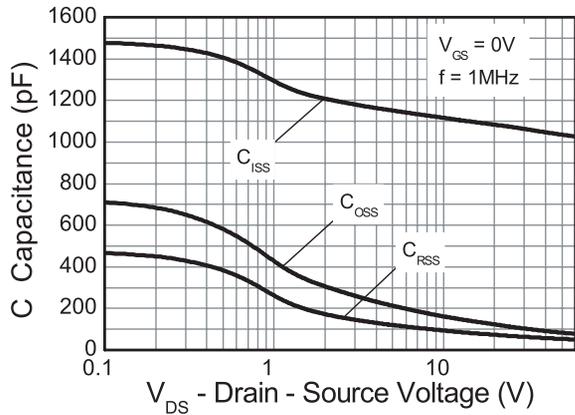
(†) Switching characteristics are independent of operating junction temperature

(‡) For design aid only, not subject to production testing.

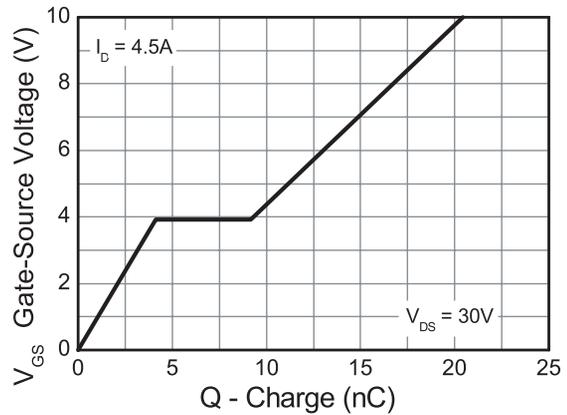
Typical characteristics



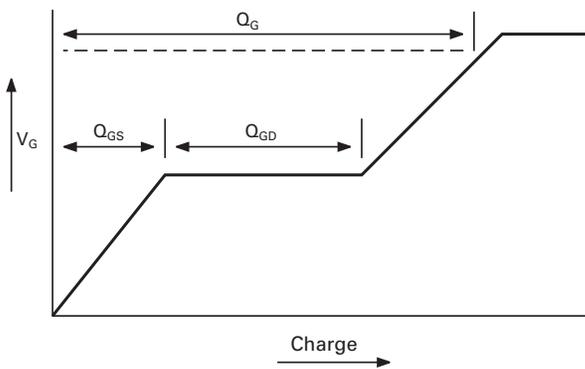
Typical characteristics



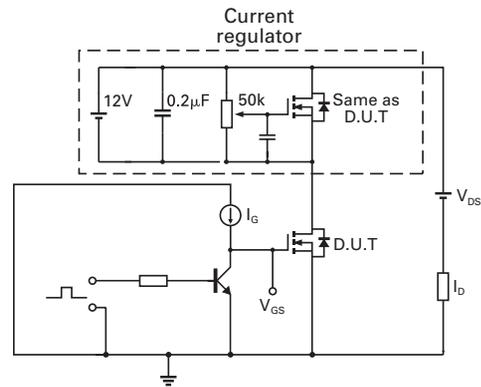
Capacitance v Drain-Source Voltage



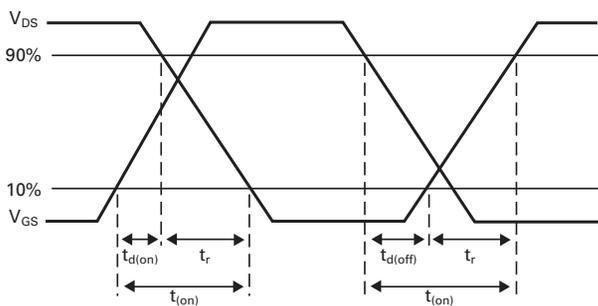
Gate-Source Voltage v Gate Charge



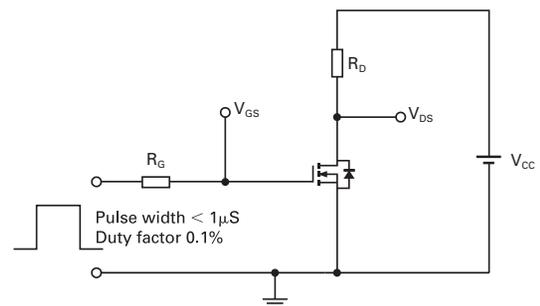
Basic gate charge waveform



Gate charge test circuit

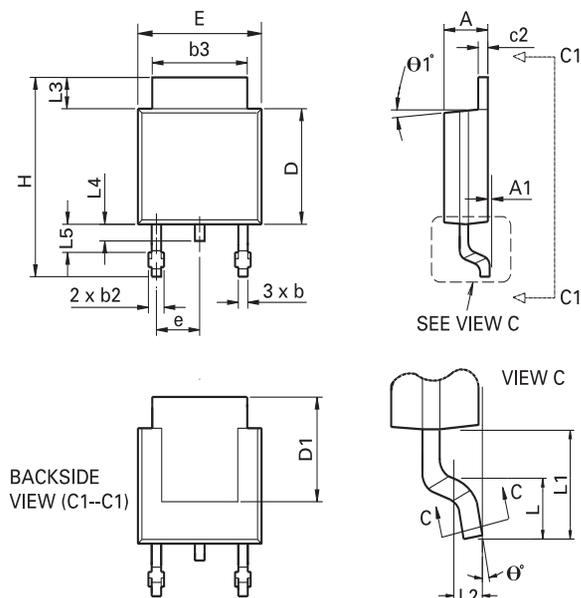


Switching time waveforms



Switching time test circuit

Package outline - DPAK



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.086	0.094	2.18	2.39	e	0.090 BSC		2.29 BSC	
A1	-	0.005	-	0.127	H	0.370	0.410	9.40	10.41
b	0.020	0.035	0.508	0.89	L	0.055	0.070	1.40	1.78
b2	0.030	0.045	0.762	1.14	L1	0.108 REF		2.74 REF	
b3	0.205	0.215	5.21	5.46	L2	0.020 BSC		0.508 BSC	
c	0.018	0.024	0.457	0.61	L3	0.035	0.065	0.89	1.65
c2	0.018	0.023	0.457	0.584	L4	0.025	0.040	0.635	1.016
D	0.213	0.245	5.41	6.22	L5	0.045	0.060	1.14	1.52
D1	0.205	-	5.21	-	θ_1°	0°	10°	0°	10°
E	0.250	0.265	6.35	6.73	θ°	0°	15°	0°	15°
E1	0.170	-	4.32	-	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters