优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_C = +25°C
-100V	150mΩ @ V_{GS} = -10V	-15A
	190mΩ @ V_{GS} = -6V	-14A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- Low Gate Drive

Description and Applications

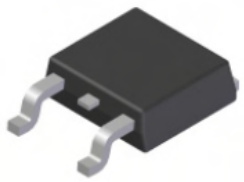
This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- DC-DC converters
- Power management functions
- Disconnect switches
- Motor controls

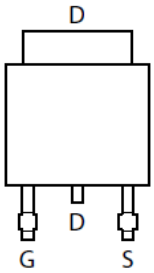
Mechanical Data

- Package: TO252
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals Connections: See Diagram Below
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.315 grams (Approximate)

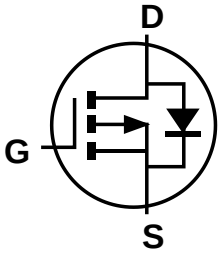
TO252 (DPAK)



Top View



Top View
Pin Out



Equivalent Circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = -10V	T_C = +25°C T_C = +70°C	I_D	-15 -12	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)		I_{DM}	-32	A
Maximum Continuous Body Diode Forward Current (Note 5)		I_S	-15	A
Pulsed Source Current (10μs Pulse, Duty Cycle = 1%)		I_{SM}	-32	A
Avalanche Current, L = 1mH		I_{AS}	-12.5	A
Avalanche Energy, L = 1mH		E_{AS}	78	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	38	°C/W
Total Power Dissipation	P_D	3.3	W
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	1.75	°C/W
Total Power Dissipation	P_D	71	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-100	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -100V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-2	—	-4	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	— —	92 109	150 190	mΩ	V_{GS} = -10V, I_D = -2.8A V_{GS} = -6V, I_D = -2.4A
Diode Forward Voltage	V_{SD}	—	-0.8	-0.95	V	V_{GS} = 0V, I_S = -3.5A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1055	—	pF	V_{DS} = -50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	90	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	76	—	pF	
Turn-On Delay Time	$t_{D(ON)}$	—	4.9	—	ns	V_{DS} = -50V, V_{GS} = -10V I_D = -1A, R_G = 6Ω
Rise Time	t_R	—	6.8	—		
Turn-On Delay Time	$t_{D(OFF)}$	—	33.9	—		
Rise Time	t_F	—	17.9	—		
Total Gate Charge	Q_g	—	26.9	—	nC	V_{DS} = -50V, V_{GS} = -10V I_D = -2.8A
Gate-Source Charge	Q_{gs}	—	3.9	—		
Gate-Drain Charge	Q_{gd}	—	10.2	—		
Reverse Recovery Time	t_{RR}	—	49	—	ns	I_S = -2.8A, dI/dt = 100A/μs
Reverse Recovery Charge	Q_{RR}	—	107	—	nC	

Notes: 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

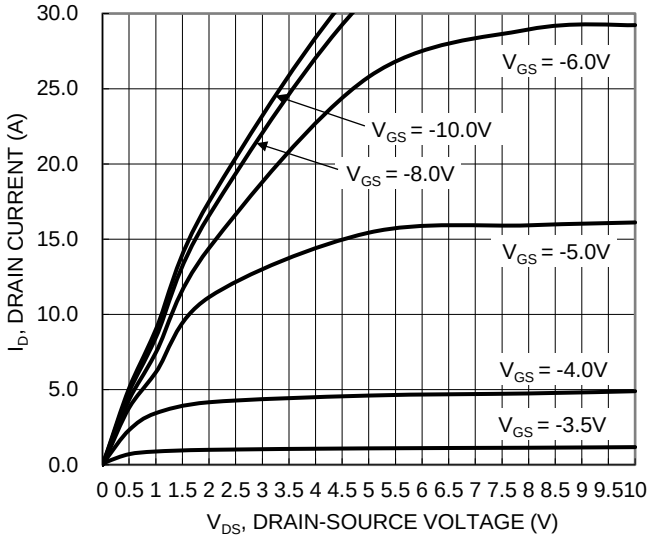


Figure 1. Typical Output Characteristic

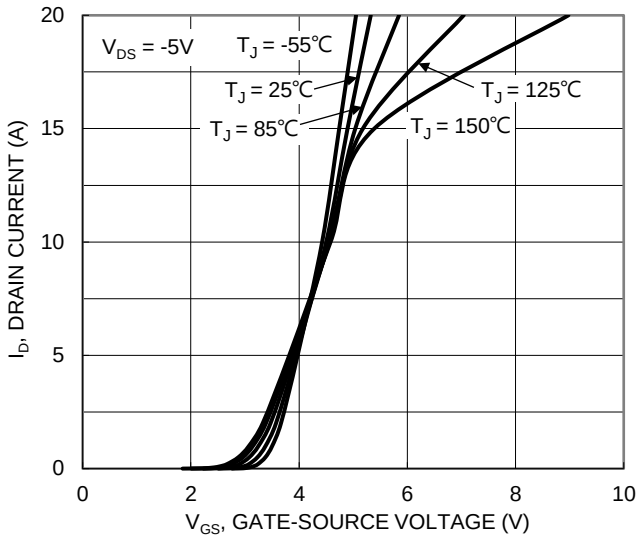


Figure 2. Typical Transfer Characteristic

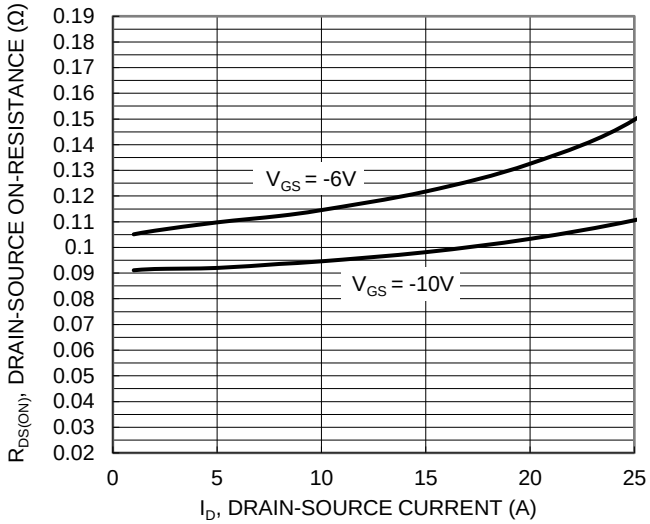


Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage

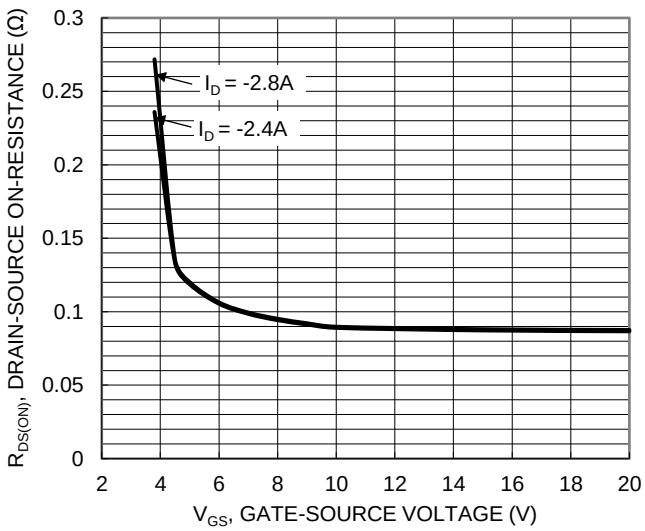


Figure 4. Typical Transfer Characteristic

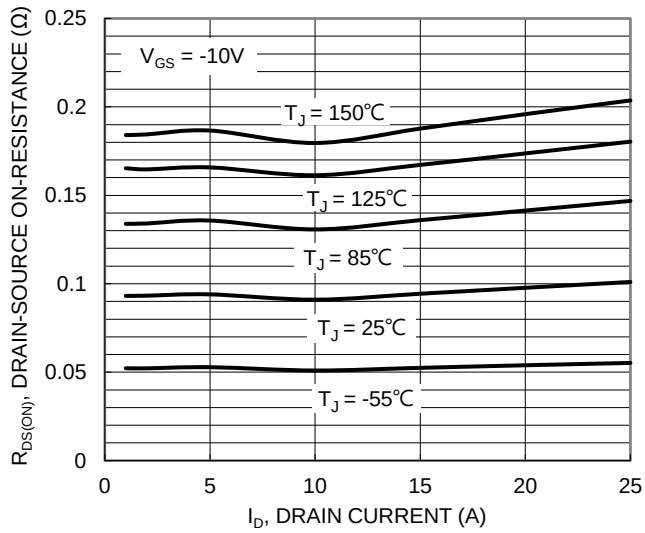


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

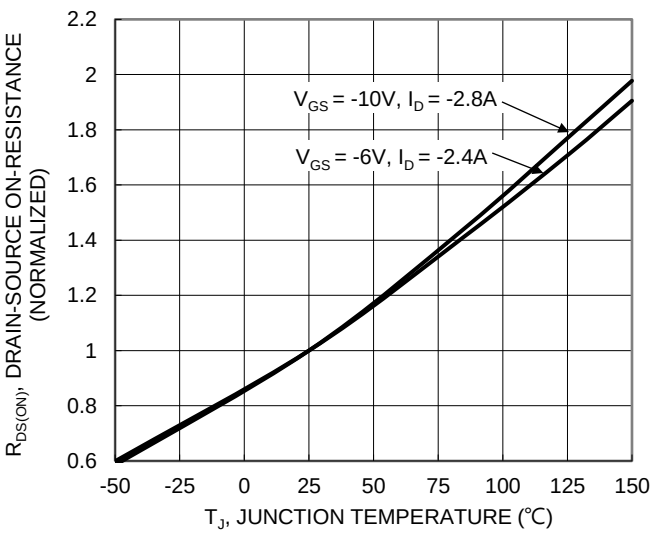


Figure 6. On-Resistance Variation with Junction Temperature

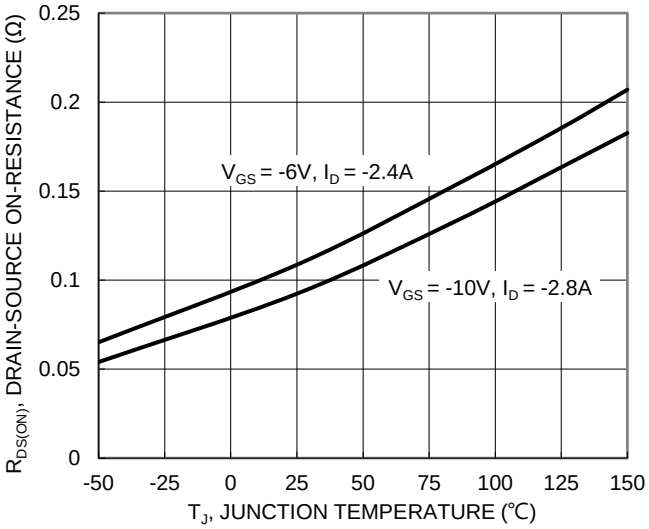


Figure 7. On-Resistance Variation with Junction Temperature

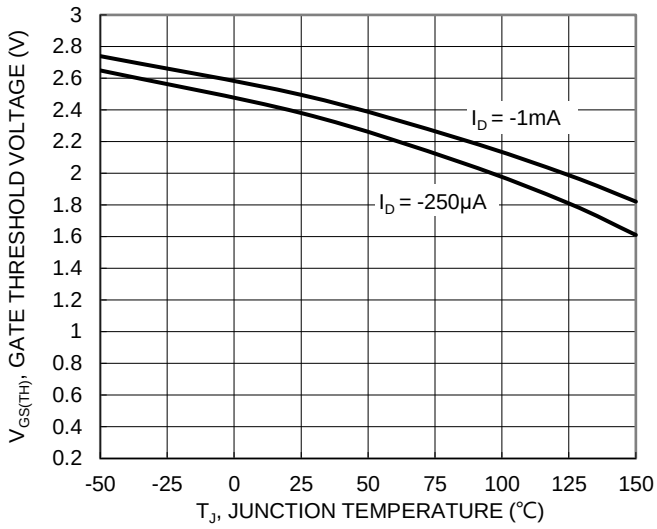


Figure 8. Gate Threshold Variation vs Junction Temperature

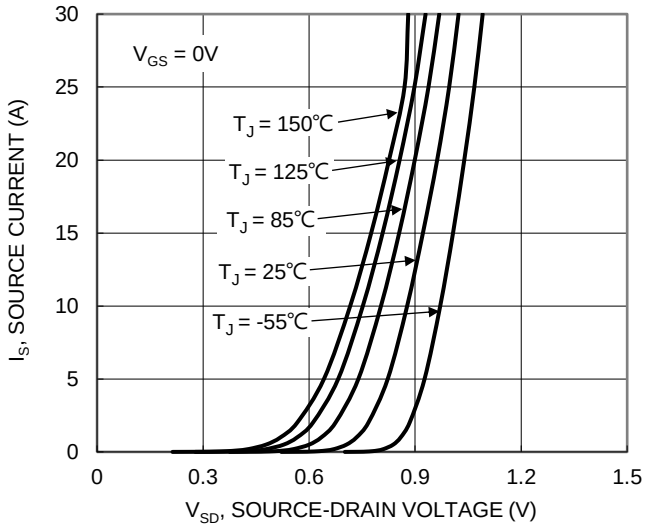


Figure 9. Diode Forward Voltage vs. Current

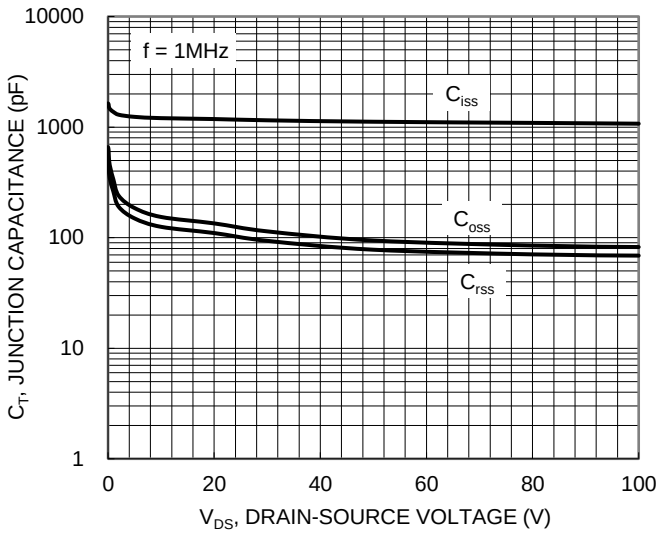


Figure 10. Typical Junction Capacitance

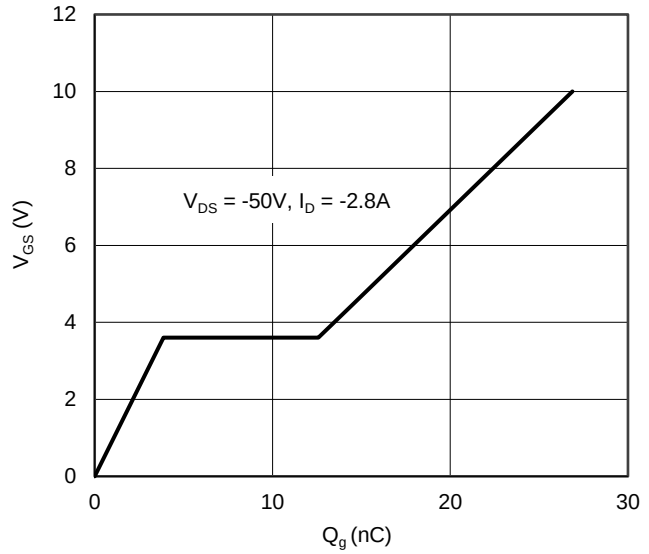


Figure 11. Gate Charge

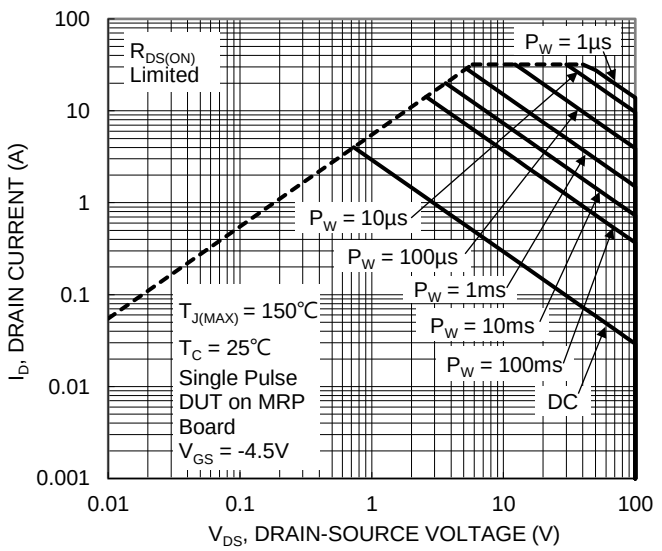


Figure 12. SOA, Safe Operation Area

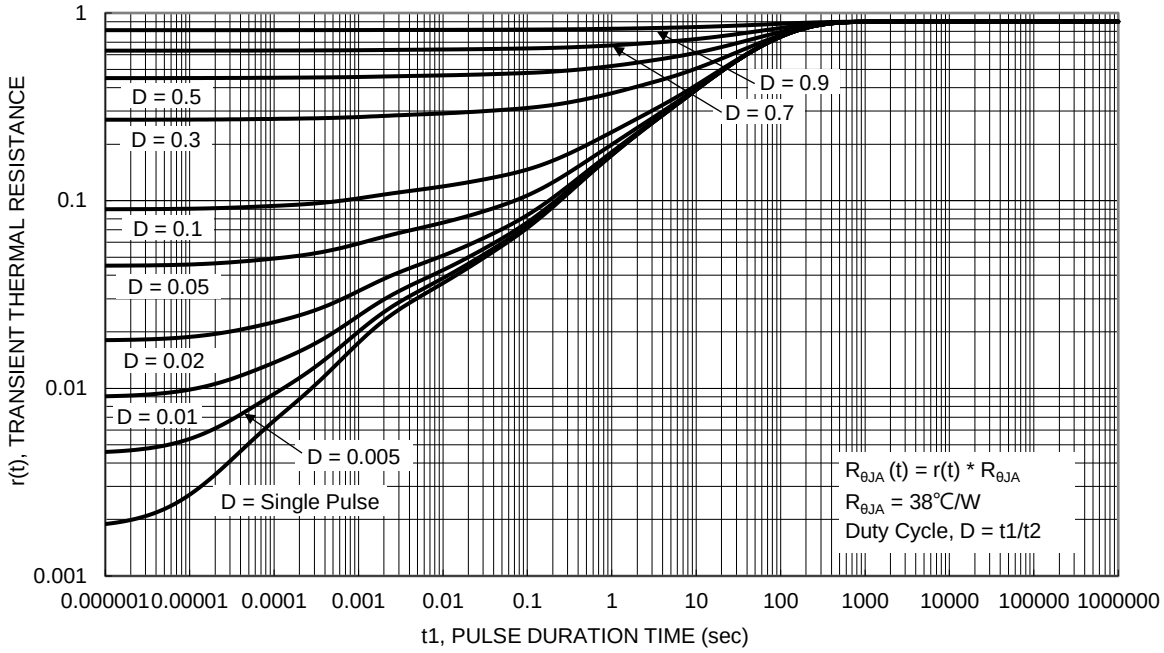
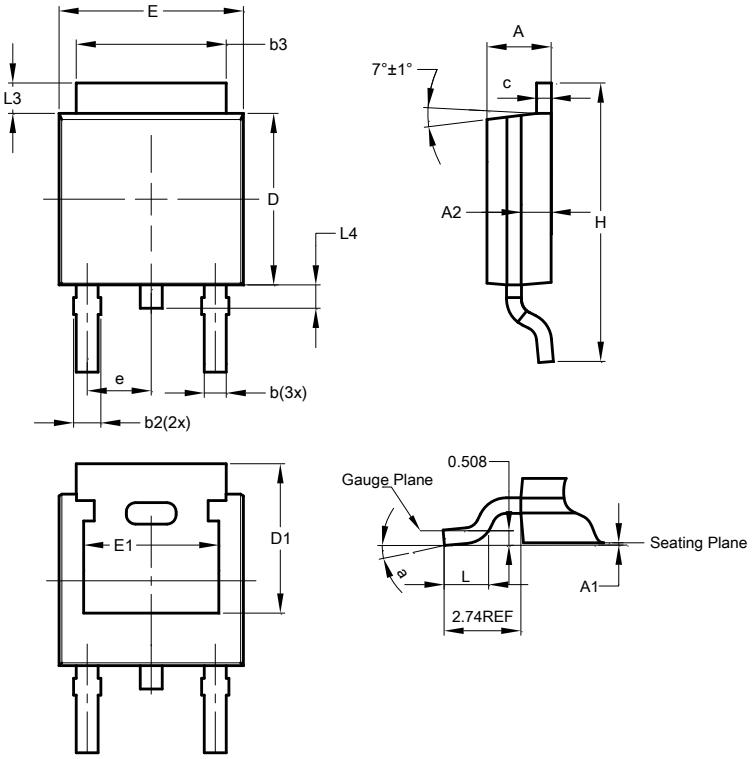


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

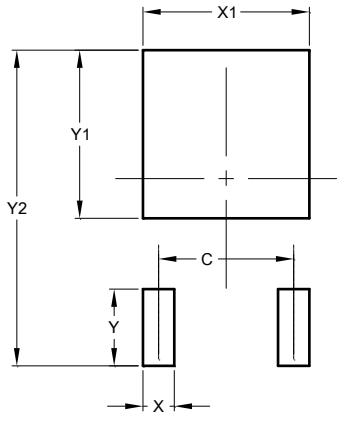
TO252 (DPAK)



TO252 (DPAK)			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.50	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	--	--
e	2.286 BSC		
E	6.45	6.70	6.58
E1	4.32	--	--
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	--
All Dimensions in mm			

Suggested Pad Layout

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700