



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638

ysbdt@szyoushang.cn

www.szyoushang.cn



企业微信二维码



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Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (mA)
-200	28 @ $V_{GS} = -10V$	-137

Description

This 200V enhancement mode P-channel MOSFET provides users with a competitive specification offering efficient power handling capability, high impedance and freedom from thermal runaway and thermally induced secondary breakdown.

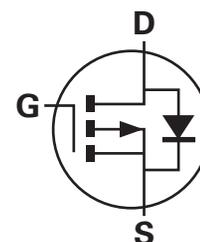
Applications benefiting from this device include a variety of telecom and general high voltage circuits.

Features

- High voltage
- Low on-resistance
- Fast switching speed
- Low gate drive
- Low threshold
- SOT23 FLAT package

Applications

- Active clamping of primary side MOSFETs in 48 volt DC-DC converters



Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	-200	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS}=10V$; $T_{amb}=25^{\circ}C^{(a)}$	I_D	-137	mA
Pulsed drain current ^(c)	I_{DM}	-0.8	A
Pulsed source current (body diode) ^(c)	I_{SM}	-0.8	A
Power dissipation at $T_{amb}=25^{\circ}C^{(a)}$	P_D	1	W
Linear derating factor		8	mW/ $^{\circ}C$
Power dissipation at $T_{amb}=25^{\circ}C^{(b)}$	P_D	1.5	W
Linear derating factor		12.3	mW/ $^{\circ}C$
Operating and storage temperature range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

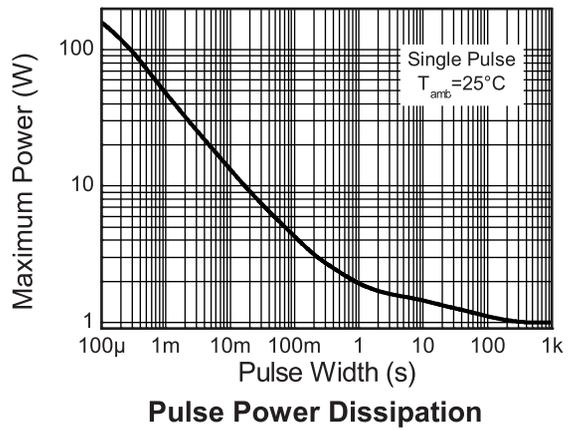
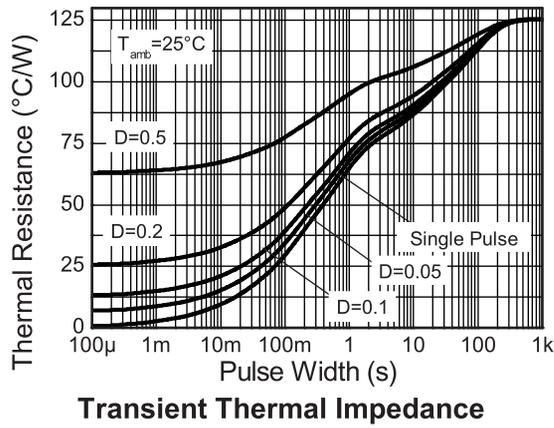
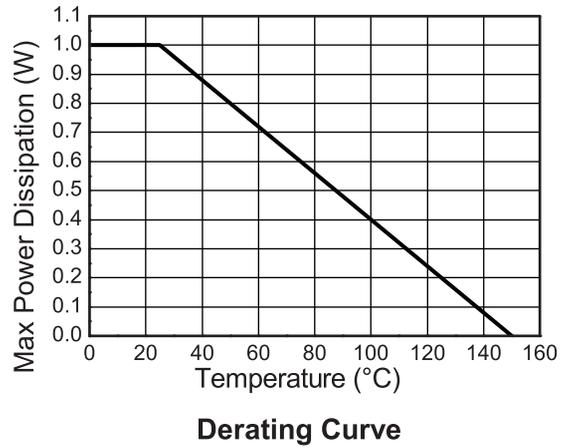
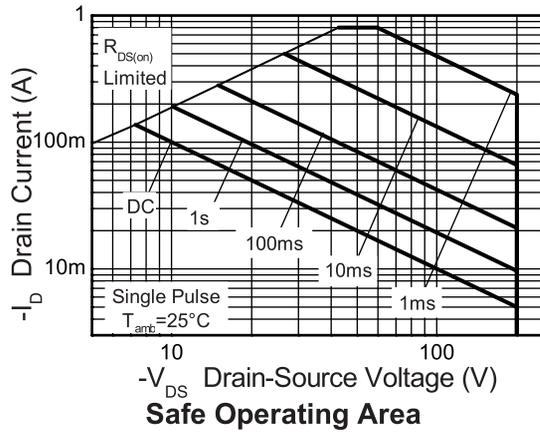
Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	125	$^{\circ}C/W$
Junction to ambient ^(b)	$R_{\theta JA}$	81	$^{\circ}C/W$

NOTES:

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 pcb measured at $t \leq 5$ sec.
- (c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μ s - pulse width limited by maximum junction temperature.

Thermal characteristics



Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Static					
Drain-source breakdown voltage	$V_{(BR)DSS}$	-200		V	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$
Zero gate voltage drain current	I_{DSS}		-10	μA	$V_{DS} = -200\text{V}, V_{GS} = 0\text{V}$
			-100	μA	$V_{DS} = -160\text{V}, V_{GS} = 0\text{V}, T = 125^{\circ}\text{C}^{(\ddagger)}$
Gate-body leakage	I_{GSS}		20	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
Gate-source threshold voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D = 250\mu\text{A}, V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$		28	Ω	$V_{GS} = -10\text{V}, I_D = -150\text{mA}$
On-state drain current ^(*)	$I_{D(on)}$	-300		mA	$V_{DS} = -25\text{V}, V_{GS} = -10\text{V}$
Forward transconductance ^(*) (\ddagger)	g_{fs}	50		mS	$V_{DS} = -25\text{V}, I_D = -150\text{mA}$
Dynamic^(\ddagger)					
Input capacitance	C_{iss}		100	pF	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		25	pF	
Reverse transfer capacitance	C_{rss}		7	pF	
Switching^(\ddagger) (\ddagger)					
Turn-on-delay time	$t_{d(on)}$		7	ns	$V_{DD} = -25\text{V}, V_{GS} = -10\text{V}$ $I_D = -150\text{mA}$ $R_{SOURCE} \approx 50\Omega$
Rise time	t_r		15	ns	
Turn-off delay time	$t_{d(off)}$		12	ns	
Fall time	t_f		15	ns	

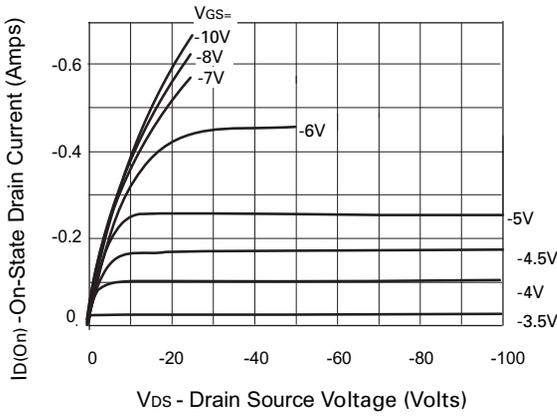
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

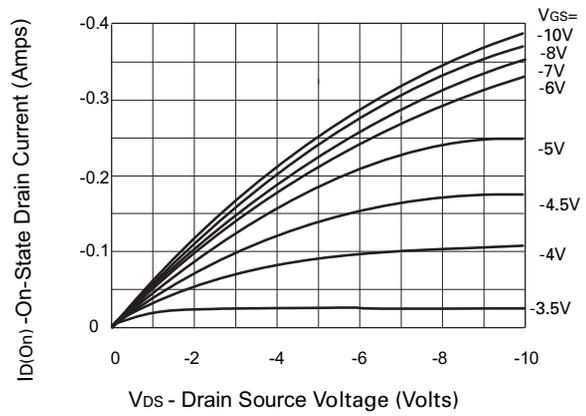
(\ddagger) Switching characteristics are independent of operating junction temperature.

(\ddagger) For design aid only, not subject to production testing.

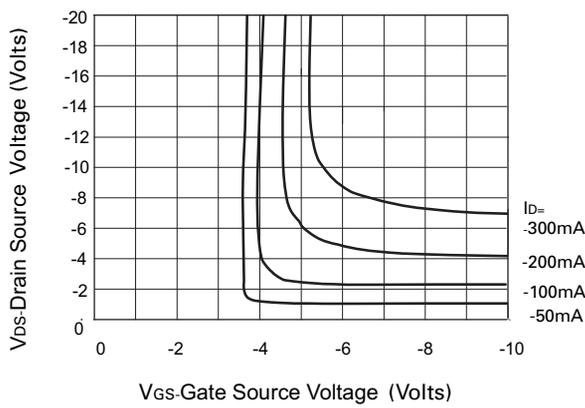
Typical characteristics



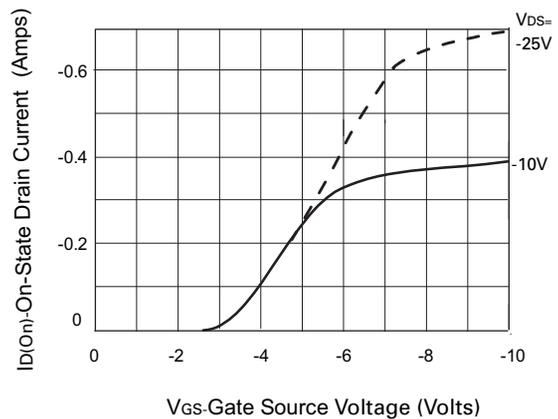
Output Characteristics



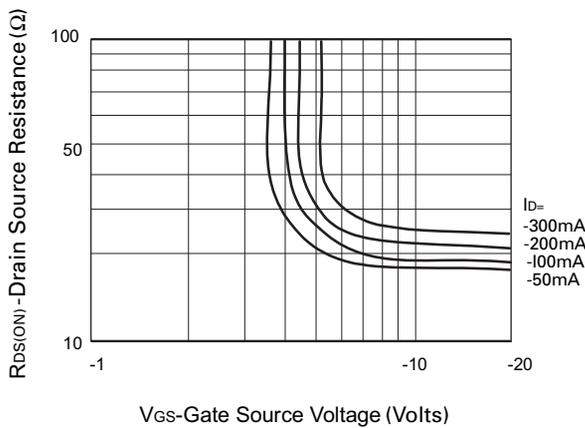
Saturation Characteristics



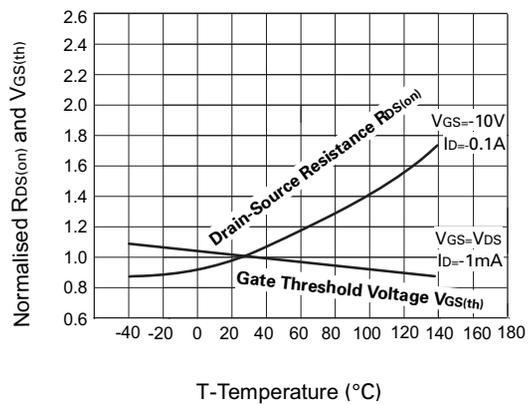
Voltage Saturation Characteristics



Transfer Characteristics

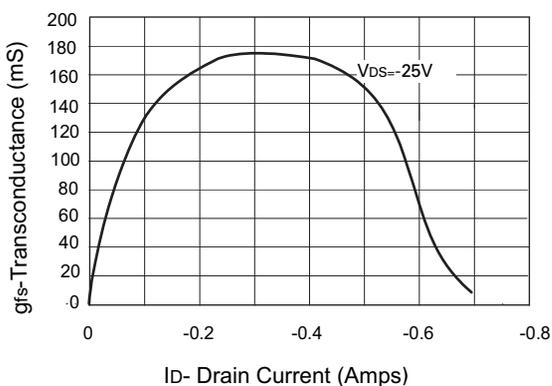


On-resistance vs gate-source voltage

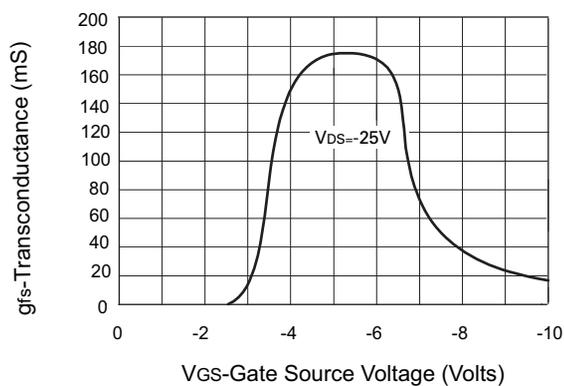


Normalised $R_{DS(on)}$ and $V_{GS(th)}$ vs Temperature

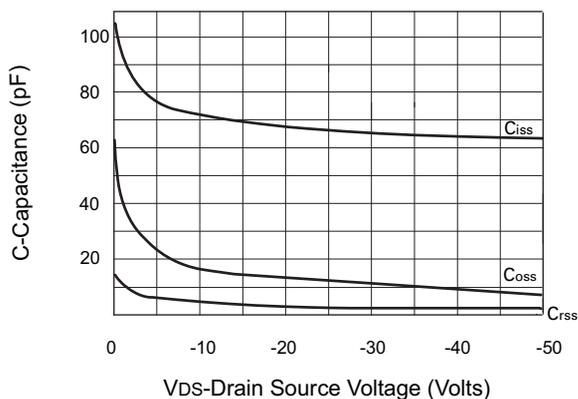
Typical characteristics



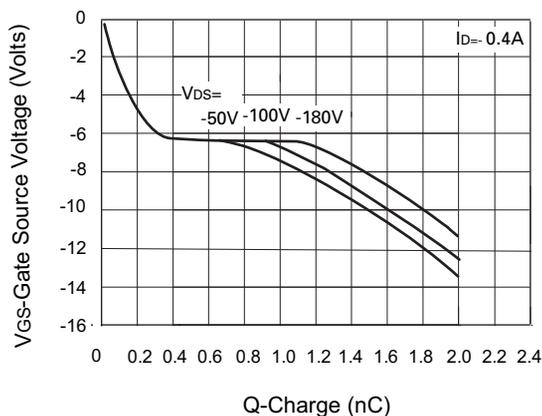
Transconductance v drain current



Transconductance v gate-source voltage

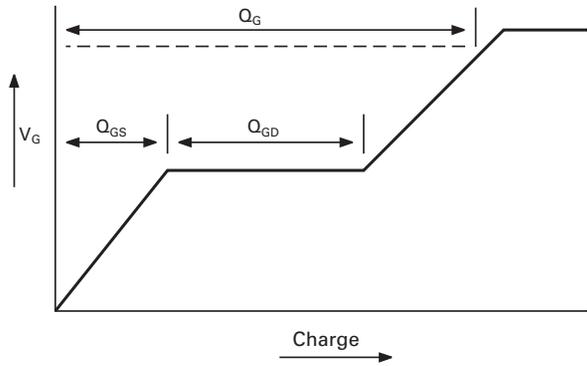


Capacitance v drain-source voltage

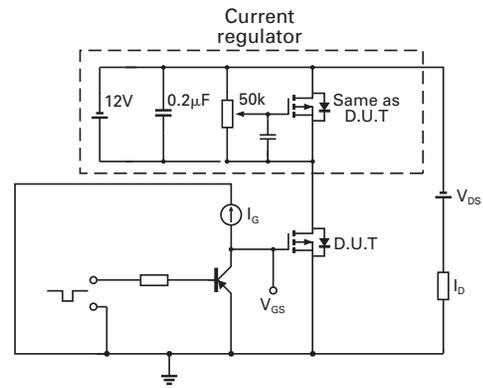


Gate charge v gate-source voltage

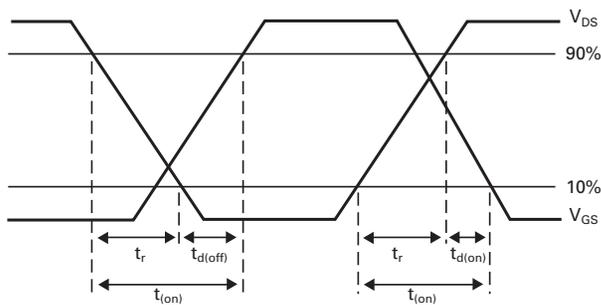
Typical characteristics



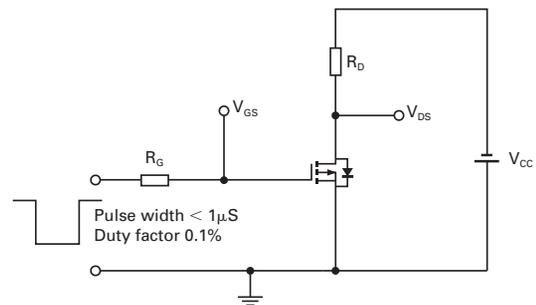
Basic gate charge waveform



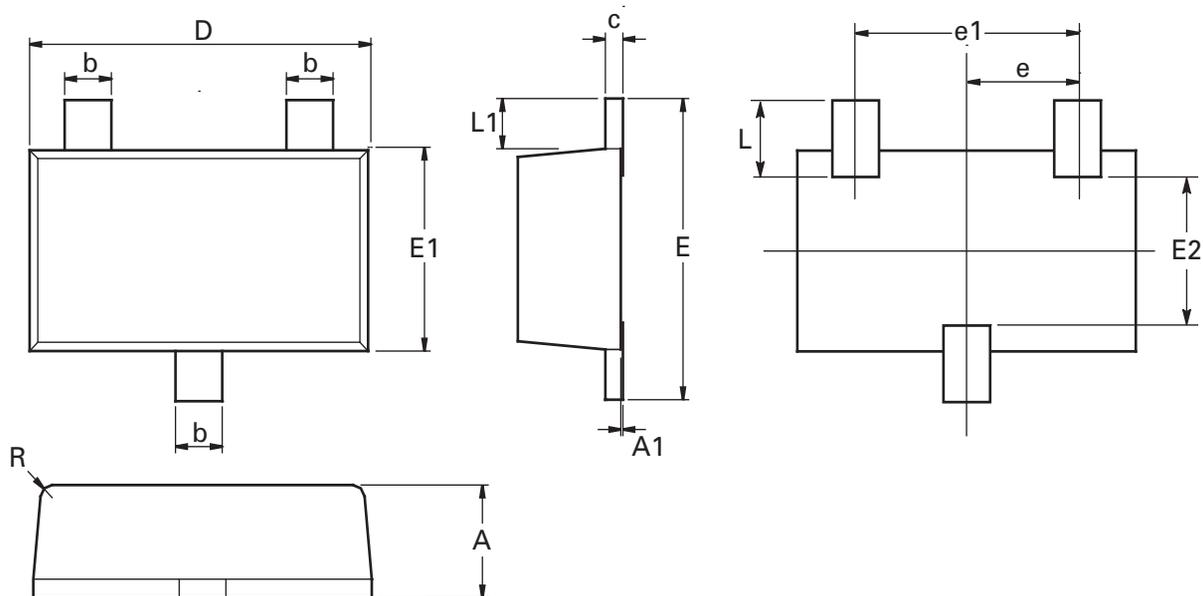
Gate charge test circuit



Switching time waveforms



Switching time test circuit

Package outline - SOT23F


Dim.	Millimeters		Inches		Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Max.	Max.
A	0.80	1.00	0.0315	0.0394	E	2.30	2.50	0.0906	0.0984
A1	0.00	0.10	0.00	0.0043	E1	1.50	1.70	0.0590	0.0669
b	0.35	0.45	0.0153	0.0161	E2	1.10	1.26	0.0433	0.0496
c	0.10	0.20	0.0043	0.0079	L	0.48	0.68	0.0189	0.0268
D	2.80	3.00	0.1102	0.1181	L1	0.30	0.50	0.0153	0.0161
e	0.95 ref		0.0374 ref		R	0.05	0.15	0.0019	0.0059
e1	1.80	2.00	0.0709	0.0787	O	0°	12°	0°	12°

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches