



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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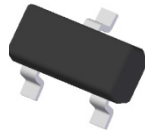
Features

- Low On-Resistance:
 - $R_{DS(ON)} < 54m\Omega @ V_{GS} = 10V$
 - $R_{DS(ON)} < 72m\Omega @ V_{GS} = 4.5V$
 - $R_{DS(ON)} < 115m\Omega @ V_{GS} = 2.5V$
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

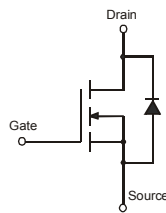
Mechanical Data

- Case: SOT-23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking Information: See Page 4
- Ordering Information: See Page 4
- Weight: 0.008 grams (approximate)

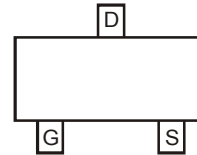
SOT-23



TOP VIEW



EQUIVALENT CIRCUIT



Pin Configuration

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 12	V
Drain Current (Note 5)	I_D	$T_A = +25^\circ\text{C}$	3.8
		$T_A = +70^\circ\text{C}$	3.1
Drain Current (Note 5)	I_{DM}	15	A
Body-Diode Continuous Current (Note 5)	I_S	2.0	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.4	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	90	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	800	nA	$V_{DS} = 28\text{V}, V_{GS} = 0\text{V}$
Gate-Body Leakage	I_{GSS}	—	—	± 80 ± 800	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$ $V_{GS} = \pm 19\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	0.62	0.92	1.4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	39	54	m Ω	$V_{GS} = 10\text{V}, I_D = 3.8\text{A}$
		—	52	72		$V_{GS} = 4.5\text{V}, I_D = 3.6\text{A}$
			90	115		$V_{GS} = 2.5\text{V}, I_D = 3.1\text{A}$
Forward Transconductance	$ Y_{fs} $	—	3	—	S	$V_{DS} = 5\text{V}, I_D = 3.1\text{A}$
Source-Drain Diode Forward Voltage	V_{SD}	—	—	1.16	V	$V_{GS} = 0\text{V}, I_S = 2.0\text{A}$
DYNAMIC CHARACTERISTICS (Note 7)						
Gate Resistance	R_g	-	4.17	-	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge (10V)	Q_g	-	8.2	-	nC	$V_{GS} = 10\text{V}, V_{DS} = 10\text{V}, I_D = 3.8\text{A}$
Total Gate Charge (4.5V)	Q_g	-	3.7	-	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V}, I_D = 3.8\text{A}$
Gate-Source Charge	Q_{gs}	-	0.7	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.1	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	1.14	-	ns	$V_{DD} = 15\text{V}, V_{GEN} = 10\text{V}, R_{GEN} = 6\Omega, R_L = 3.9\Omega$
Turn-On Rise Time	t_r	-	3.49	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	15.02	-	ns	
Turn-Off Fall Time	t_f	-	3.26	-	ns	
Input Capacitance	C_{iss}	—	305	—	pF	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	74	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	48	—	pF	

- Notes:
- Device mounted on FR-4 PCB. $t \leq 5$ sec.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

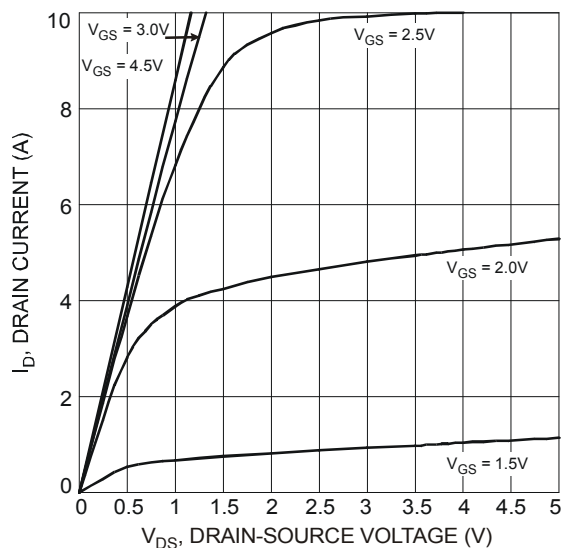


Fig. 1 Typical Output Characteristics

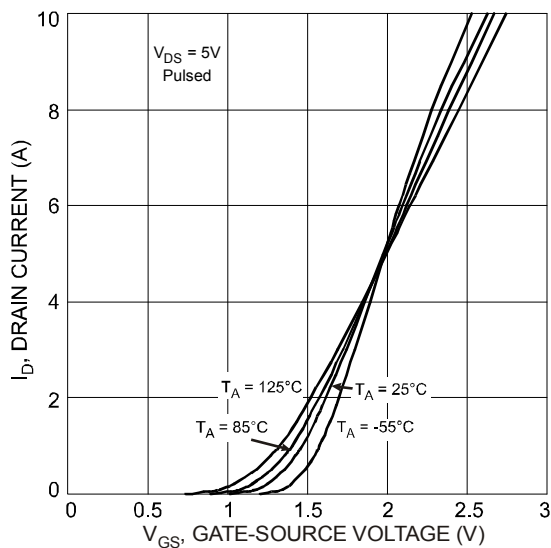


Fig. 2 Typical Transfer Characteristics

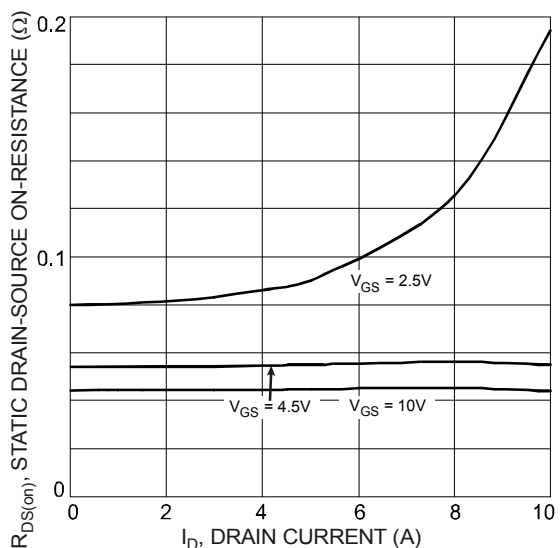


Fig. 3 On-Resistance vs. Drain Current and Gate Voltage

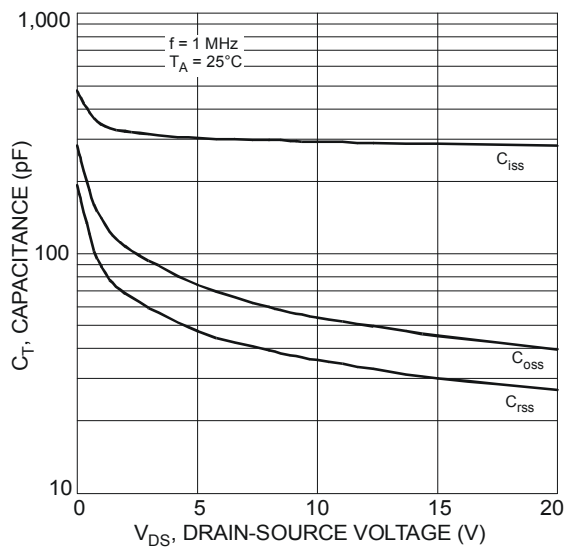


Fig. 4 Typical Total Capacitance

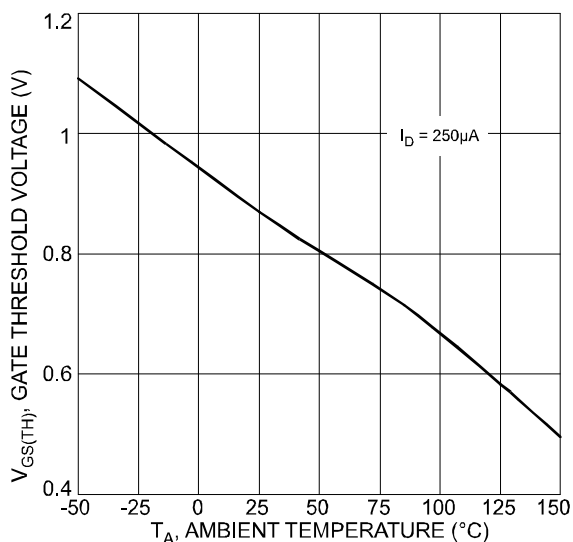


Fig. 5 Gate Threshold Voltage vs. Ambient Temperature

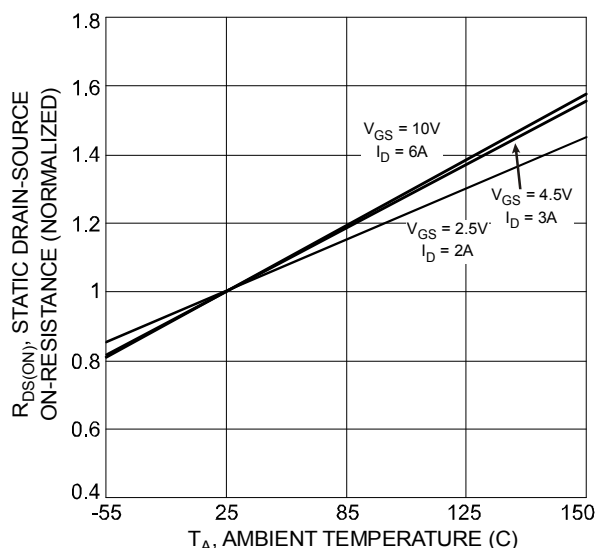


Fig. 6 Normalized Static Drain-Source On-Resistance vs. Ambient Temperature

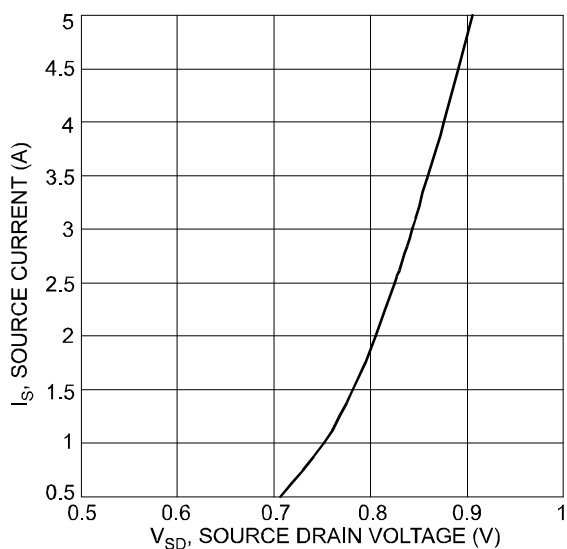


Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

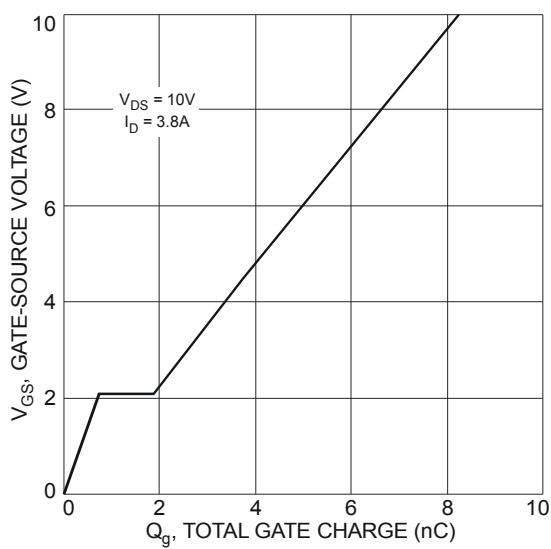
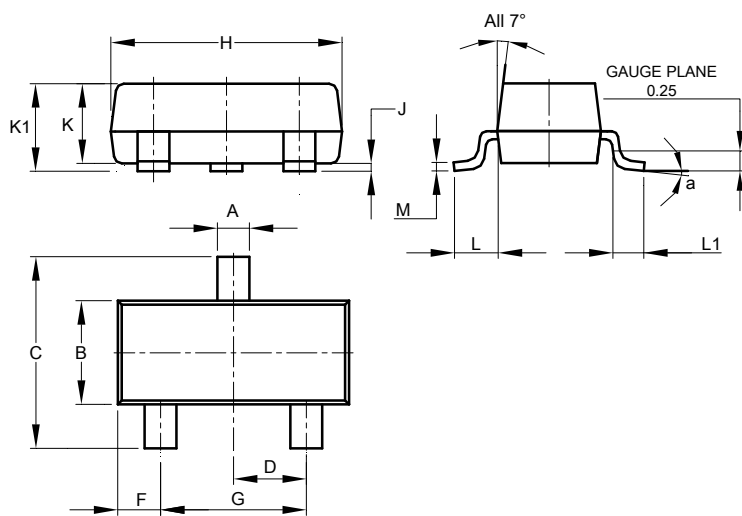


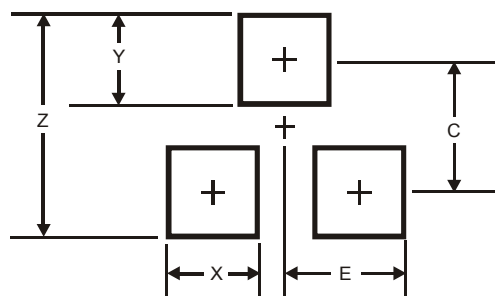
Fig. 8 Gate-Source Voltage vs. Total Gate Charge

Package Outline Dimensions



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
α	8°		
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35