优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	Package	I_D T_A = +25°C
30V	0.15Ω @ V_{GS} = 4.5V	SOT23	2A
	0.2Ω @ V_{GS} = 2.5V		1.6A
	0.25Ω @ V_{GS} = 1.8V		1.4A
	0.3Ω @ V_{GS} = 1.5V		1.2A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc

Features

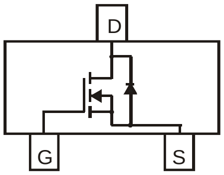
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (approximate)

SOT23

Top View



Internal Schematic

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	1.5 1.2	A
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	2.0 1.6	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I_{DM}	8	A
Maximum Body Diode Continuous Current (Note 6)			I_S	1.6	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 5)	P_D	0.7	W
	(Note 6)		1.3	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	176	°C/W
	(Note 6)		102	
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	45	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	37	—	V	V_{GS} = 0V, I_D = 100µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	100	150	mΩ	V_{GS} = 4.5V, I_D = 4.5A
			140	200		V_{GS} = 2.5V, I_D = 3.5A
			185	250		V_{GS} = 1.8V, I_D = 1.5A
			240	300		V_{GS} = 1.5V, I_D = 0.5A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	5	—	S	V_{DS} =5V, I_D = 2.4A
Diode Forward Voltage	V_{SD}	—	0.8	1.1	V	V_{GS} = 0V, I = 0.5A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	193	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	35	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	23	—	pF	
Turn-On Delay Time	$t_{d(on)}$	—	7	—	ns	V_{DD} = 10V, R_L = 10Ω I_D = 1A, V_{GEN} = 4.5V, R_G = 6Ω
Rise Time	t_r	—	24	—		
Turn-Off Delay Time	$t_{d(off)}$	—	24	—		
Fall Time	t_f	—	12	—		

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
7 .Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing

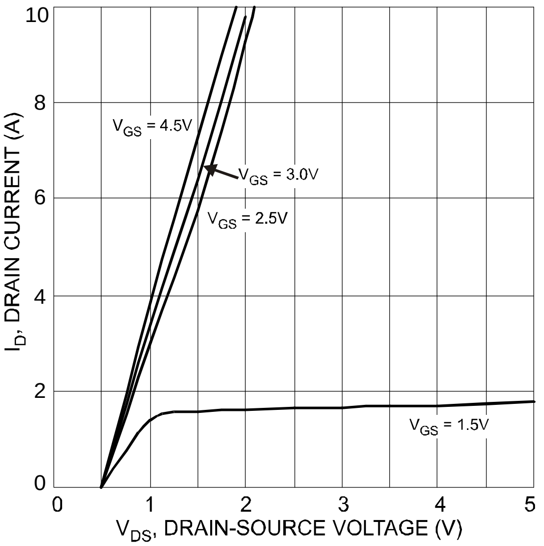


Fig.1 Typical Output Characteristic

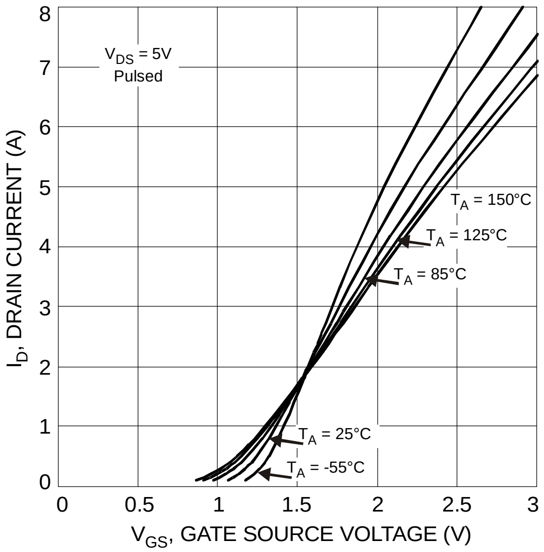


Fig. 2 Typical Transfer Characteristics

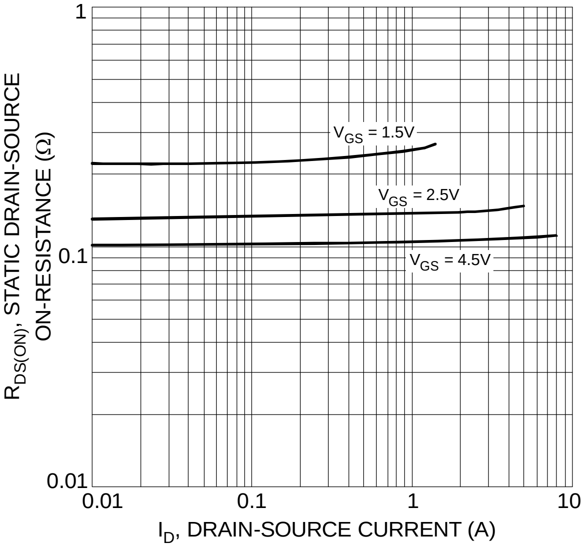


Fig. 3 On-Resistance vs. Drain Current & Gate Voltage

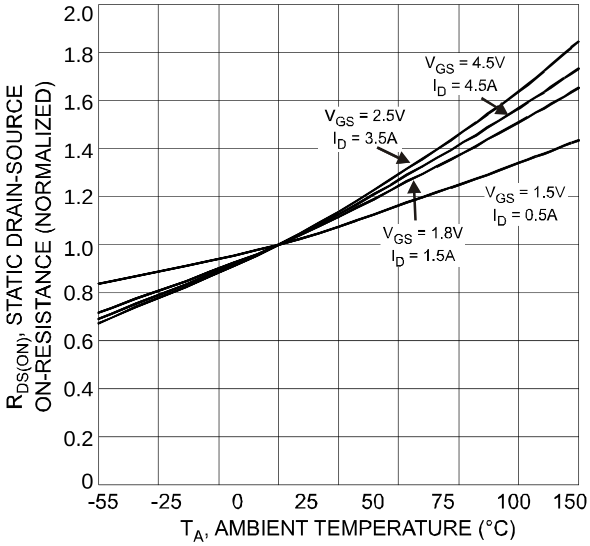


Fig. 4 Normalized Static Drain-Source On-Resistance vs. Ambient Temperature

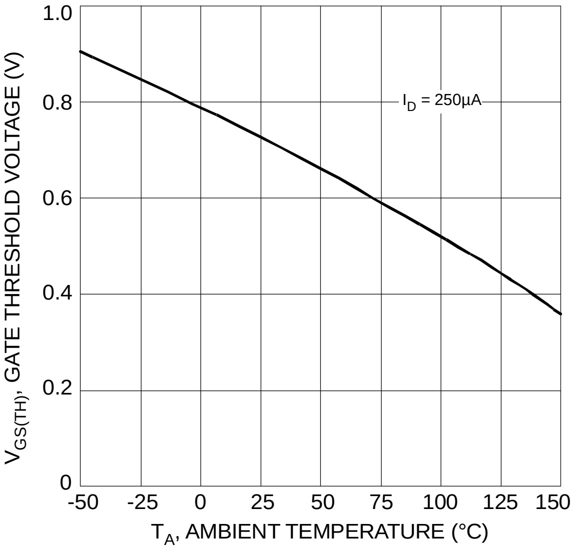


Fig. 5 Gate Threshold Variation vs. Ambient Temperature

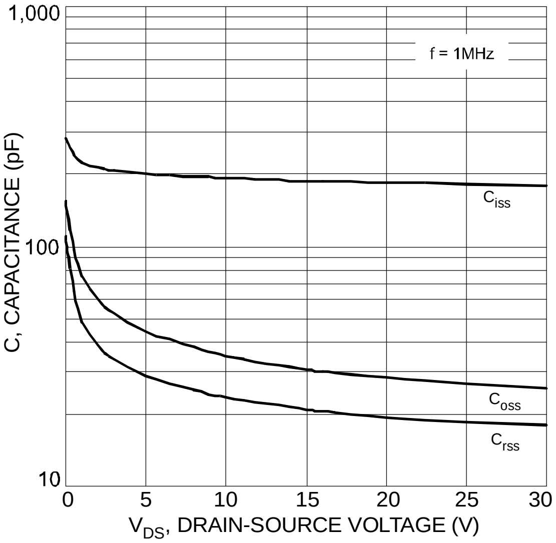


Fig. 6 Typical Total Capacitance

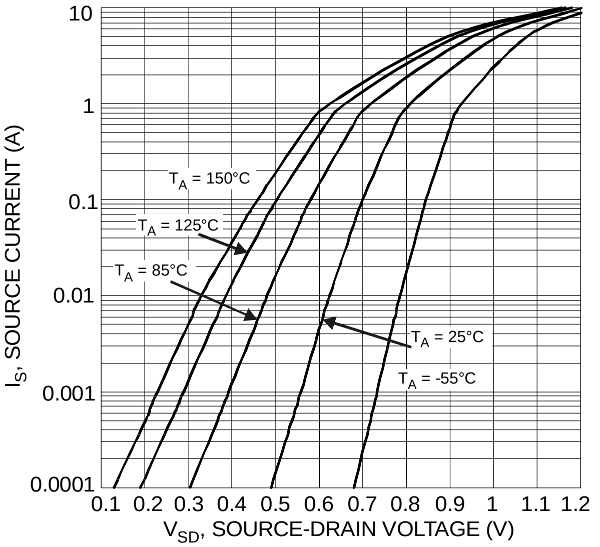


Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

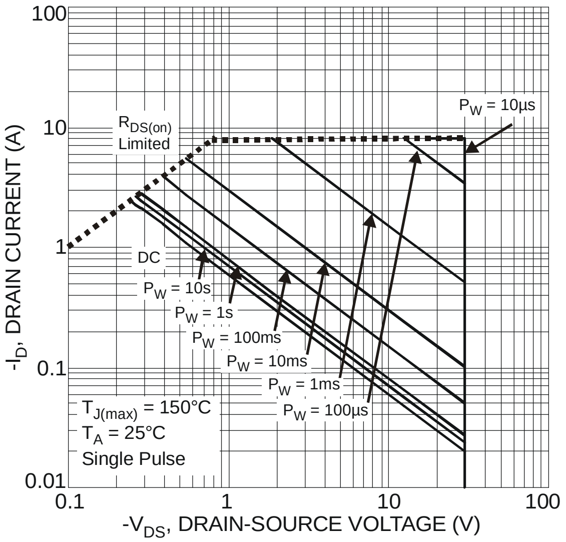


Fig. 8 SOA, Safe Operation Area

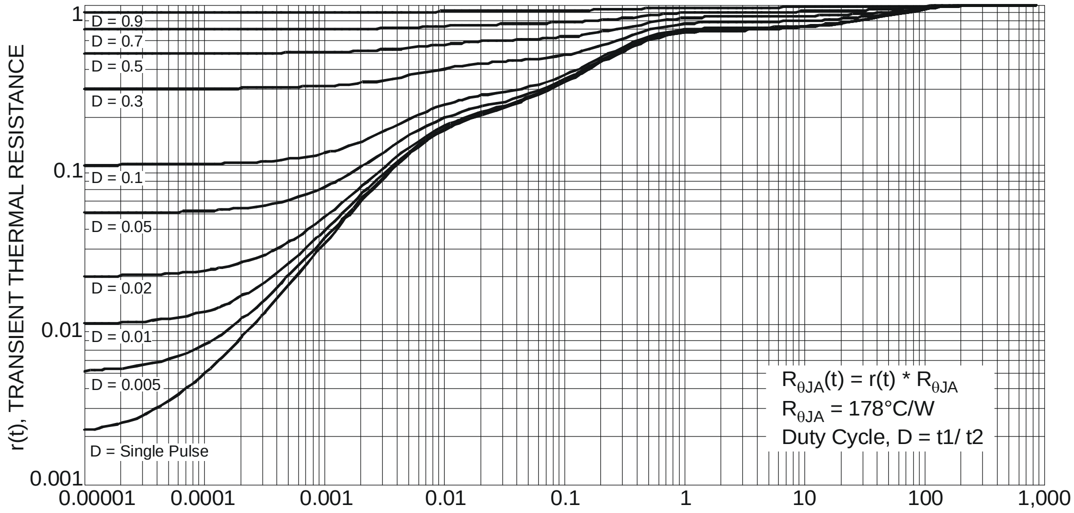
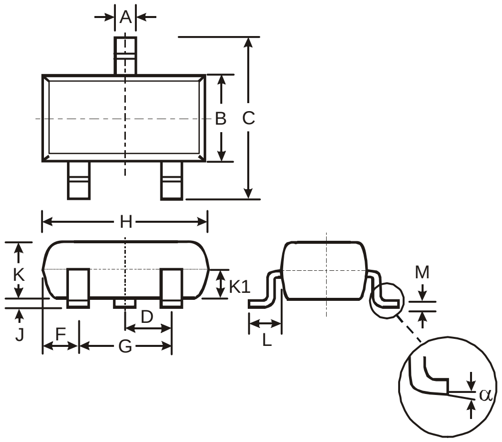


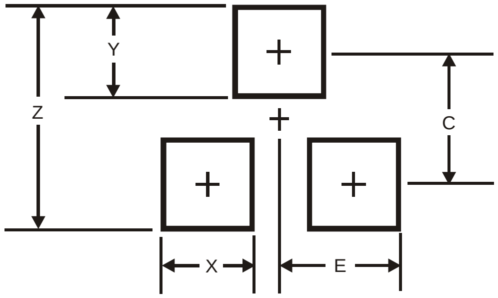
Fig. 9 Transient Thermal Resistance

Package Outline Dimensions



SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35