



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D max $T_A = 25^\circ\text{C}$
20V	55m Ω @ $V_{GS} = 4.5\text{V}$	4.0A
	70m Ω @ $V_{GS} = 2.5\text{V}$	3.5A
	90m Ω @ $V_{GS} = 1.8\text{V}$	3.1A
	130m Ω @ $V_{GS} = 1.5\text{V}$	2.5A

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate

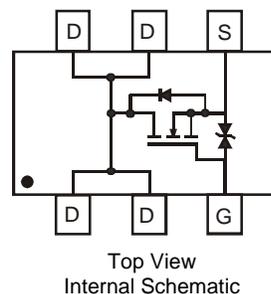
Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions

Mechanical Data

- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.015 grams (approximate)



Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Units	
Drain-Source Voltage		V_{DSS}	20	V	
Gate-Source Voltage		V_{GSS}	± 8	V	
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	I_D	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	4.0 3.1	A
	$t < 10\text{s}$		$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	4.5 3.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)		I_{DM}	13	A	
Maximum Body Diode Continuous Current		I_S	1.5	A	

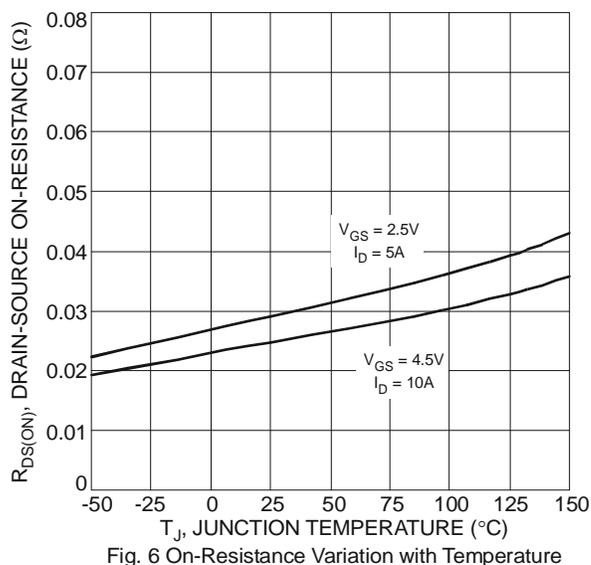
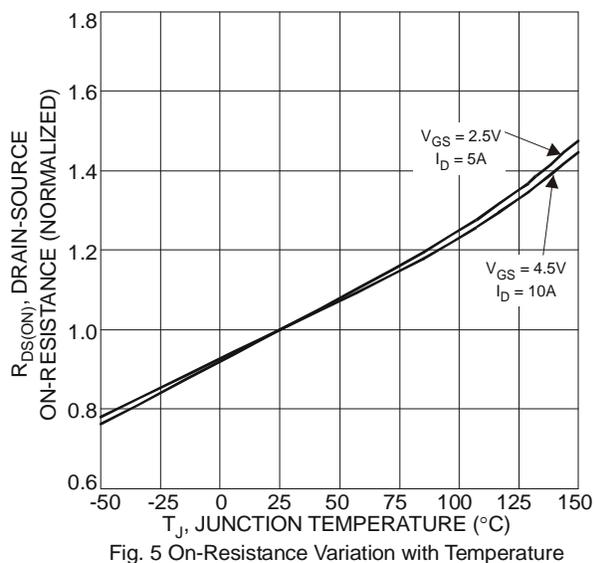
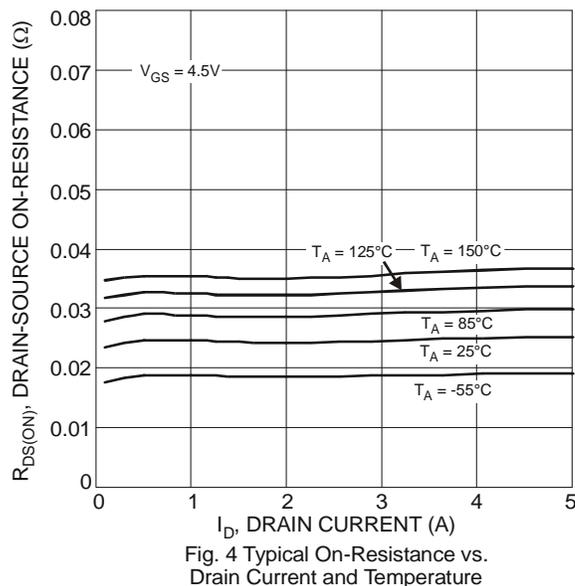
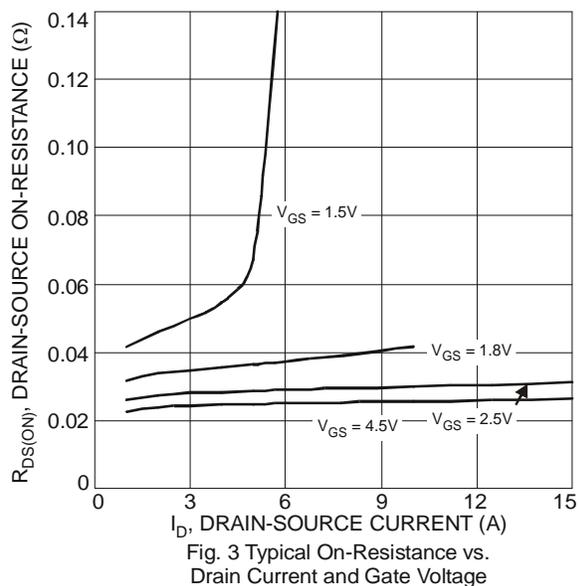
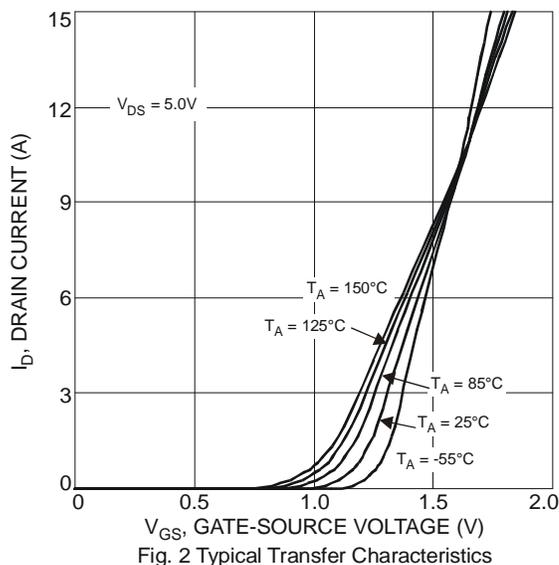
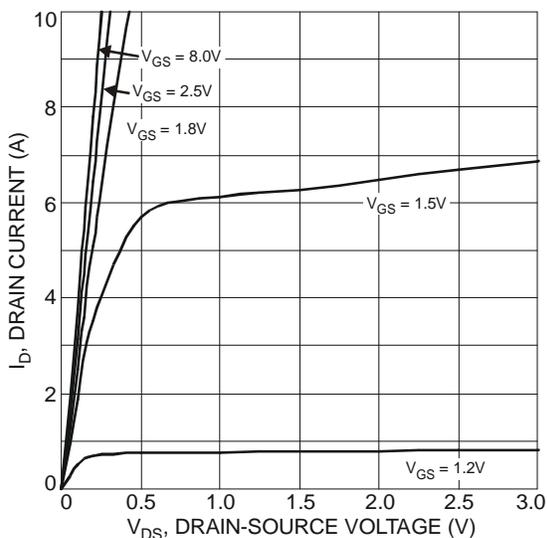
Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = 25^\circ\text{C}$	P_D	1	W
	$T_A = 70^\circ\text{C}$		0.6	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	127	$^\circ\text{C/W}$
	$t < 10\text{s}$		91	
Total Power Dissipation (Note 6)	$T_A = 25^\circ\text{C}$	P_D	1.5	W
	$T_A = 70^\circ\text{C}$		0.9	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	85	$^\circ\text{C/W}$
	$t < 10\text{s}$		63	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	3.1	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 1	μA	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	0.6	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	32	55	m Ω	$V_{GS} = 4.5\text{V}, I_D = 6\text{A}$
		—	43	70		$V_{GS} = 2.5\text{V}, I_D = 4.0\text{A}$
		—	56	90		$V_{GS} = 1.8\text{V}, I_D = 1.5\text{A}$
		—	80	130		$V_{GS} = 1.5\text{V}, I_D = 1.0\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	8	—	S	$V_{DS} = 10\text{V}, I_D = 6\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.1	V	$V_{GS} = 0\text{V}, I_S = 2\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	555	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	112	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	84	—	pF	
Total Gate Charge	Q_g	—	8.8	—	nC	$V_{DS} = 10\text{V}, V_{GS} = 4.5\text{V},$ $I_D = 6.5\text{A}$
Gate-Source Charge	Q_{gs}	—	1.4	—	nC	
Gate-Drain Charge	Q_{gd}	—	3	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	53	—	ns	$V_{DS} = 10\text{V}, I_D = 1.0\text{A}$ $V_{GS} = 4.5\text{V}, R_G = 6\Omega$
Turn-On Rise Time	t_r	—	78	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	561	—	ns	
Turn-Off Fall Time	t_f	—	234	—	ns	

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate
 - Short duration pulse test used to minimize self-heating effect
 - Guaranteed by design. Not subject to production testing



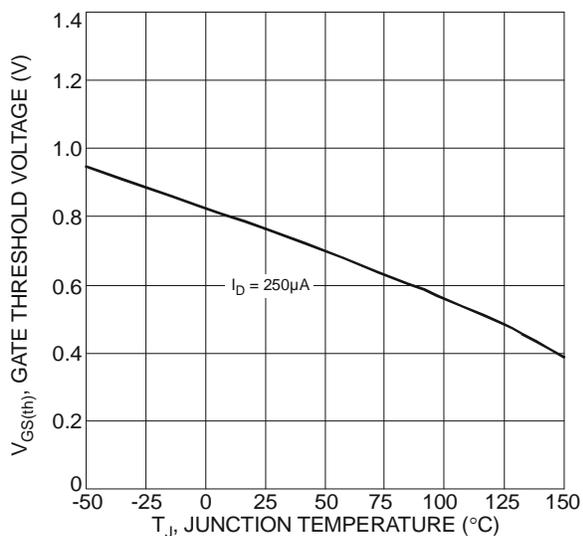


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

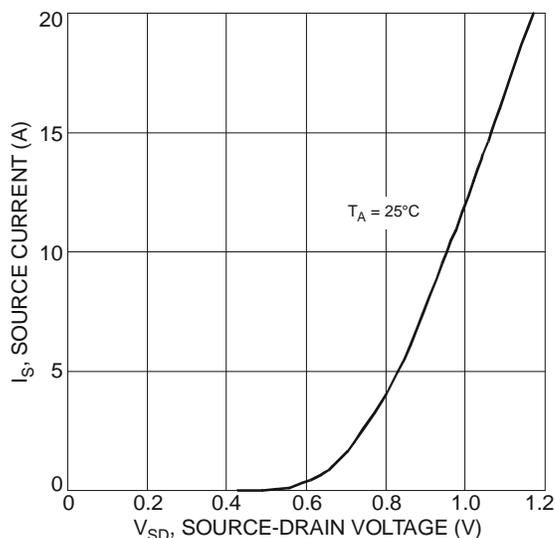


Fig. 8 Diode Forward Voltage vs. Current

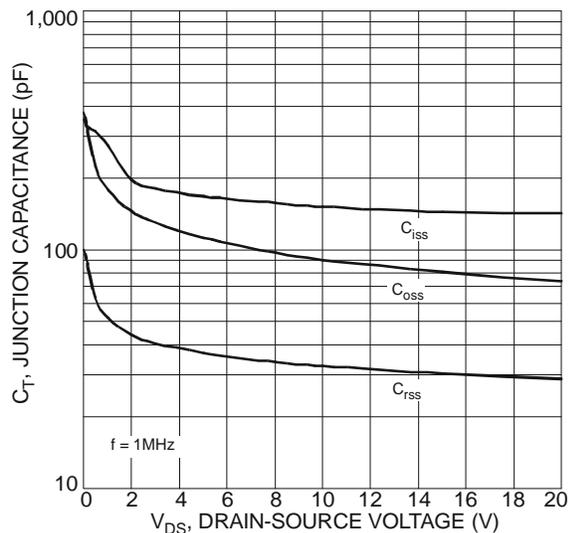


Fig. 9 Typical Junction Capacitance

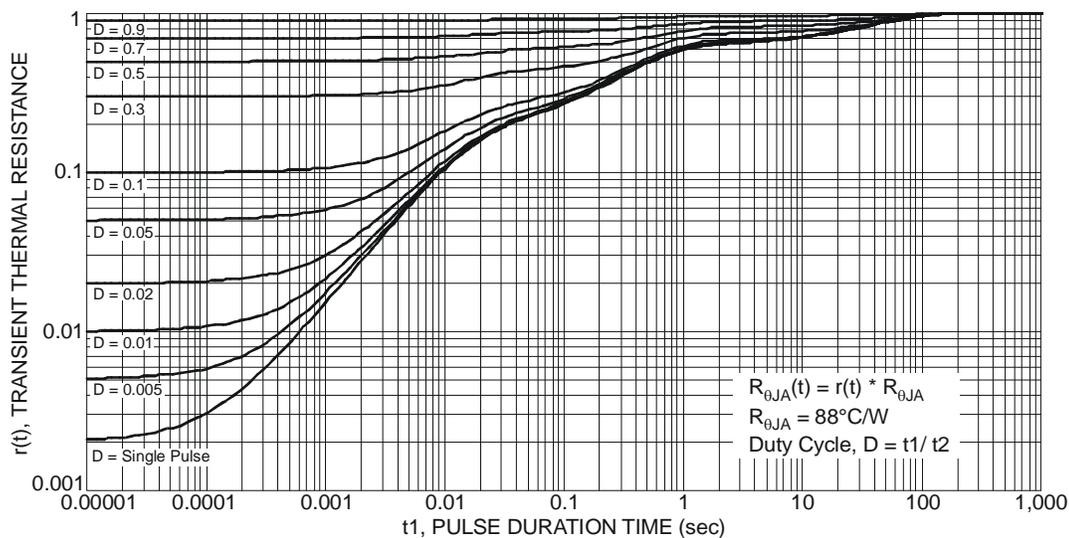
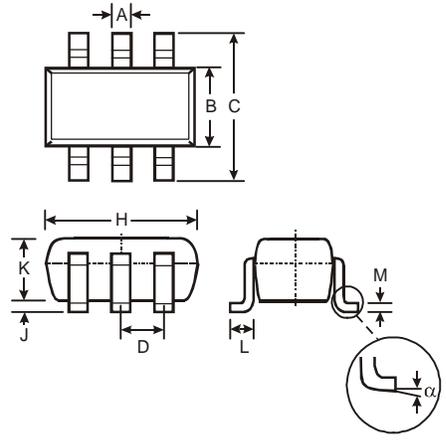


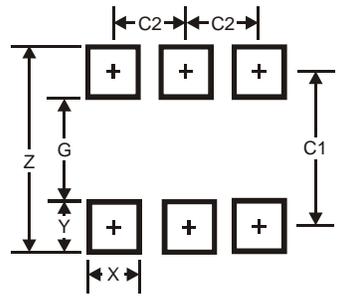
Fig. 10 Transient Thermal Resistance

Package Outline Dimensions



SOT26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
α	0°	8°	—
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95