



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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企业微信二维码



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Product Summary

BV _{DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
-30V	14mΩ @ V _{GS} = -10V	-12.0A
	25mΩ @ V _{GS} = -4.5V	-8.5A

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

Description

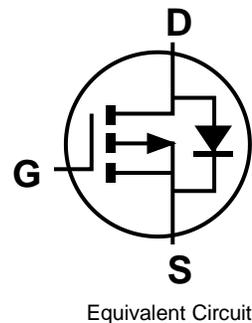
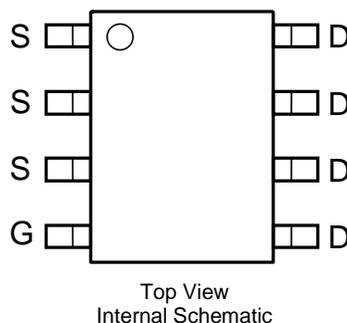
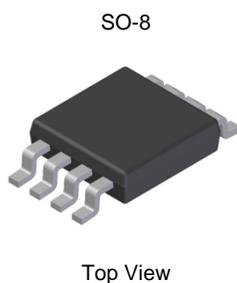
This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 Ⓔ
- Weight: 0.074g (Approximate)



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Drain Current (Note 5)	Steady State	$T_A = +25^\circ\text{C}$	I_D	-12	A
		$T_A = +70^\circ\text{C}$		-9	
Pulsed Drain Current (Note 6)			I_{DM}	-80	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.5	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu\text{A}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$	
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
		—	—	± 800		$V_{GS} = \pm 25V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	$V_{GS(TH)}$	-1	—	-2	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	11.6	14	m Ω	$V_{GS} = -10V, I_D = -8A$	
		—	18.6	25		$V_{GS} = -4.5V, I_D = -5A$	
Forward Transconductance	g_{fs}	—	12	—	S	$V_{DS} = -10V, I_D = -12A$	
Diode Forward Voltage (Note 7)	V_{SD}	-0.5	—	-1.1	V	$V_{GS} = 0V, I_S = -2A$	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{iss}	—	1802	—	pF	$V_{DS} = -15V, V_{GS} = 0V, f = 1.0\text{MHz}$	
Output Capacitance	C_{oss}	—	415	—	pF		
Reverse Transfer Capacitance	C_{rss}	—	295	—	pF		
Gate Resistance	R_G	—	2.3	—	Ω	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$	
SWITCHING CHARACTERISTICS							
Total Gate Charge	Q_g	—	15.3	—	nC	$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -8A$	
			30.7			$V_{DS} = -15V, V_{GS} = -10V, I_D = -8A$	
Gate-Source Charge	Q_{gs}	—	3.5	—		nC	$V_{DS} = -15V, V_{GS} = -10V, I_D = -8A$
Gate-Drain Charge	Q_{gd}	—	7.9	—			$V_{DS} = -15V, V_{GS} = -10V, I_D = -8A$
Turn-On Delay Time	$t_{D(ON)}$	—	5.1	—	ns	$V_{GS} = -10V, V_{DS} = -15V, R_D = 15\Omega, R_G = 6\Omega$	
Rise Time	t_R	—	8	—			
Turn-Off Delay Time	$t_{D(OFF)}$	—	46	—			
Fall Time	t_F	—	30	—			

- Notes:
- Device mounted on 2 oz. copper pads on FR-4 PCB with $R_{\theta JA} = 50^\circ\text{C/W}$.
 - Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
 - Short duration pulse test used to minimize self-heating effect.

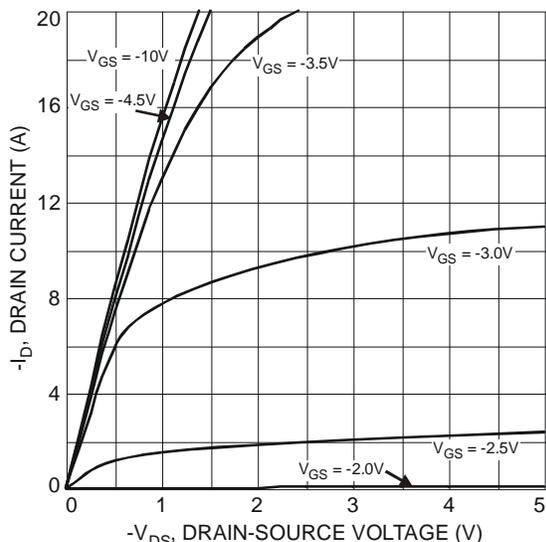


Fig. 1 Typical Output Characteristic

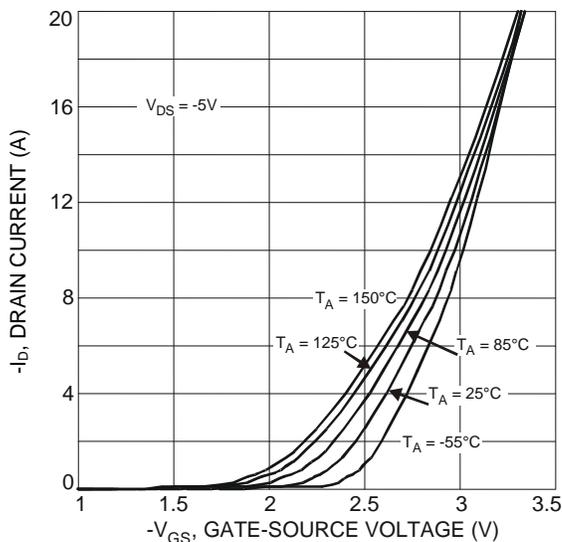


Fig. 2 Typical Transfer Characteristic

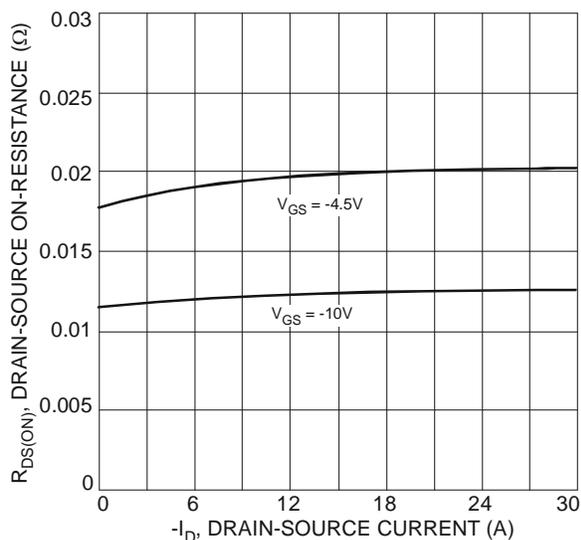


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

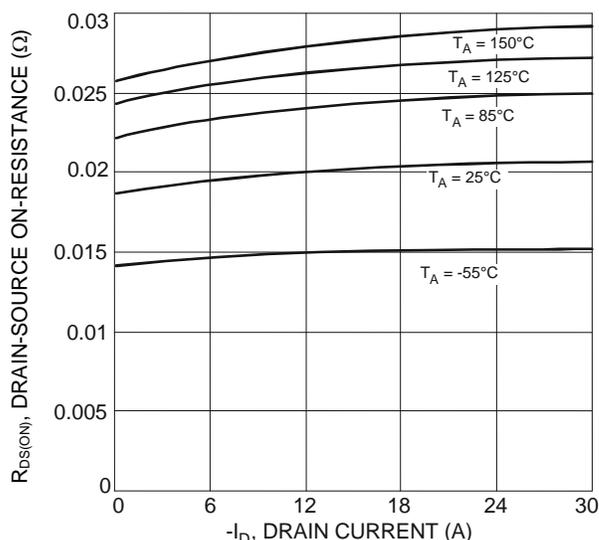


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

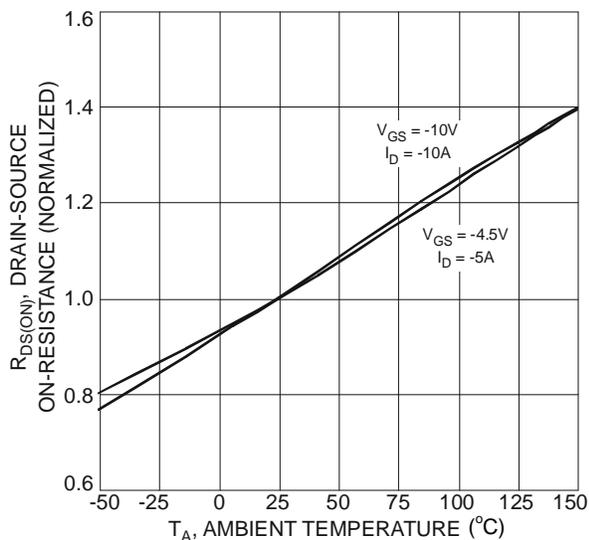


Fig. 5 Normalized On-Resistance vs. Ambient Temperature

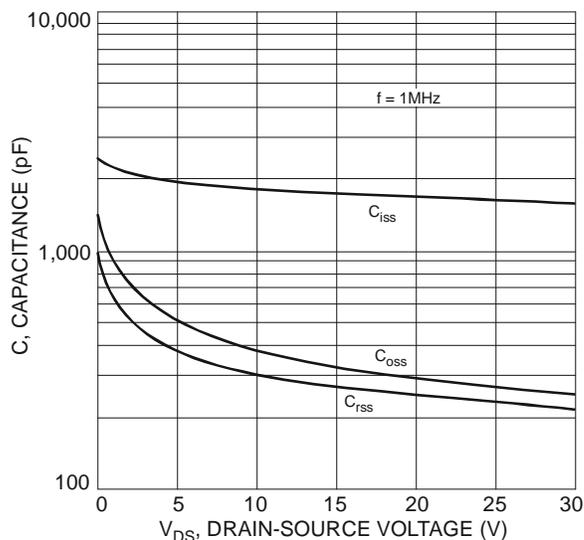


Fig. 6 Typical Total Capacitance

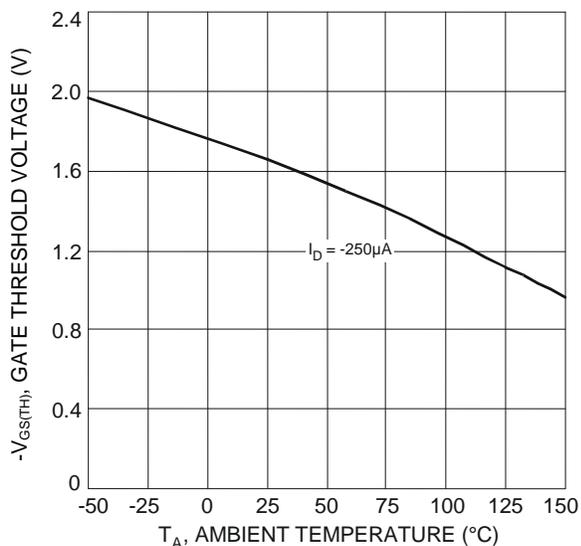


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

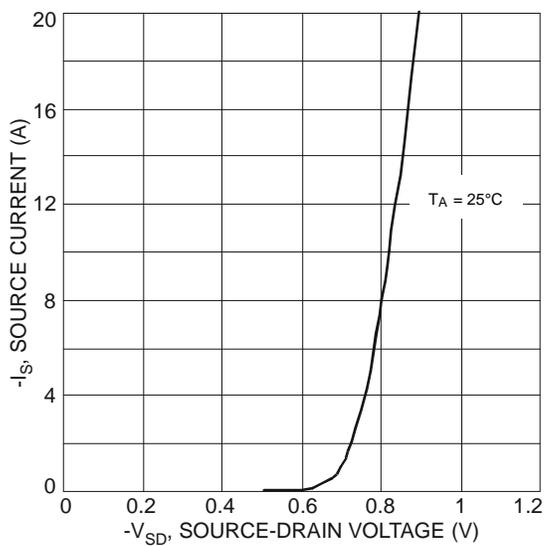


Fig. 8 Diode Forward Voltage vs. Current

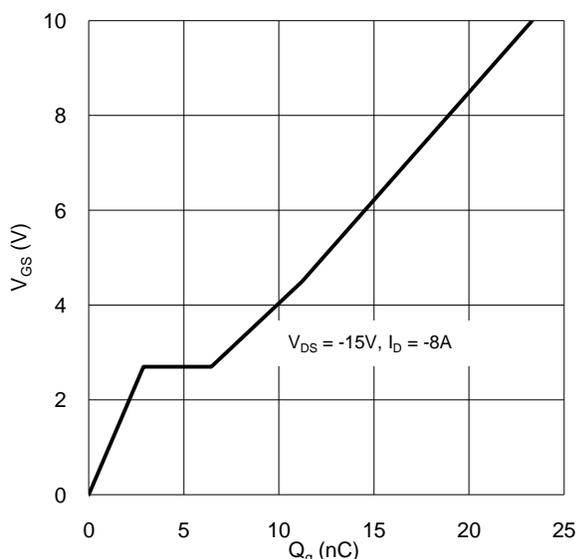


Fig. 9 Gate Charge

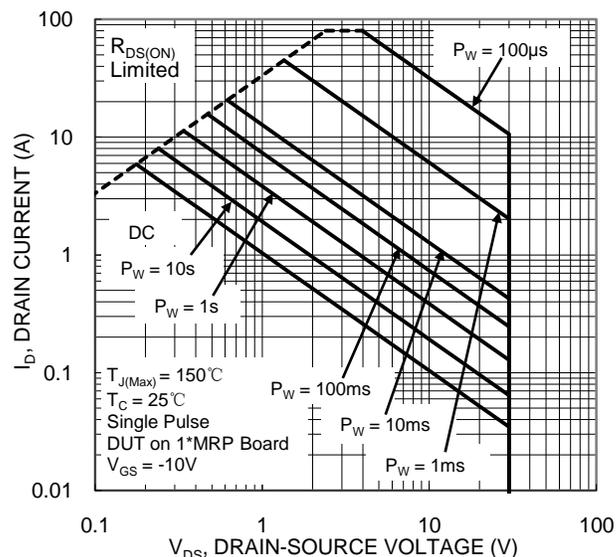


Fig. 10 SOA, Safe Operation Area

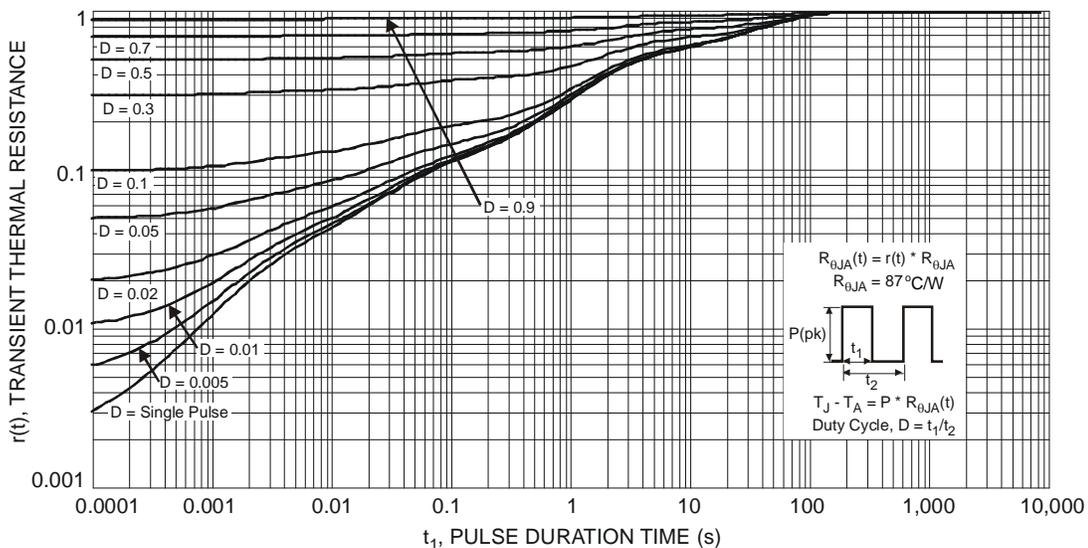
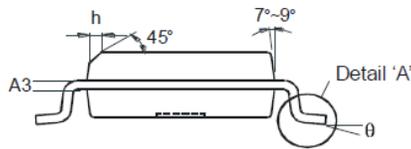
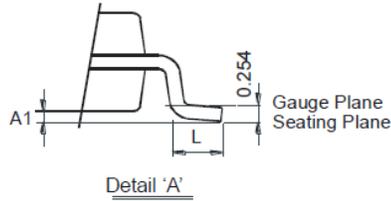
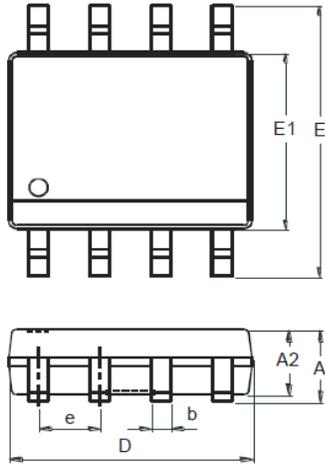


Fig. 11 Transient Thermal Response

Package Outline Dimensions

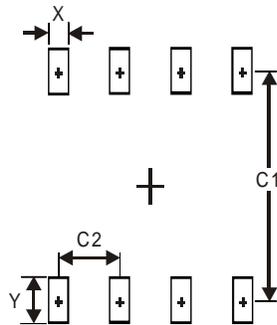
SO-8



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27