



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ\text{C}$
60V	6Ω @ $V_{GS} = 5V$	200mA

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

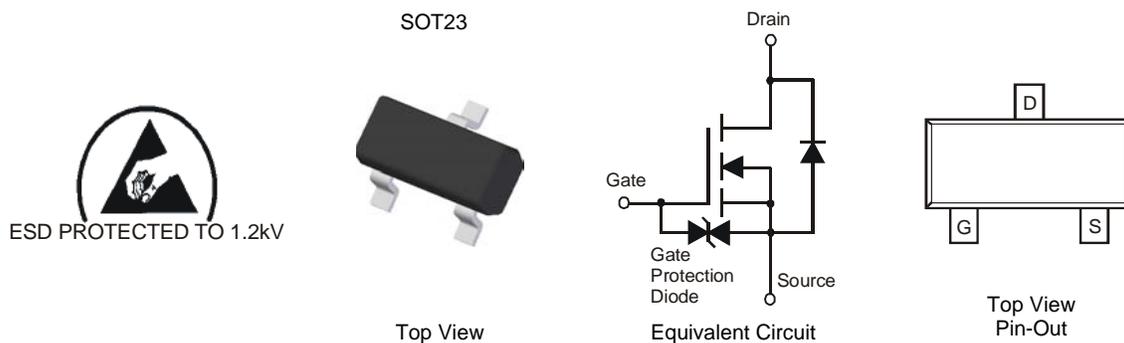
- Motor Control
- Power Management Functions

Features and Benefits

- N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package
- ESD Protected Gate, 1.2kV HBM
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	180	mA
		$T_A = +85^\circ\text{C}$		130	
		$T_A = +100^\circ\text{C}$		115	
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	220	mA
		$T_A = +85^\circ\text{C}$		160	
		$T_A = +100^\circ\text{C}$		140	
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	0.5	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	800	mA

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 5)	P_D	370	mW
	(Note 6)		540	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	348	$^\circ\text{C/W}$
	(Note 6)		241	
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	91	$^\circ\text{C}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout
 6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	60	70	—	V	V _{GS} = 0V, I _D = 10μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1.0 500	μA	@ T _C = +25°C @ T _C = +125°C V _{DS} = 60V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	1.2	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	3.5 3.0	6 5	Ω	@ T _J = +25°C @ T _J = +125°C V _{GS} = 5.0V, I _D = 0.115A V _{GS} = 10V, I _D = 0.115A
Forward Transconductance	g _{FS}	80	—	—	mS	V _{DS} = 10V, I _D = 0.115A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	23	—	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	3.4	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	1.4	—	pF	
Gate Resistance	R _G	—	260	400	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
SWITCHING CHARACTERISTICS (Note 8)						
Turn-On Delay Time	t _{D(ON)}	—	10	—	ns	V _{DD} = 30V, I _D = 0.115A, R _L = 150Ω, V _{GEN} = 10V, R _{GEN} = 25Ω
Turn-Off Delay Time	t _{D(OFF)}	—	33	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

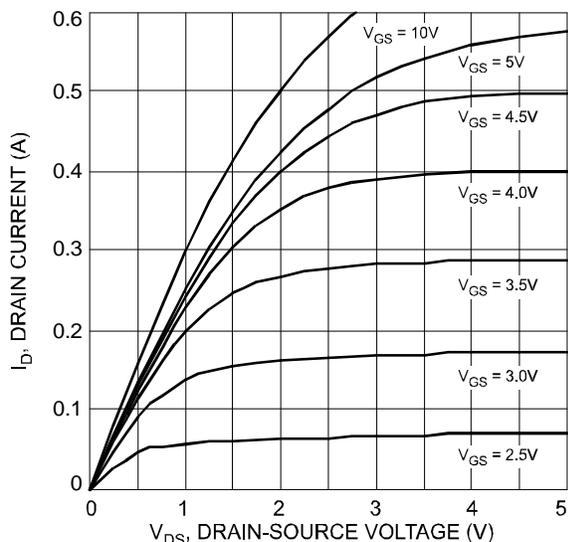


Fig.1 Typical Output Characteristic

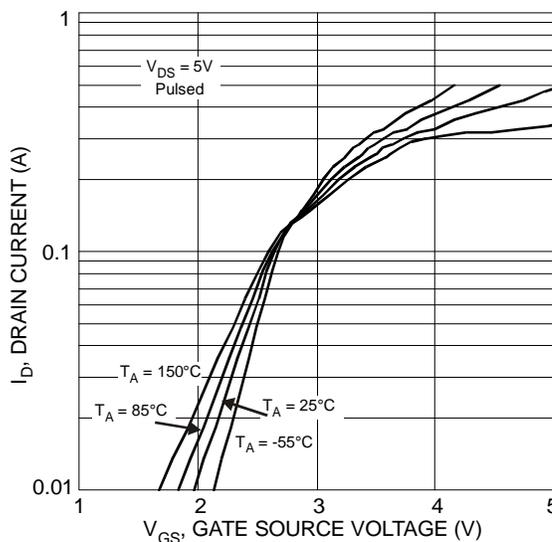


Fig.2 Typical Transfer Characteristics

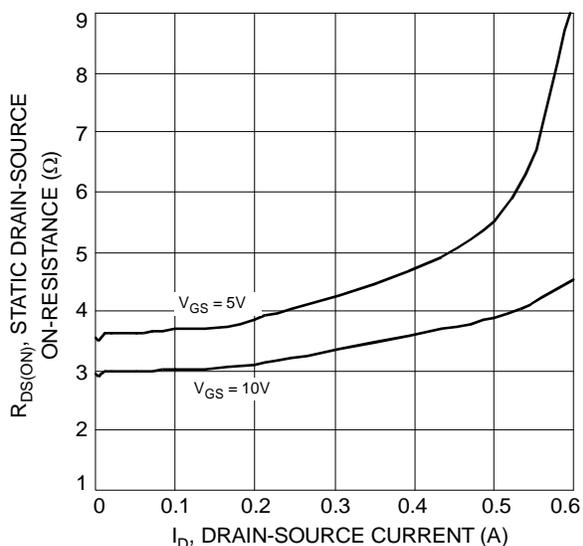


Fig. 3 On-Resistance vs. Drain Current & Gate Voltage

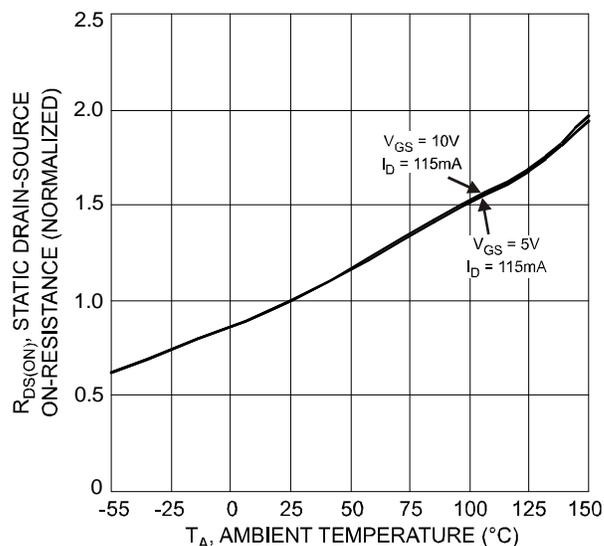


Fig. 4 Normalized Static Drain-Source On-Resistance vs. Ambient Temperature

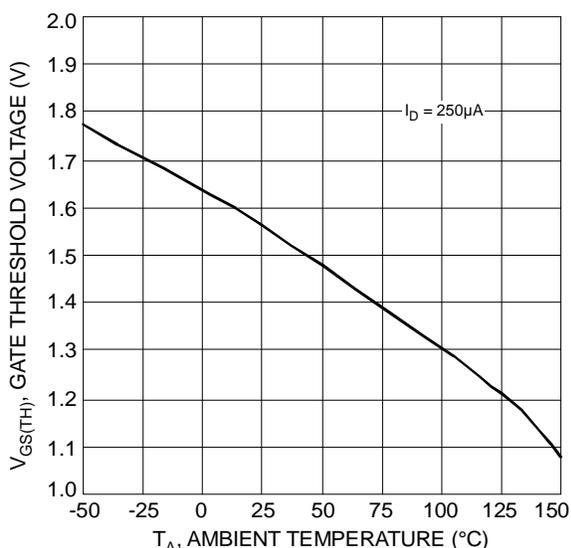


Fig. 5 Gate Threshold Variation vs. Ambient Temperature

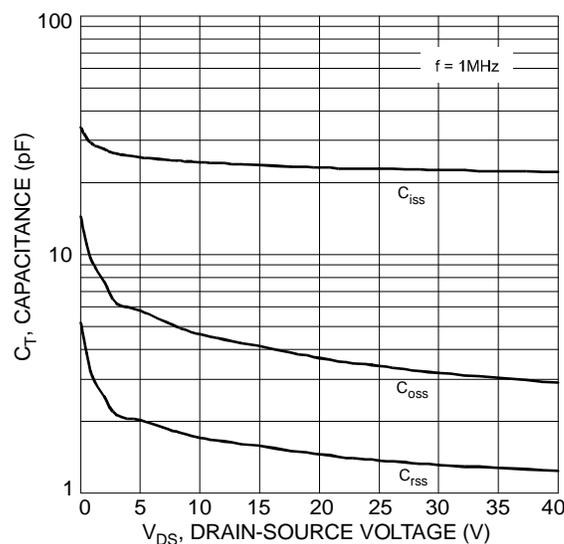


Fig. 6 Typical Total Capacitance

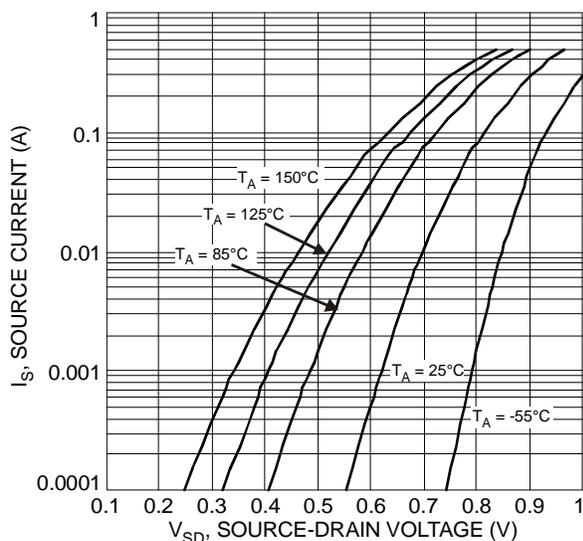
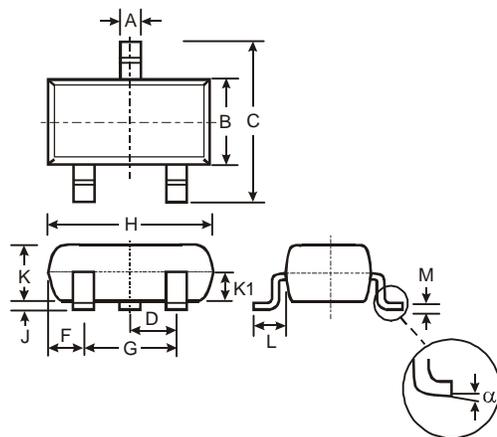


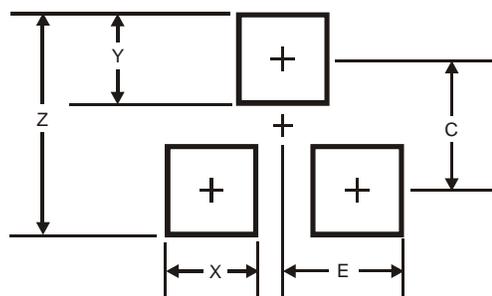
Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

Package Outline Dimensions



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35